CH32F205_207_203 (High Capacity) Datasheet

V2.4

Overview

CH32F205_207_203 (high capacity) series are based 32-bit ARM® Cortex™-M3 core design industrial-grade general-purpose microcontroller. The series has a main frequency up to 144MHz and independent GPIO voltage (separate from system power supply). Resources increased year-on-year random number unit, 4 groups of op-amp comparators, touch detection, increase the number of serial USART/UART to 8 groups, motor timer to 4 groups. In the dedicated interface: USB2.0 high-speed interface (480Mbps) with built-in PHY transceiver, Ethernet MAC to gigabit, and integrated 10M-PHY module, etc. With resources such as clock security, power management, dual-group DMA, ADC, DAC, SPI, I^2C, DVP, SDIO, CAN, FSMC, etc., it can be applied to comprehensive class application scenarios with multiple acquisition and multiple communication directions.

Features

- Core:
  - 32-bit ARM Cortex-M3 core
  - Single-cycle multiplication, hardware division
  - Interruption technology, Fault handling mechanism
  - System main frequency 144MHz
- Memory:
  - Available with up to 128KB volatile data storage area SRAM
  - Available with 480KB program memory CodeFlash (zero-wait application area + non-zero-wait data area)
  - 28KB BootLoader
  - 128B non-volatile system configuration memory
  - 128B user-defined memory
- Power management and low-power consumption:
  - System power supply V_{DD}: 3.3V
  - Independent power supply for GPIO unit $V_{I/O}$: 3.3V
  - Low-power mode: Sleep, Stop, Standby
  - V_{BAT} independently powers RTC and backup register
- Clock & Reset
  - Built-in factory-trimmed 8MHz RC oscillator
  - Built-in 40 KHz RC oscillator
  - Built-in PLL, optional CPU clock up to 144MHz
  - High-speed external 3~25MHz oscillator
  - Low-speed external 32.768 KHz oscillator
  - Power on/down reset, programmable voltage detector
- Real-time clock (RTC): 32-bit independent RTC timer
- 2 groups of 18-channel general-purpose DMA controllers
  - 18 channels, support ring buffer
  - Support TIMx/ADC /DAC/USART/I^2C/SPI/I^2S/SDIO
- 4 groups of OPAs and comparators: connected with ADC and TIMx
- 2 groups of 12-bit DAC
- 2 groups of 12-bit ADC
  - Analog input range: V_{SSA}~V_{DDA}
  - 16 external signals + 2 internal signals
  - On-chip temperature sensor
  - Dual ADC conversion mode
- 16-channels Touch-Key detection
- Multiple timers
  - 4 16-bit advanced-control timers, with dead zone control and emergency brake; can offer PWM complementary output for motor control
  - 4 16-bit general-purpose timers, provide input capture/output comparison/PWM/pulse counting/incremental encoder input
  - 2 basic timers
  - 2 watchdog timers (independent watchdog and window watchdog)

- SysTick: 24-bit self-subtracting counter

- Communication interfaces:
  - 8 USART interfaces (including 5 UARTs)
  - 2 I²C interfaces (support SMBus/PMBus)
  - 3 SPI interfaces (SPI2, SPI3 for I²S2, I²S3)
  - USB2.0 full-speed device interface (full-speed and low-speed)
  - USB2.0 full-speed host/device interface
  - USB2.0 Full-speed OTG interface
  - USB2.0 high-speed host/device interface (built-in PHY)
  - 2 CAN interfaces (2.0B active)
  - SDIO host interface (MMC, SD/SDIO card and CE-ATA)
  - FSMC memory interface
  - Digital Video Interface DVP
  - Gigabit Ethernet Controller MAC, 10M PHY Transceiver
- Fast GPIO port
  - 80 GPIO ports, with 16 external interrupts
- Security features: CRC unit, 96-bit unique ID
- Debug mode: serial 2-wire debug interface
- Package: LQFP48, LQFP64M or LQFP100

Chapter 1 Series product description

The CH32F series are industrial-grade general-purpose enhanced MCUs based on the high performance ARM® Cortex™-M3 32-bit RISC core, which are divided into general-purpose, connectivity, wireless and other categories according to functional resources. They extend each other in terms of package types, peripheral resources and quantities, pin numbers, and device characteristics, but they are compatible with each other in software, functions, and hardware pin configurations. The product iterations and rapid applications provide freedom and convenience for users in product development.

For the features of this series of products, please refer to the datasheet.

For the peripheral function description, usage and register configuration, please refer to "CH32FV2_V3RM".

The data manuals and reference manuals can be downloaded on the official website of WCH:http://www.wch.cn/

For information about the Cortex™-M3 core, please refer to "Cortex-M3 Technical Reference Manual", available for download from ARM website.

This manual is for CH32F205_207_203 (high capacity) series datasheet. Please refer to "CH32F203DS0" for F203 series and "CH32V208DS0" for F208 series.

Table 1-1 Series overview

Low-and-medium capacity general-purpose device (F203)		High capacity general-purpose device (F203)		Connectivity device (F205)	Interconnectivity device (F207)	Wireless device (F208)
32K Flash	64K Flash	128K Flash	256K Flash	128K Flash	256K Flash	128K Flash
10K SRAM	20K SRAM	32K SRAM	64K SRAM	32K SRAM	64K SRAM	64K SRAM
2*ADC(TKey) ADTM 2*GPTM 2*USART SPI I²C USBD USBFS CAN RTC 2*WDG 2*OPA	2*ADC(TKey) ADTM 3*GPTM 4*USART 2*SPI 2*I²C USBD USBFS CAN RTC 2*WDG 2*OPA	2*ADC(TKey) 2*DAC ADTM 3*GPTM 3*USART 2*SPI 2*I²C USBD CAN RTC 2*WDG	2*ADC(TKey) 2*DAC 4*ADTM 4*GPTM 2*BCTM 8*USART/UART 3*SPI(2*I²S) 2*I²C USBD CAN RTC 2*WDG 4*OPA RNG SDIO FSMC	2*ADC(TKey) 2*DAC 4*ADTM 4*GPTM 2*BCTM 5*USART/UART 3*SPI(2*I²S) 2*I²C OTG_FS USBHS(+PHY) 2*CAN RTC 2*WDG 4*OPA RNG SDIO	2*ADC(TKey) 2*DAC 4*ADTM 4*GPTM 2*BCTM 8*USART/UART 3*SPI(2*I²S) 2*I²C OTG_FS USBHS(+PHY) 2*CAN RTC 2*WDG 4*OPA RNG SDIO FSMC DVP ETH-1000MAC 10M-PHY	ADC(TKey) ADTM 3*GPTM GPTM(32) 4*USART/UART 2*SPI 2*I²C USBD USBFS CAN RTC 2*WDG 2*OPA ETH-10M(+PHY) BLE5.3

Note: The number of peripherals or functions of some products in the same category may be limited by the package, please confirm the product package when selecting.

Abbreviations:

ADTM: Advanced-control Timer
GPTM: General-purpose Timer
GPTM (32):32-bit General-purpose Timer
BCTM: Basic Timer
TKey: Touch key
OPA: Operational Amplifier/Comparator
RNG: Random Number Generator
USBD: Universal Serial Bus Full-speed Device
USBFS: Universal Serial Bus Full-speed Host/Device
USBHS: Universal Serial Bus High-speed Host/Device

Chapter 2 Specification

CH32F205_207_203 (high-capacity) series uses the high-performance ARM® Cortex™-M3 32-bit RISC core with a maximum operating frequency of 144MHz, built-in high-speed memory, and multiple buses working synchronously in the system structure, providing rich peripheral functions and enhanced I/O ports. This series has 2 built-in 12-bit ADC modules, 2 12-bit DAC modules, multiple timers, multi-channel touch key capacitance detection (TKey), etc. It also contains standard and dedicated communication interfaces: I²C, I²S, SPI, USART, SDIO, CAN controller, USB2.0 high-speed host/device controller (built-in PHY), digital image interface, Gigabit Ethernet controller, etc.

The rated working voltage of the product is 3.3V, and the working temperature range is -40℃～85℃ in industrial grade. It supports several power-saving operating modes to meet the product's low-power application requirements. Various models in the series are different in terms of resource allocation, number of peripherals, peripheral functions, etc., and can be selected as needed.

2.1 Model comparison

Table 2-1 CH32F205/7/3 Connection/Interconnection/Capacity general-purpose product resource allocation

Resource Differences \ Product Model		CH32F205 RBT6	CH32F207 VCT6	CH32F203 CB	CH32F203 RB	CH32F203 RC	CH32F203 VC
Pin count		64	100	48	64	64	100
Flash (bytes) (1)		128K	256K(2)	128K	128K	256K(2)	256K(2)
SRAM (bytes)		32K	64K(2)	32K	32K	64K(2)	64K(2)
GPIO port count		51	80	37	51	51	80
GPIO power supply		Independent power supply $V_{I/O}$		Shared with V_{DD}	Independent power supply $V_{I/O}$		
Timer	Advanced-control (16-bit)	4	4	1	1	4	4
	General-purpose (16-bit)	4	4	3	3	4	4
	General-purpose (32-bit)	2	2	-	-	2	2
	Watchdog	2 (WWDG + IWDG)					
	SysTick (24-bit)	support					
RTC		support					
ADC/TKey (channel@ unit count)		16@2	16@2	10@2	16@2	16@2	16@2
DAC (unit)		2	2	2	2	2	2
OPA		4	4	4	4	4	4
RNG		1	1	-	1	1	1
Communication interfaces	USART/UART	5	8	3	3	8	8
	SPI	3	3	2	2	3	3
	I²S	2	2	-		2	2
	I²C	2	2	2	2	2	2
	CAN	2	2	1	1	1	1

Resource Differences \ Product Model			CH32F205 RBT6	CH32F207 VCT6	CH32F203 CB	CH32F203 RB	CH32F203 RC	CH32F203 VC
	SDIO		1	1	-		1	1
	DVP		-	1	-		-	
	USB(FS)	USBD	-		1			
		USBHD	1		-			
	USB(HS+PHY)		1		-			
	Ethernet		-	1G MAC+10M PHY	-			
	FSMC		-	1	-			1
CPU clock speed			Max：144MHz					
Rated voltage			3.3V					
Operating temperature			Industrial-grade: -40℃~85℃					
Package			LQFP64M	LQFP100	LQFP48	LQFP64M		LQFP100

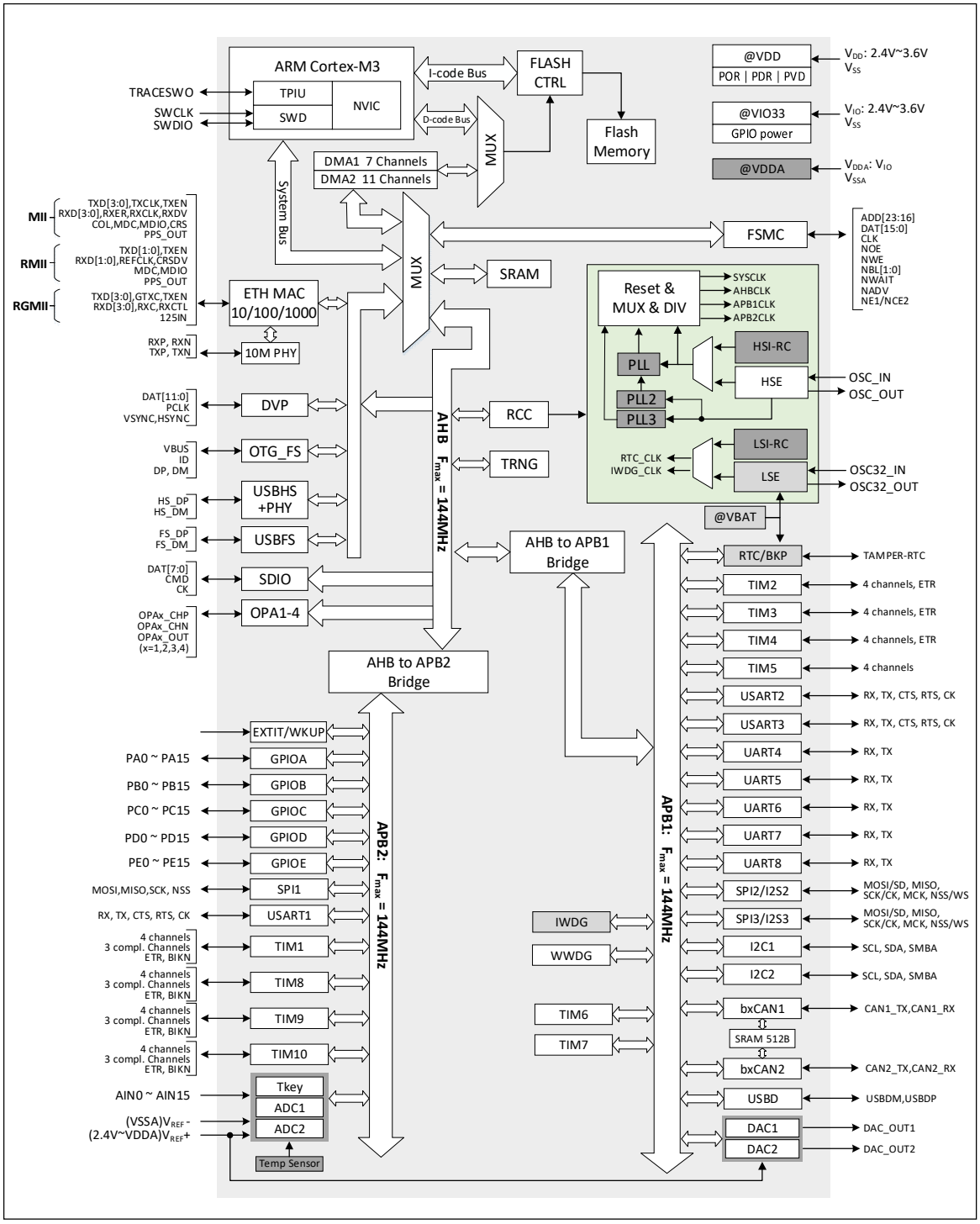
Note: 1. Flash bytes represent zero-wait run area R_{0WAIT}, and the non-zero-wait area is (480K-R_{0WAIT}).

2. The 207 series with 256K FLASH+64K SRAM support user select word to be configured as one of several combinations of (192K FLASH+64K SRAM), (224K FLASH+48K SRAM), (256K FLASH+64K SRAM), (288K FLASH+32K SRAM).

2.2 System architecture

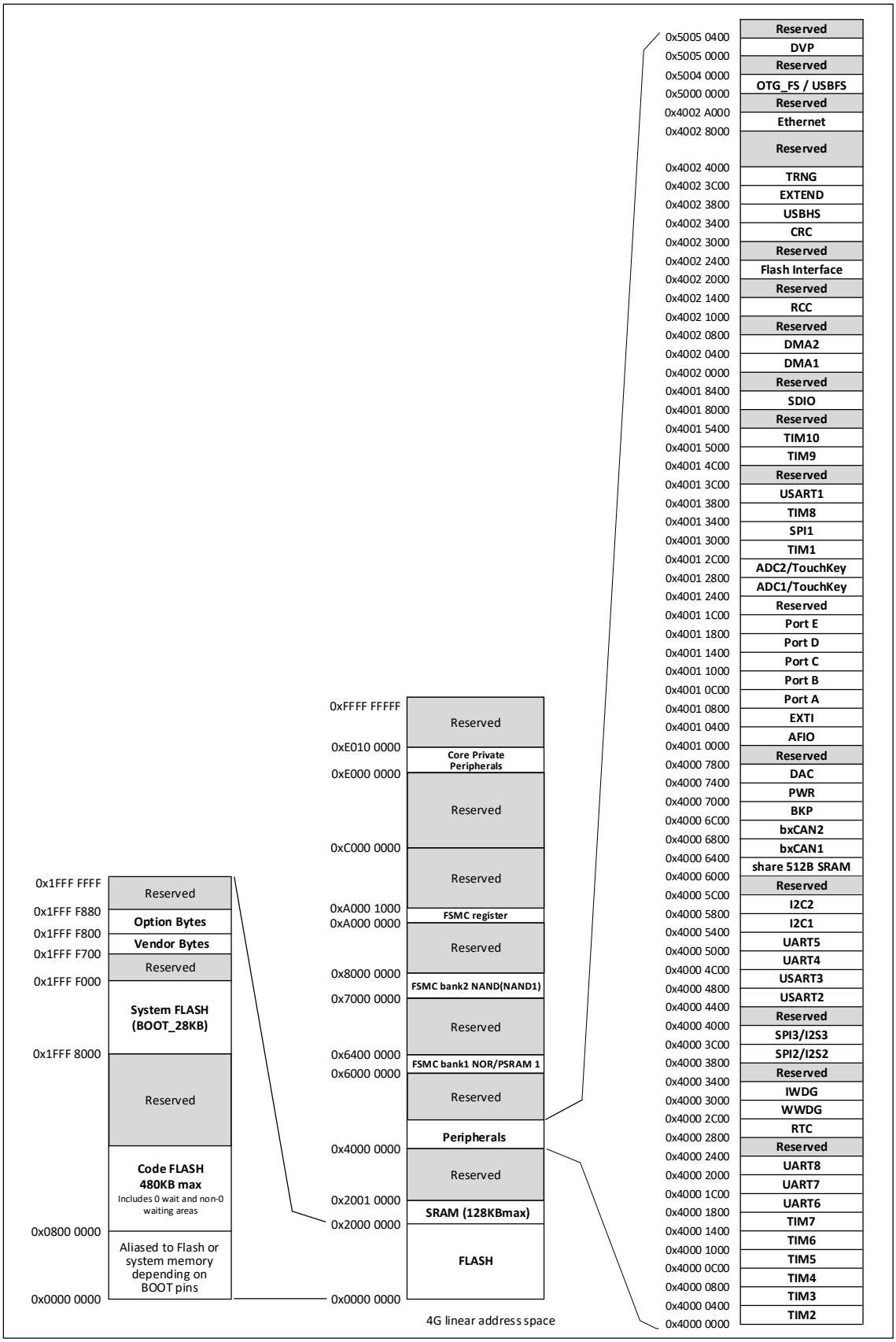
The microcontroller is designed with ARM® Cortex™-M3 as the design core, the architecture of the core, arbitration unit, DMA module, SRAM memory and other parts of the interaction through multiple bus groups. The design integrates a general-purpose DMA controller to reduce the CPU burden and improve access efficiency, and applies a multi-level clock management mechanism to reduce the power consumption of peripherals, as well as a data protection mechanism and automatic clock switching protection to increase system stability. The following figure shows the overall internal architecture of the series.

Figure 2-1 System block diagram



2.3 Memory map

Figure 2-2 Memory address map



2.4 Clock tree

Four groups of clock sources are introduced into the system: internal high-frequency RC oscillator (HSI), internal low-frequency RC oscillator (LSI), external high-frequency oscillator (HSE), and external low-frequency oscillator (LSE). Among them, the low-frequency clock source provides the clock reference for RTC and independent watchdog. The high-frequency clock source is directly or indirectly multiplied by the PLL and output as the system clock (SYSCLK). The system clock is then provided by each prescaler to provide the AHB domain, APB1 domain, APB2 domain peripheral control clock and sampling or output clock. Some modules need to be directly provided by the PLL clock.

Figure 2-3 CH32F205/207 clock tree block diagram

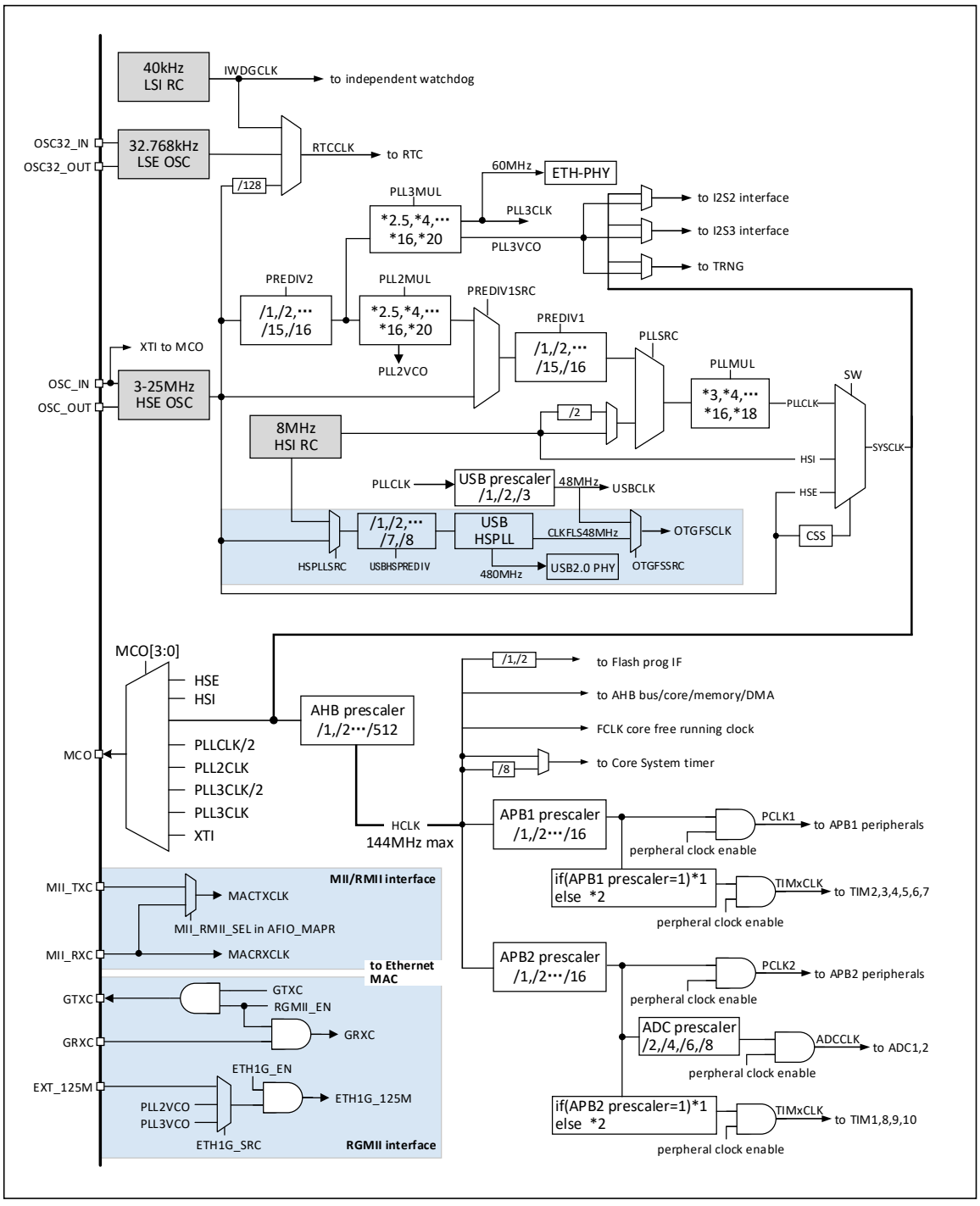
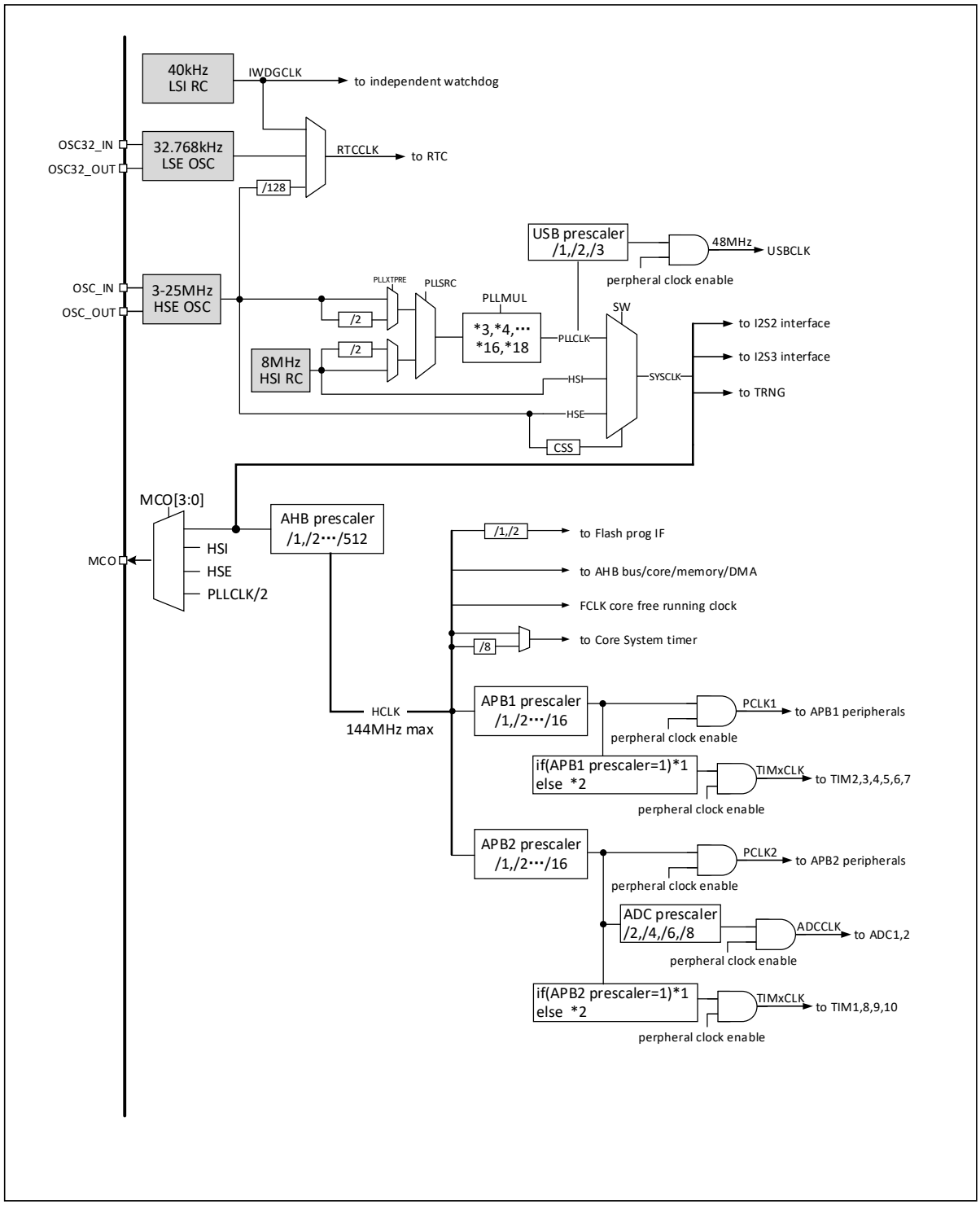


Figure 2-4 CH32F203 (high capacity) clock tree block diagram



Note: When using USB, the CPU clock speed must be 48MHz or 96MHz or 144MHz. When the system wakes up from Stop mode or Standby mode, the system will automatically select HSI as the system clock frequency

2.5 Functional description

2.5.1 ARM Cortex-M3 Core

ARM® Cortex™-M3 is a 32-bit embedded processor that provides the low-cost platform, reduced pin count, and reduced system power needed to implement an MCU, as well as superior computational performance and advanced interrupt system response. Its additional code efficiency leverages the high performance of the ARM core on the storage space of typical 8-and 16-bit systems.

- Harvard architecture, add branch prediction function, improve pipeline processor performance play
- Tail-Chaining is a hardware-based technology that improves efficiency
- Core low-power 3 modes, more effective power control
- Advanced Fault handling mechanism, debugging solutions, etc.

The CH32F2x series controllers have a built-in ARM core and are therefore compatible with most ARM tools and software.

2.5.2 On-chip memory and boot mode

Up to 128K bytes of built-in SRAM area, used to store data, data will be lost after power failure. The specific capacity depends on the corresponding chip model.

The built-in program flash memory storage area (Code FLASH) of up to 480K bytes is used for user's application and constant data storage. This includes a zero-wait program run area and a non-zero-wait area. The specific size of the area corresponds to the chip model.

Built-in 28K byte system memory (System FLASH), used for system boot program storage (manufacturer curing boot loader).

128 bytes are used for system non-volatile configuration word storage, and 128 bytes are used for user selection word storage.

At startup, one of 3 boot modes can be selected through the boot pins (BOOT0 and BOOT1):

- Boot from program flash
- Boot from system memory
- Boot from internal SRAM

The bootloader is stored in the system memory, and the contents of the program Flash memory storage can be reprogrammed through the USART1 and USB interface.

2.5.3 Power supply scheme

- V_{DD} = 2.4～3.6V: Power supply for some I/O pins and internal voltage regulator.
- $V_{I/O}$ = 2.4～3.6V: It supplies power to most of the I/O pins and the Ethernet module, which determines the pin output high voltage amplitude. Normal work during operation, the $V_{I/O}$ voltage cannot be higher than the V_{DD} voltage.
- V_{DDA} = 2.4～3.6V: It supplies power to the analog part of the high-frequency RC oscillator, ADC, temperature sensor, DAC and PLL. The V_{DDA} voltage must be the same as the $V_{I/O}$ voltage (If V_{DD} is powered down and $V_{I/O}$ is powered on, Then V_{DDA} must be powered on and consistent with $V_{I/O}$). When using ADC, V_{DDA} must not be less than 2.4V.
- V_{BAT} = 1.8～3.6V: When V_{DD} is turned off, (through the internal power switch) independently powers the RTC, external low-frequency oscillator and backup registers. (Pay attention to V_{BAT} power supply)

2.5.4 Power supply monitor

This product integrates a power-on reset (POR)/power-down reset (PDR) circuit, which is always in working

condition to ensure that the system is in supply. It works when the power exceeds 2.4V; when V_{DD} is lower than the set threshold ($V_{POR/PDR}$), the device is placed in the reset state without using an external reset circuit.

In addition, the system is equipped with a programmable voltage monitor (PVD), which needs to be turned on by software to compare the voltage of V_{DD} power supply with the set threshold V_{PVD}.

Turn on the corresponding edge interrupt of PVD, and you can receive interrupt notification when V_{DD} drops to the PVD threshold or rises to the PVD threshold. Refer to Chapter 4 for the values of $V_{POR/PDR}$ and V_{PVD}.

2.5.5 Voltage regulator

After reset, the regulator is automatically turned on, and there are 3 operation modes according to the application mode.

- ON mode: Normal operation, providing stable core power.
- Low-power mode: When the CPU enters Stop mode, the regulator can be selected to run with low-power consumption.
- OFF mode: When the CPU enters Standby mode, it automatically switches the regulator to this mode, the voltage regulator output is in high impedance, and the core power.

The voltage regulator is always ON after reset. It is OFF in Standby mode, and the regulator output is in high impedance.

2.5.6 Low-power mode

The system supports 3 low-power modes, which can be selected for low-power consumption, short start-up time and multiple wake-up events to achieve the best balance.

- Sleep mode

In Sleep mode, only the CPU clock is stopped, but all peripheral clocks are powered normally and the peripherals are in a working state. This mode is the shallowest low-power mode, but it is the fastest mode to wake up the system.
Exit condition: any interrupt or wake-up event.

- Stop mode

In this mode, the FLASH enters low-power mode, and the PLL, HSI RC oscillator and HSE crystal oscillator are turned off. In the case of keeping the contents of SRAM and registers not lost, the Stop mode can achieve the lowest power consumption.
Exit conditions: any external interrupt/event (EXTI signal), external reset signal on NRST, IWDG reset, among which EXTI signal includes one of 16 external I/O ports, PVD output, RTC alarm clock, Ethernet wake-up signal or USB wake-up signal.

- Standby mode

In this mode, the main LDO of the system is turned off, the low-power LDO supplies power to the wake-up circuit, all other digital circuits are powered off, and the FLASH is powered off. The system wakes up from Standby mode will generate a reset, and SBF (PWR_CSR) will be set at the same time. After waking up, check the SBF status to know the low-power mode before waking up. SBF is cleared by the CSBF (PWR_CR) bit. In the Standby mode, the contents of 32KB of SRAM can be kept (depending on the planning and configuration before going to bed), and the contents of the backup registers are kept.
Exit conditions: any external interrupt/event (EXTI signal), external reset signal on NRST, IWDG reset, a rising edge on the WKUP pin, where EXTI signal includes one of 16 external I/O ports, RTC alarm clock,

Ethernet Wake-up signal, USB Wake-up signal.

2.5.7 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit uses a fixed polynomial generator to generate a CRC code from a 32-bit data word. In many applications, CRC-based technology is used to verify the consistency of data transmission or storage. Within the scope of the EN/IEC 60335-1 standard, a means of detecting flash errors is provided. The CRC calculation unit can be used to calculate the signature of the software in real time and compare it with the signature generated when the software is linked and generated.

2.5.8 Nested vector interrupt controller (NVIC)

The system product has a built-in nested vector interrupt controller (NVIC), which manages 88 maskable interrupt channels and 16 core interrupt channels. And 16 priority levels can be configured.

- Tightly coupled NVIC enables low latency interrupt response processing
- Vectorized interrupt design implements vector entry address directly into the core
- 16 levels of nesting, dynamic modification
- Allow early processing of interrupts
- Support late arrival of higher priority interrupt responses
- Support for break tail link function
- Provide first response to unmaskable interruptions
- Automatic stacking and recovery on interrupt entry and exit, no additional instruction overhead

The module provides flexible interrupt management capabilities with minimal interrupt latency.

2.5.9 External interrupt/event controller (EXTI)

The external interrupt/event controller contains a total of 19 edge detectors for generating interrupt/event requests. Each interrupt line can independently configure its trigger event (rising edge or falling edge or both edges), and can be individually masked; the suspend register maintains all interrupt request states. EXTI can detect that the pulse width is smaller than the clock period of the internal APB2. Up to 80 general-purpose I/O ports can be connected to 16 external interrupt lines.

2.5.10 General DMA controller

The system has built-in 2 groups of general-purpose DMA controllers, manages 18 channels in total, and flexibly handles high-speed data transmission from memory to memory, peripherals to memory, and memory to peripherals, and supports ring buffer mode. Each channel has a dedicated hardware DMA request logic to support one or more peripherals' access requests to the memory. The access priority, transfer length, source address and destination address of the transfer can be configured.

The main peripherals used by DMA include: general/advanced/basic timers TIMx, DAC, I²S, USART, I²C, SPI and SDIO.

Note: DMA and CPU access the system SRAM after arbitration by the arbiter.

2.5.11 Clock and Boot

The system clock source HSI is turned on by default. After the clock is not configured or reset, the internal 8MHz RC oscillator is used as the default CPU clock, and then an external 3~25MHz clock or PLL clock can be additionally selected. When the clock security mode is turned on, if the HSE is used as the system clock (directly or indirectly), the system clock will automatically switch to the internal RC oscillator when the external clock is detected to be invalid, and the HSE and PLL will be automatically turned off at the same

time; in low-power consumption mode, the system will automatically switch to the internal RC oscillator after waking up. If the clock interrupt is enabled, the software can receive the corresponding interrupt.

Multiple prescalers are used to configure the frequency of AHB. The high-speed APB (APB2) and low-speed APB (APB1) regions provide peripheral clocks with a maximum frequency of 144MHz. Refer to the clock tree block diagram in Figure 2-3. The I^2S unit is clocked from another dedicated PLL (PLL3) so that the I^2S master clock can generate all the standard between 8 KHz and 192 KHz of sampling frequencies.

2.5.12 Real time clock (RTC) and backup registers

The RTC and the backup register are in the backup power supply area inside the system. When V_{DD} is valid, it is powered by V_{DD}, and when V_{DD} is invalid, the internal power is automatically switched to the V_{BAT} pin.

The RTC real-time clock is a set of 32-bit programmable counters, and the time base supports 20-bit prescaler for measurement in a longer period of time. The clock reference source is a high-speed external clock divided by 128 (HSE/128), external crystal low-frequency oscillator (LSE) or internal low-power RC oscillator (LSI). The LSE also has a backup power supply area, so when the LSE is selected as the RTC time base, the RTC setting and time can remain unchanged after the system resets or wakes up from Standby mode.

The backup register contains up to 42 16-bit registers, which can be used to store 84 bytes of user application data. This data can continue to be maintained after wake-up from Standby, or system Reset or power Reset. When the intrusion detection function is turned on, once the intrusion detection signal is valid, all contents in the backup register will be cleared.

2.5.13 Analog-to-digital converter (ADC) and touch key capacitance detection (TKey)

The product is embedded with 2 12-bit analog/digital converters (ADC), sharing up to 16 external channels and 2 internal channels for sampling. The programmable channel sampling time can realize single, continuous, scanning or discontinuous conversion. And supports dual ADC conversion mode. The analog watchdog function is provided to allow very precise monitoring of one or more selected channels for monitoring the signal voltage of the channel. It supports external event-triggered conversion, the trigger source includes the internal signal and external pin of the on-chip timer; it also supports the use of DMA operations.

ADC internal channel sampling includes 1 channel of built-in temperature sensor sampling and 1 channel of internal reference power sampling. The temperature sensor generates a voltage that varies linearly with temperature. The temperature sensor is internally connected to the IN16 input channel, which is used to convert the output of the sensor to a digital value.

The capacitance touch key detection unit provides up to 16 detection channels, multiplexing the external channels of the ADC module. The detection result is converted and output by the ADC module, and the state of the touch key is recognized by the user software.

2.5.14 Digital-to-analog converter (DAC)

The product is embedded with two 12-bit voltage output digital/analog converters (DAC), converting 2 digital signals to 2 analog voltage signals and outputting them, supporting independent or synchronous conversion of dual DAC channels, and supporting external event triggered conversion, with trigger sources including internal signals of on-chip timer and external pins (EXTI line 9). Triangle wave and noise generation can be implemented. Support using DMA operation.

2.5.15 Timer and watchdog

The timers in the system include advanced timers, general timers, basic timers, watchdog timers, and system time base timers. The number of timers included in different products in the series is different, please refer to Table 2-2 for details.

Table 2-2 Timer comparison

Timer		Resolution	Count Type	Time Base	DMA	Function
Advanced-control timer	TIM1	16 bits	Up Down Up/down	APB2 time domain 16-bit divider	Support	PWM complementary output, single pulse output Input capture Output compare Timer count
	TIM8					
	TIM9					
	TIM10					
General-purpose timer	TIM2	16 bits	Up Down Up/down	APB1 time domain 16-bit divider	Support	Input capture Output compare Timer count
	TIM3					
	TIM4					
	TIM5	16 bits				
Basic timer	TIM6	16 bits	Up	APB1 time domain 16-bit divider	Support	Timed counting
	TIM7					
Window watchdog		7 bits	Down	APB1 time domain 4 types of frequency division	Not support	Timing Reset the system (normal work)
Independent watchdog		12 bits	Down	APB1 time domain 7 types of frequency division	Not support	Timing Reset the system (normal work + low-power work)
SysTick Timer		24 bits	Down	SYSCLK or SYSCLK/8	Not support	Timing

- Advanced-control timer

The advanced-control timer is a 16-bit auto-loading up/down counter with a 16-bit programmable prescaler. In addition to the complete general-purpose timer function, it can be regarded as a three-phase PWM generator distributed to 6 channels, with a complementary PWM output function with dead zone insertion, allowing the timer to be updated after a specified number of counter cycles to repeat counting cycle, braking function, etc. Many functions of the advanced-control timer are the same as the general timer, and the internal structure is also the same. Therefore, the advanced control timer can cooperate with other TIM timers through the timer link function to provide synchronization or event link functions.

- General-purpose timer

The general-purpose timer is a 16-bit or 32-bit auto-loading up/down counter with a programmable 16-bit prescaler and 4 independent channels. Each channel supports input capture, output comparison, and PWM generation and single pulse mode output. It can also work with advanced control timers through the timer link

function to provide synchronization or event link functions. In Debug mode, the counter can be frozen while the PWM outputs are disabled, thereby cutting off the switches controlled by these outputs. Any general-purpose timer can be used to generate PWM output. Each timer has an independent DMA request mechanism. These timers can also process signals from incremental encoders, as well as digital outputs from 1 to 3 Hall sensors.

- Independent Watchdog

The independent watchdog is a configurable 12-bit down counter that supports 7 frequency division factors. The clock is provided by an internal independent 40 KHz RC oscillator (LSI); because the LSI is independent of the main clock, it can run in Stop and Standby modes. IWDG is outside the main program and can work completely independently. Therefore, it is used to reset the entire system when a problem occurs, or as a free timer to provide timeout management for the application. It can be configured as software or hardware to start the watchdog through the option byte. In Debug mode, the counter can be frozen.

- Window Watchdog

The window watchdog is a 7-bit down counter and can be set to free-running. It can be used to reset the entire system when a problem occurs. It is driven by the main clock and has an early warning interrupt function; in Debug mode, the counter can be frozen.

- SysTick Timer

This is a 24-bit optional increment or decrement counter that comes with the core controller. It is used to generate SYSTICK anomalies (exception number: 15). It can be dedicated to the real-time operating system (RTOS) to provide a "heartbeat" tick for the system, or it can be used as a standard 24-bit counter. It has an automatic reload function and a programmable clock source.

2.5.16 Communication interface

2.5.16.1 Universal Synchronous/Asynchronous Receiver Transmitter (USART)

The product provides 3 groups of Universal Synchronous/Asynchronous Receiver Transmitters (USART1, USART2, USART3), and 5 groups of Universal Asynchronous Receiver Transmitters (UART4, UART5, UART6, UART7, UART8). It supports full-duplex asynchronous communication, synchronous one-way communication and half-duplex single-wire communication. It also supports LIN (Local Interconnect Network), compatible with ISO7816 smart card protocol and IrDA SIR ENDEC transmission codec specification, and modem (CTS/RTS hardware flow control) operation. It also allows multi-processor communication. It uses a fractional baud rate generator system and supports DMA operation continuous communication.

2.5.16.2 Serial Peripheral Interface (SPI)

Up to 3 groups of serial peripherals interface (SPI) provide master or slave operation, dynamic switching. Support multi-master mode, full-duplex or half-duplex synchronous transmission, support basic SD card and MMC mode. Programmable clock polarity and phase, data bit width provides 8 or 16-bit selection, hardware CRC generation/check for reliable communication, and continuous communication support for DMA operation.

2.5.16.3 I2S (audio) interface

Up to 2 sets of standard I^2S interfaces (multiplexed with SPI2 and SPI3) work in master or slave mode. The

software is configurable for 16/32-bit packet transfer frames and supports audio sampling frequencies from 8KHz to 192KHz, supporting 4 audio standards. In master mode, its master clock can be output to an external DAC or CODEC (decoder) at a fixed 256x audio sampling frequency, with DMA support.

2.5.16.4 I2C bus

Up to 2 I²C bus interfaces can work in multi-master mode or Slave mode, perform all I²C Bus specific timing, protocol, arbitration, etc. It supports both standard and fast speed, and is compatible with SMBus2.0.

The I²C interface provides 7-bit or 10-bit addressing, and supports dual slave addressing in 7-bit Slave mode. It integrates built-in hardware CRC generator/checker. It also supports DMA operation and supports SMBus bus version 2.0 / PMBus bus.

2.5.16.5 Controller Area Network (CAN)

The CAN interface is compatible with specifications 2.0A and 2.0B (active), the baud rate is up to 1Mbits/s, and it supports time-triggered communication functions. It can receive and send standard frames with 11-bit identifiers, as well as extended frames with 29-bit identifiers. It has 3 sending mailboxes and 2 3-level deep receiving FIFOs.

Products with 2 groups of CAN controllers share 28 configurable filters and 512 bytes of SRAM memory resources.

With 1 group of CAN controller products, there are only 14 configurable filters, and share a dedicated 512-byte SRAM memory with the USBD module for data transmission and reception. When USBD and CAN are used at the same time, in order to prevent access to SRAM conflicts, USBD can only use the lower 384 bytes.

2.5.16.6 Universal Serial Bus device (USBD)

The product is embedded with a USB2.0 full-speed controller, which complies with the USB2.0 full-speed standard. USBD provides 16 configurable USB device endpoints, supports low-speed devices and full-speed devices, supports control/batch/synchronization/interrupt transmission, double buffer mechanism, USB suspend/resume operations, and has standby/wake-up functions. The USB dedicated 48MHz clock is directly generated by the internal main PLL frequency division.

2.5.16.7 Universal Serial Bus USB2.0 full-speed Host/Device controller (USBFS)

The USB2.0 full-speed host controller and device controller (USBFS) follow the USB2.0 full-speed standard. It provides 16 configurable USB device endpoints and a set of host endpoints. Support control/batch/synchronization/interrupt transmission, double buffer mechanism, USB bus suspend/resume operation, and provide standby/wake-up functions. The 48MHz clock dedicated to the USBFS module is directly generated by the internal main PLL frequency division (the PLL must be 144MHz or 96MHz or 48MHz).

2.5.16.8 Universal Serial Bus USB2.0 full-speed OTG (OTG-FS)

OTG_FS is a dual role USB controller that supports both host-side and device-side functionality and is compatible with the On-The-Go Supplement to the USB2.0 specification. The controller can also be configured as a host-side only or device-side only controller, compatible with the USB2.0 Full Speed specification. The controller uses a 48MHz clock derived from PLL divider and key features include.

- Support for the USB On-The-Go Supplement (physical layer of OTG_FS controller), defined as an optional item OTG protocol in the Revision 1.3 specification

- USB full-speed host, USB full/low-speed device, USB dual role device can be configured via software
- Provides power saving function
- Support control transfer, batch transfer, interrupt transfer, real-time/synchronous transfer
- Provides bus reset, suspend, wake up and resume functions

2.5.16.9 Universal Serial Bus USB 2.0 high-speed host/device controller (USBHS)

The USB 2.0 High Speed Controller has a dual role as host controller and device controller and has an embedded USB-PHY transceiver unit. When acting as a host controller, it can support low-speed, full-speed, and high-speed USB devices. When used as a device controller, it can be flexibly set to low-speed, full-speed, or high-speed modes to suit a variety of applications. Key features include:

- Support USB 2.0, USB 1.1, USB 1.0 protocol specification
- Support control transfer, batch transfer, interrupt transfer, real-time/synchronous transfer
- Provides bus reset, suspend, wake up and resume functions
- High-speed HUB support
- Provide 16 groups of up and down transmission channels in device mode, supporting configuration of 16 endpoint numbers
- All endpoints except device endpoint 0 support packets up to 1024 bytes, with double buffering available

2.5.16.10 Digital Video Interface (DVP)

The Digital Video Port (DVP) is used to connect to the camera module to obtain the image data stream. It provides 8/10/12bit parallel interface way of communication. It supports image data organized in original line and frame formats, such as YUV, RGB, etc., and also supports compressed image data streams such as JPEG format. When receiving, it mainly relies on VSYNC and HSYNC signal synchronization. Support image cropping function.

2.5.16.11 SDIO host controller

The SDIO host interface provides interfaces for the operation of multimedia cards (MMC), SD memory cards, SDIO cards, and CE-ATA devices. Three different data bus modes are supported: 1-bit (default), 4-bit and 8-bit. In 8-bit mode, the interface enables data transfer rates up to 48 MHz. currently the interface is fully compatible with the Multimedia Card System Specification 4.2 (forward compatible), SD I/O Card Specification 2.0, SD Memory Card Specification 2.0, and CE-ATA Digital Protocol Specification 1.1.

2.5.16.12 Configurable Static Memory Controller (FSMC)

The FSMC interface provides mainly synchronous or asynchronous memory interfaces, supporting SRAM, PSRAM, NOR and NAND devices. The internal AHB transfer signal is converted to a suitable external communication protocol, allowing continuous access to 8/16/32-bit data. The sampling delay time is flexible and configurable to meet different device timings.

In addition, FSMC can also be used for most graphic LCD controller interfaces. It supports the Intel 8080 and Motorola 6800 models, making it easy to build simple graphics application environments or high-performance solutions for dedicated acceleration controllers.

2.5.16.13 Gigabit Ethernet controller (MAC, +10M PHY)

The product provides a Gigabit Ethernet controller (MAC) compliant with IEEE 802.3-2002 standard, acting as a data link layer with Link rate supporting up to 1Gbps, providing MII/RMII/RGMII interface to connect external PHY (Gigabit/100Gigabit/speed adaptive, 10M PHY transceiver built-in), when applied, combined

with TCP/IP protocol stack interface to achieve the development of network products. Main features include.

- Compliant with IEEE.802.3 protocol specification and design
- Provides RGMII, RMII, MII interfaces to connect to external Ethernet PHY transceivers
- Support full-duplex operation, supporting 10/100/1000Mbps data transmission rate
- Hardware automatically performs IPv4 and IPv6 packet integrity checks, IP/ICMP/UDP/TCP packet checks and computer frame length padding
- Multiple MAC address filtering modes
- SMI can configure and manage the external PHY

2.5.17 General-purpose input and output (GPIO)

The system provides 5 groups of GPIO ports with a total of 80 GPIO pins. Each pin can be configured by software as output (push-pull or open-drain), input (with or without pull-up or pull-down) or multiplexed peripheral function port. Most GPIO pins are shared with digital or analog multiplexed peripherals. Except for ports with analog input functions, all GPIO pins have high current passing capabilities. A locking mechanism is provided to freeze the I/O configuration to avoid accidental writing to the I/O register.

Most of the I/O pins in the system are provided by $V_{I/O}$. Changing the $V_{I/O}$ power supply will change the high value of the I/O pin output level to adapt to the external communication interface level. Please refer to the pin description for specific pins.

2.5.18 Random Number Generator (RNG)

A random number generator is embedded in the product, which provides a 32-bit random number through an internal analog circuit.

2.5.19 Operational amplifier/comparator (OPA)

The product has built-in 4 groups of operational amplifiers/comparators, and the internal selection is linked to the ADC and TIMx peripherals. Its input and output can be selected by changing the configuration to select multiple channels. It supports to amplify the external analog small signal and send it to the ADC to realize the small signal ADC conversion. It can also complete the signal comparator function. The comparison result is output by GPIO or directly connected to the input channel of TIMx.

2.5.20 Serial 2-wire Debug Interface (SWD)

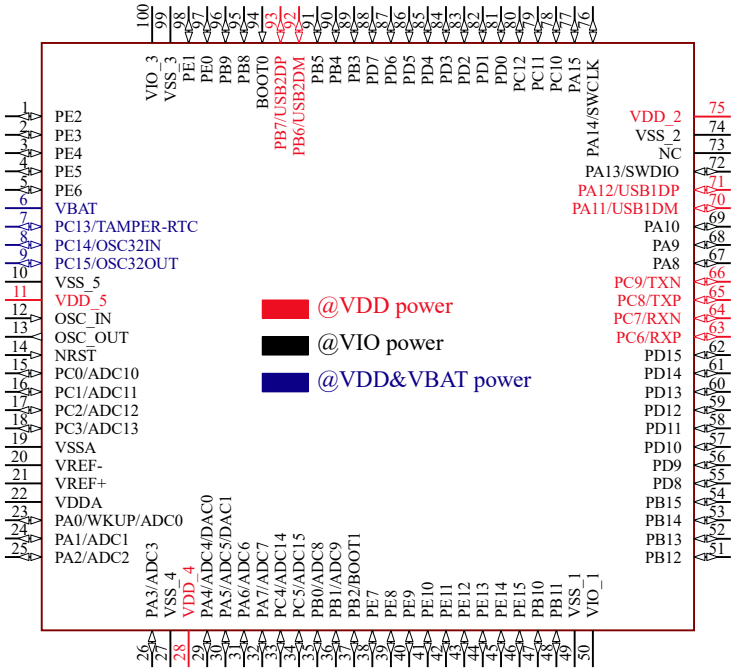
The ARM core comes with the SW-DP interface, which is a serial 2-wire debug interface. It includes SWDIO and SWCLK pins. The default debug interface pin function is turned on after system power on or reset.

Chapter 3 Pinouts and pin definition

3.1 Pin Arrangement

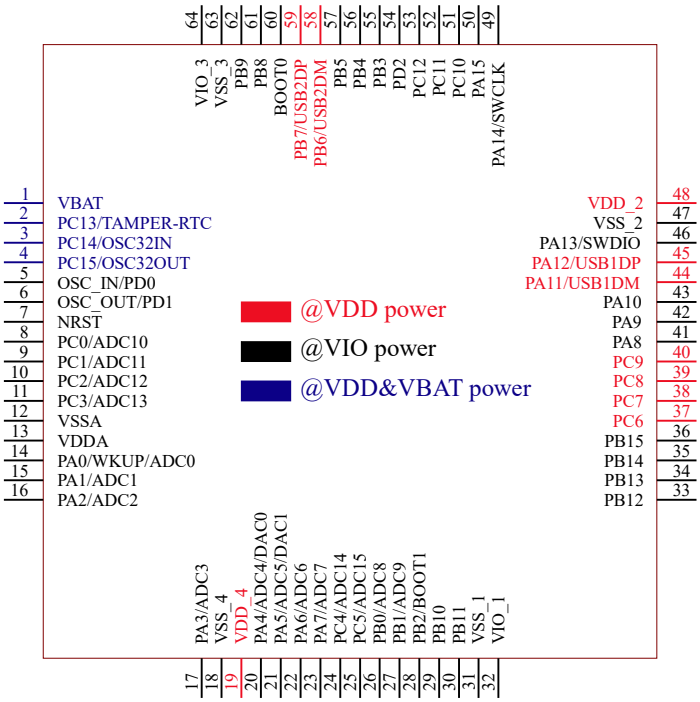
3.1.1 Interconnection type F207

CH32F207VCT6



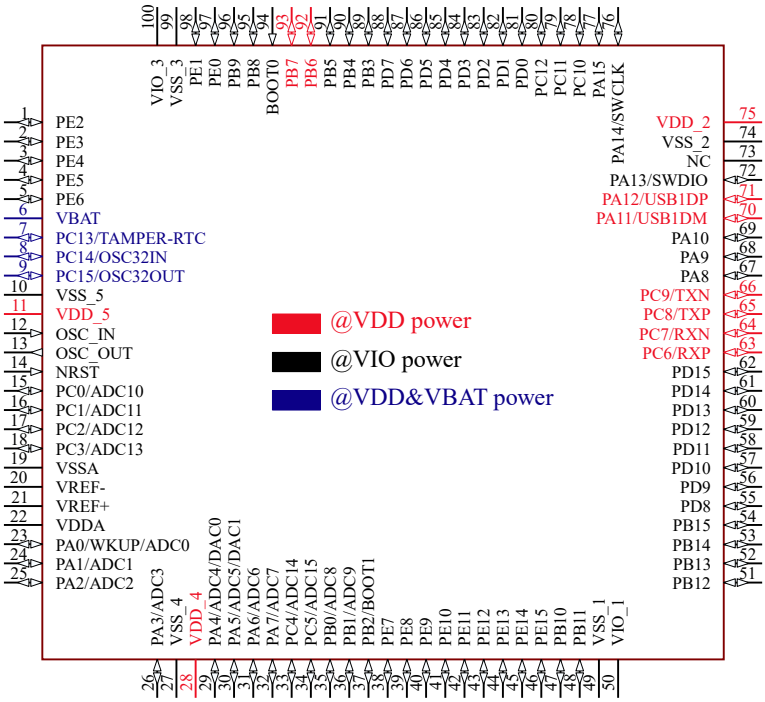
3.1.2 Connection type F205

CH32F205RBT6

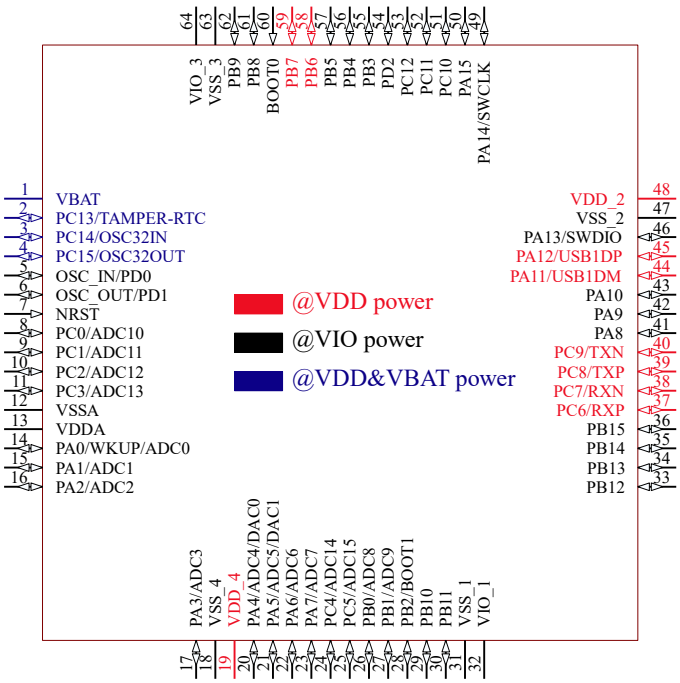


3.1.3 High capacity general-purpose F203

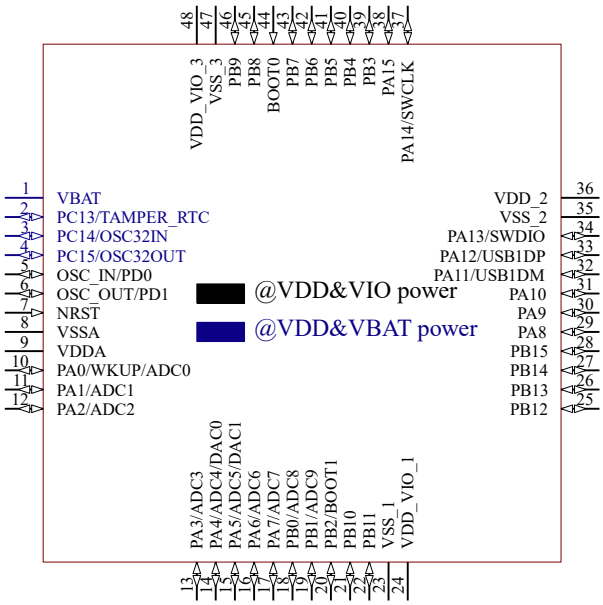
CH32F203VCT6



CH32F203RC/BT6



CH32F203CBT6



3.2 Pin description

Table 3-1 CH32F203_205_207xB/xC pin definitions

Note: The pin function descriptions in the table below are for all functions and do not relate to specific model products. Peripheral resources may vary between models, so please check the availability of this function according to the product model resource table before viewing.

Pin No.			Pin name	Pin type (1)	I/O level	Main function (after reset)	Default alternate function	Remapping function
LQFP48	LQFP64M	LQFP100						
-	-	1	PE2	I/O	FT	PE2	FSMC_A23	TIM10_BKIN_2
-	-	2	PE3	I/O	FT	PE3	FSMC_A19	TIM10_CH1N_2
-	-	3	PE4	I/O	FT	PE4	FSMC_A20	TIM10_CH2N_2
-	-	4	PE5	I/O	FT	PE5	FSMC_A21	TIM10_CH3N_2
-	-	5	PE6	I/O	FT	PE5	FSMC_A22	
1	1	6	V_{BAT}	P	-	V_{BAT}		
2	2	7	PC13-TAMPER-RTC(2)	I/O	-	PC13(3)	TAMPER-RTC	TIM8_CH4_1
3	3	8	PC14-OSC32_IN(2)	I/O/A	-	PC14(3)	OSC32_IN	TIM9_CH4_1
4	4	9	PC15-OSC32_OUT(2)	I/O/A	-	PC15(3)	OSC32_OUT	TIM10_CH4_1
-	-	10	V_{SS_5}	P	-	V_{SS_5}		
-	-	11	V_{DD_5}	P	-	V_{DD_5}		
5	5	12	OSC_IN	I/A	-	OSC_IN		PD0(4)
6	6	13	OSC_OUT	O/A	-	OSC_OUT		PD1(4)
7	7	14	NRST	I	-	NRST		
-	8	15	PC0	I/O/A	-	PC0	ADC_IN10 TIM9_CH1N UART6_TX ETH_RGMII_RXC	
-	9	16	PC1	I/O/A	-	PC1	ADC_IN11 TIM9_CH2N UART6_RX ETH_MII_MDC ETH_RMII_MDC ETH_RGMII_RXCTL	
-	10	17	PC2	I/O/A	-	PC2	ADC_IN12 TIM9_CH3N UART7_TX OPA3_CH1N ETH_MII_TXD2	

Pin No.			Pin name	Pin type (1)	I/O level	Main function (after reset)	Default alternate function	Remapping function
LQFP48	LQFP64M	LQFP100						
							ETH_RGMII_RXD0	
-	11	18	PC3	I/O/A	-	PC3	ADC_IN13 TIM10_CH3 UART7_RX OPA4_CH1N ETH_MII_TX_CLK ETH_RGMII_RXD1	
8	12	19	V_{SSA}	P	-	V_{SSA}		
-	-	20	V_{REF-}	P	-	V_{REF-}		
-	-	21	V_{REF+}	P	-	V_{REF+}		
9	13	22	V_{DDA}	P	-	V_{DDA}		
10	14	23	PA0-WKUP	I/O/A	-	PA0	WKUP USART2_CTS ADC_IN0 TIM2_CH1 TIM2_ETR TIM5_CH1 TIM8_ETR OPA4_OUT0 ETH_MII_CRS_WKUP ETH_RGMII_RXD2	TIM2_CH1_ETR_2 TIM8_ETR_1
11	15	24	PA1	I/O/A	-	PA1	USART2_RTS ADC_IN1 TIM5_CH2 TIM2_CH2 OPA3_OUT0 ETH_MII_RX_CLK ETH_RMII_REF_CLK ETH_RGMII_RXD3	TIM2_CH2_2 TIM9_BKIN_1
12	16	25	PA2	I/O/A	-	PA2	USART2_TX TIM5_CH3 ADC_IN2 TIM2_CH3 TIM9_CH1 TIM9_ETR OPA2_OUT0 ETH_MII_MDIO ETH_RMII_MDIO ETH_RGMII_GTXC	TIM2_CH3_1 TIM9_CH1_ETR_1
13	17	26	PA3	I/O/	-	PA3	USART2_RX	TIM2_CH4_1

Pin No.			Pin name	Pin type (1)	I/O level	Main function (after reset)	Default alternate function	Remapping function
LQFP48	LQFP64M	LQFP100						
				A			TIM5_CH4 ADC_IN3 TIM2_CH4 TIM9_CH2 OPA1_OUT0 ETH_MII_COL ETH_RGMII_TXEN	TIM9_CH2_1
-	18	27	V_{SS_4}	P	-	V_{SS_4}		
-	19	28	V_{DD_4}	P	-	V_{DD_4}		
14	20	29	PA4	I/O/A	-	PA4	SPI1_NSS USART2_CK ADC_IN4 DAC_OUT1 TIM9_CH3 DVP_HSYNC	SPI3_NSS I²S3_WS TIM9_CH3_1
15	21	30	PA5	I/O/A	-	PA5	SPI1_SCK ADC_IN5 DAC_OUT2 OPA2_CH1N DVP_VSYNC	TIM10_CH1N_1 USART1_CTS_2 USART1_CK_3
16	22	31	PA6	I/O/A	-	PA6	SPI1_MISO TIM8_BKIN ADC_IN6 TIM3_CH1 OPA1_CH1N DVP_PCLK	TIM1_BKIN_1 USART1_TX_3 UART7_TX_1 TIM10_CH2N_1
17	23	32	PA7	I/O/A	-	PA7	SPI1_MOSI TIM8_CH1N ADC_IN7 TIM3_CH2 OPA2_CH1P ETH_MII_RX_DV ETH_RMII_CRS_DV ETH_RGMII_TXD0	TIM1_CH1N_1 USART1_RX_3 UART7_RX_1 TIM10_CH3N_1
-	24	33	PC4	I/O/A	-	PC4	ADC_IN14 TIM9_CH4 UART8_TX OPA4_CH1P ETH_MII_RXD0 ETH_RMII_RXD0	USART1_CTS_3

Pin No.			Pin name	Pin type (1)	I/O level	Main function (after reset)	Default alternate function	Remapping function
LQFP48	LQFP64M	LQFP100						
							ETH_RGMII_TXD1	
-	25	34	PC5	I/O/A	-	PC5	ADC_IN15 TIM9_BKIN UART8_RX OPA3_CH1P ETH_MII_RXD1 ETH_RMII_RXD1 ETH_RGMII_TXD2	USART1_RTS_3
18	26	35	PB0	I/O/A	-	PB0	ADC_IN8 TIM3_CH3 TIM8_CH2N OPA1_CH1P ETH_MII_RXD2 ETH_RGMII_TXD3	TIM1_CH2N_1 TIM3_CH3_2 TIM9_CH1N_1 UART4_TX_1
19	27	36	PB1	I/O/A	-	PB1	ADC_IN9 TIM3_CH4 TIM8_CH3N OPA4_CH0N ETH_MII_RXD3 ETH_RGMII_125IN	TIM1_CH3N_1 TIM3_CH4_2 TIM9_CH2N_1 UART4_RX_1
20	28	37	PB2	I/O	FT	PB2/BOOT1	OPA3_CH0N	TIM9_CH3N_1
-	-	38	PE7	I/O/A	FT	PE7	FSMC_D4 OPA3_OUT1	TIM1_ETR_3
-	-	39	PE8	I/O/A	FT	PE8	FSMC_D5 OPA4_OUT1	TIM1_CH1N_3 UART5_TX_2
-	-	40	PE9	I/O	FT	PE9	FSMC_D6	TIM1_CH1_3 UART5_RX_2
-	-	41	PE10	I/O	FT	PE10	FSMC_D7	TIM1_CH2N_3 UART6_TX_2
-	-	42	PE11	I/O	FT	PE11	FSMC_D8	TIM1_CH2_3 UART6_RX_2
-	-	43	PE12	I/O	FT	PE12	FSMC_D9	TIM1_CH3N_3 UART7_TX_2
-	-	44	PE13	I/O	FT	PE13	FSMC_D10	TIM1_CH3_3 UART7_RX_2
-	-	45	PE14	I/O/A	FT	PE14	FSMC_D11 OPA2_OUT1	TIM1_CH4_3 UART8_TX_2
-	-	46	PE15	I/O/A	FT	PE15	FSMC_D12 OPA1_OUT1	TIM1_BKIN_3 UART8_RX_2

Pin No.			Pin name	Pin type (1)	I/O level	Main function (after reset)	Default alternate function	Remapping function
LQFP48	LQFP64M	LQFP100						
21	29	47	PB10	I/O/A	FT	PB10	I²C2_SCL USART3_TX OPA2_CH0N ETH_MII_RX_ER	TIM2_CH3_2 TIM2_CH3_3 TIM10_BKIN_1
22	30	48	PB11	I/O/A	FT	PB11	I²C2_SDA USART3_RX OPA1_CH0N ETH_MII_TX_EN ETH_RMII_TX_EN	TIM2_CH4_2 TIM2_CH4_3 TIM10_ETR_1
23	31	49	V_{SS_1}	P		V_{SS_1}		
-	32	50	V_{I/O_1}	P		V_{I/O_1}		
24	-	-	V_{DD_I/O_1}	P		V_{DD_I/O_1}		
25	33	51	PB12	I/O/A	FT	PB12	SPI2_NSS I²S2_WS I²C2_SMBA USART3_CK TIM1_BKIN OPA4_CH0P CAN2_RX ETH_MII_TXD0 ETH_RMII_TXD0	
26	34	52	PB13	I/O/A	FT	PB13	SPI2_SCK I²S2_CK USART3_CTS TIM1_CH1N OPA3_CH0P CAN2_TX ETH_MII_TXD1 ETH_RMII_TXD1	USART3_CTS_1
27	35	53	PB14	I/O/A	FT	PB14	SPI2_MISO TIM1_CH2N USART3_RTS OPA2_CH0P	USART3_RTS_1
28	36	54	PB15	I/O/A	FT	PB15	SPI2_MOSI/I²S2_SD TIM1_CH3N/OPA1_CH0P	USART1_TX_2
-	-	55	PD8	I/O	FT	PD8	FSMC_D13	USART3_TX_3 TIM9_CH1N_2 ETH_MII_RX_DV ETH_RMII_CRS_D

Pin No.			Pin name	Pin type (1)	I/O level	Main function (after reset)	Default alternate function	Remapping function
LQFP48	LQFP64M	LQFP100						
								V
-	-	56	PD9	I/O	FT	PD9	FSMC_D14	USART3_RX_3 TIM9_CH1_ETR_2 ETH_MII_RXD0 ETH_RMII_RXD0
-	-	57	PD10	I/O	FT	PD10	FSMC_D15	USART3_CK_3 TIM9_CH2N_2 ETH_MII_RXD1 ETH_RMII_RXD1
-	-	58	PD11	I/O	FT	PD11	FSMC_A16	USART3_CTS_3 TIM9_CH2_2 ETH_MII_RXD2
-	-	59	PD12	I/O	FT	PD12	FSMC_A17	TIM4_CH1_1 TIM9_CH3N_2 USART3_RTS_3 ETH_MII_RXD3
-	-	60	PD13	I/O	FT	PD13	FSMC_A18	TIM4_CH2_1 TIM9_CH3_2
-	-	61	PD14	I/O	FT	PD14	FSMC_D0	TIM4_CH3_1 TIM9_BKIN_2
-	-	62	PD15	I/O	FT	PD15	FSMC_D1	TIM4_CH4_1 TIM9_CH4_2
-	37	63	PC6	I/O	FT	PC6	I^2S2_MCK TIM8_CH1 SDIO_D6 ETH_RXP	TIM3_CH1_3
-	38	64	PC7	I/O	FT	PC7	I^2S3_MCK TIM8_CH2 SDIO_D7 ETH_RXN	TIM3_CH2_3
-	39	65	PC8	I/O	FT	PC8	TIM8_CH3 SDIO_D0 ETH_TXP DVP_D2	TIM3_CH3_3
-	40	66	PC9	I/O	FT	PC9	TIM8_CH4 SDIO_D1 ETH_TXN DVP_D3	TIM3_CH4_3
29	41	67	PA8	I/O	FT	PA8	USART1_CK TIM1_CH1	USART1_CK_1 USART1_RX_2

Pin No.			Pin name	Pin type (1)	I/O level	Main function (after reset)	Default alternate function	Remapping function
LQFP48	LQFP64M	LQFP100						
							MCO	TIM1_CH1_1
30	42	68	PA9	I/O	FT	PA9	USART1_TX TIM1_CH2 OTG_FS_VBUS DVP_D0	USART1_RTS_2 TIM1_CH2_1
31	43	69	PA10	I/O	FT	PA10	USART1_RX TIM1_CH3 OTG_FS_ID DVP_D1	USART1_CK_2 TIM1_CH3_1
32	44	70	PA11	I/O/A	FT	PA11	USART1_CTS USBDM CAN1_RX TIM1_CH4 OTG_FS_DM	USART1_CTS_1 TIM1_CH4_1
33	45	71	PA12	I/O/A	FT	PA12	USART1_RTS USBDP CAN1_TX TIM1_ETR TIM10_CH1N OTG_FS_DP	USART1_RTS_1 TIM1_ETR_1
34	46	72	PA13	I/O	FT	SWDIO	TIM10_CH2N	PA13 TIM8_CH1N_1
-	-	73	未使用					
35	47	74	V_{SS_2}	P	-	V_{SS_2}		
36	48	75	V_{DD_2}	P	-	V_{DD_2}		
37	49	76	PA14	I/O	FT	SWCLK	TIM10_CH3N	TIM8_CH2N_1 UART8_TX_1 PA14
38	50	77	PA15	I/O	FT	PA15	SPI3_NSS I^2S3_WS	TIM2_CH1_ETR_1 TIM2_CH1_ETR_3 SPI1_NSS TIM8_CH3N_1 UART8_RX_1
-	51	78	PC10	I/O	FT	PC10	UART4_TX SDIO_D2 TIM10_ETR DVP_D8	USART3_TX_1 SPI3_SCK I^2S3_CK
-	52	79	PC11	I/O	FT	PC11	UART4_RX SDIO_D3 TIM10_CH4	USART3_RX_1 SPI3_MISO

Pin No.			Pin name	Pin type (1)	I/O level	Main function (after reset)	Default alternate function	Remapping function
LQFP48	LQFP64M	LQFP100						
							DVP_D4	
-	53	80	PC12	I/O	FT	PC12	UART5_TX SDIO_CK TIM10_BKIN DVP_D9	USART3_CK_1 SPI3_MOSI I²S3_SD
-	-	81	PD0	I/O/A	FT	PD0	FSMC_D2	CAN1_RX TIM10_ETR_2
-	-	82	PD1	I/O/A	FT	PD1	FSMC_D3	CAN1_TX TIM10_CH1_2
-	54	83	PD2	I/O	FT	PD2	TIM3_ETR UART5_RX SDIO_CMD DVP_D11	TIM3_ETR_2 TIM3_ETR_3
-	-	84	PD3	I/O	FT	PD3	FSMC_CLK	USART2_CTS_1 TIM10_CH2_2
-	-	85	PD4	I/O	FT	PD4	FSMC_NOE	USART2_RTS_1
-	-	86	PD5	I/O	FT	PD5	FSMC_NWE	USART2_TX_1 TIM10_CH3_2
-	-	87	PD6	I/O	FT	PD6	FSMC_NWAIT DVP_D10	USART2_RX_1
-	-	88	PD7	I/O	FT	PD7	FSMC_NE1 FSMC_NCE2	USART2_CK_1 TIM10_CH4_2
39	55	89	PB3	I/O	FT	PB3	SPI3_SCK I²S3_CK	TRACESWO TIM2_CH2_1 TIM2_CH2_3 SPI1_SCK TIM10_CH1_1
40	56	90	PB4	I/O	FT	PB4	SPI3_MISO	TIM3_CH1_2 SPI1_MISO UART5_TX_1 TIM10_CH2_1
41	57	91	PB5	I/O	-	PB5	I²C1_SMBA SPI3_MOSI I²S3_SD ETH_MII_PPS_OUT ETH_RMII_PPS_OUT	TIM3_CH2_2 SPI1_MOSI CAN2_RX TIM10_CH3_1 UART5_RX_1
42	58	92	PB6	I/O	FT	PB6	I²C1_SCL TIM4_CH1 USBFS_DM DVP_D5	USART1_TX_1 CAN2_TX TIM8_CH1_1

Pin No.			Pin name	Pin type (1)	I/O level	Main function (after reset)	Default alternate function	Remapping function
LQFP48	LQFP64M	LQFP100						
							USBHS_DM	
43	59	93	PB7	I/O	FT	PB7	I²C1_SDA FSMC_NADV TIM4_CH2 USBFS_DP USBHS_DP	USART1_RX_1 TIM8_CH2_1
44	60	94	BOOT0	I	-	BOOT0		
45	61	95	PB8	I/O/A	FT	PB8	TIM4_CH3 SDIO_D4 TIM10_CH1 DVP_D6 ETH_MII_TXD3	I²C1_SCL CAN1_RX UART6_TX_1 TIM8_CH3_1
46	62	96	PB9	I/O/A	FT	PB9	TIM4_CH4 SDIO_D5 TIM10_CH2 DVP_D7	I²C1_SDA CAN1_TX UART6_RX_1 TIM8_BKIN_1
-	-	97	PE0	I/O	FT	PE0	TIM4_ETR FSMC_NBL0	TIM4_ETR_1 UART4_TX_2
-	-	98	PE1	I/O	FT	PE1	FSMC_NBL1	UART4_RX_2
47	63	99	V_{SS_3}	P	-	V_{SS_3}		
	64	100	V_{I/O_3}	P	-	V_{I/O_3}		
48	-	-	V_{DD_I/O_3}	P		V_{DD_I/O_3}		

Note 1: Abbreviations in the table

I = TTL/CMOS Schmitt input;

O = CMOS tri-state output;

A = analog signal input or output;

P = power;

FT = 5V tolerance;

ANT = RF signal input and output (antenna);

Note 2: The PC13, PC14 and PC15 pins are powered by the power's switch, and this power's switch can only absorb a limited current (3mA). Therefore, when these 3 pins are used as output pins, there are the following restrictions: only one pin can be used as an output at the same time. When used as an output pin, it can only work in 2MHz mode. The maximum drive load is 30pF and cannot be used as a current source (Such as driving LED).

Note 3: These pins are in the main function state when the backup area is powered on for the first time. Even after reset, the state of these pins is controlled by the backup area registers (these registers will not be reset

by the main reset system). For specific information on how to control these I/O ports, please refer to the relevant chapters on the battery backup area and BKP register in the CH32xRM datasheet.

Note 4: Pin 5 and pin 6 of those in LQFP64M package are configured as OSC_IN and OSC_OUT function pins by default after chip reset. Software can reconfigure these 2 pins as PD0 and PD1. But for those in LQFP100 package, since PD0 and PD1 are inherent functional pins, there is no need to re-image settings by software. For more detailed information, please refer to the chapters on Alternate Function I/O and Debug Setting in the CH32xRM datasheet.

Note 5: For devices without the BOOT0 pinout, they are pulled down to GND internally. For devices with the BOOT0 pinout but no BOOT1/PB2 pinout, BOOT1/PB2 is pulled down to GND internally. At this time, if you enter the low-power mode to configure the I/O port state, it is recommended that the BOOT1/PB2 pins use the input pull-down mode to prevent additional current generation.

3.3 Pin alternate functions

Note: The pin function descriptions in the table below are for all functions and do not relate to specific model products. Peripheral resources may vary between models, so please check the availability of this function according to the product model resource table before viewing.

Table 3-2 CH32F203xB/xC_205_207xx pin alternate functions

Alternate / Pins	ADC DAC	TIM1 8/9/10	TIM2 3/4/5	UART USART	USB	SYS	I²C	SPI I²S	ETH	FSMC SDIO	DVP	OPA	CAN
PA0	ADC_IN0	TIM8_ETR TIM8_ETR_1	TIM2_CH1_ETR TIM2_CH1_ETR_2 TIM5_CH1	USART2_CTS		WKUP			ETH_MII_CRS_WKUP ETH_RGMII_RXD2			0PA4_OUT0	
PA1	ADC_1N1		TIM2_CH2 TIM2_CH2_2 TIM5_CH2 TIM9_BKIN_1	USART2_RTS					ETH_MII_RX_CLK ETH_RMII_REF_CLK ETH_RGMII_RXD3			OPA3_OUT0	
PA2	ADC_IN2	TIM9_CH1 TIM9_ETR TIM9_CH1_ETR_1	TIM2_CH3 TIM2_CH3_1 TIM5_CH3	USART2_TX					ETH_MII_MDI0 ETH_RMII_MDI0 ETH_RGMII_GTXC			OPA2_OUT0	
PA3	ADC_IN3	TIM9_CH2 TIM9_CH2_1	TIM2_CH4 TIM2_CH4_1 TIM5_CH4	USART2_RX					ETH_MII_COL ETH_RGMII_TXEN			OPA1_OUT0	
PA4	ADC_IN4 DAC_OUT1	TIM9_CH3 TIM9_CH3_1		USART2_CK				SPI1_NSS SPI3_NSS I²S3_WS			DVP_HSYNC		
PA5	ADC_IN5 DAC_OUT2	TIM10_CH1N_1		USART1_CTS_2 USART1_CK_3				SPI1_SCK			DVP_VSYNC	OPA2_CH1N	
PA6	ADC_IN6	TIM1_BKIN_1 TIM8_BKIN TIM10_CH2N_1	TIM3_CH1	USART1_TX_3 UART7_TX_1				SPI1_MISO			DVP_PCLK	OPA1_CH1N	
PA7	ADC_IN7	TIM1_CH1N_1 TIM8_CH1N TIM10_CH3N_1	TIM3_CH2	USART1_RX_3 UART7_RX_1				SPI1_MOSI	ETH_MII_RX_DV ETH_RMII_CRS_DV ETH_RGMII_TXD0			OPA2_CH1P	
PA8		TIM1_CH1 TIM1_CH1_1		USART1_CK USART1_CK_1 USART1_RX_2		MCO							
PA9		TIM1_CH2 TIM1_CH2_1		USART1_TX USART1_RTS_2	OTG_FS_VBUS						DVP_D0		
PA10		TIM1_CH3 TIM1_CH3_1		USART1_RX USART1_CK_2	OTG_FS_ID						DVP_D1		
PA11		TIM1_CH4 TIM1_CH4_1		USART1_CTS USART1_CTS_1	OTG_FS_DM USBDM								CAN1_RX
PA12		TIM1_ETR TIM1_ETR_1 TIM10_CH1N		USART1_RTS USART1_RTS_1	OTG_FS_DP USBDP								CAN1_TX
PA13		TIM8_CHIN_1 TIM10_CH2N				SWDIO							
PA14		TIM8_CH2N_1 TIM10_CH3N		UART8_TX_1		SWCLK							
PA15		TIM8_CH3N_1	TIM2_CH1_ETR_1 TIM2_CH1_ETR_3	UART8_RX_1				SPI1_NSS SPI3_NSS I²S3_WS					
PB0	ADC_ IN8	TIM1_CH2N_1 TIM8_CH2N TIM9_CH1N_1	TIM3_CH3 TIM3_CH3_2	UART4_TX_1					ETH_ MII_RXD2 ETH_RGMII_TXD3			OPA1_CH1P	
PB1	ADC_IN9	TIM1_CH3N_1 TIM8_CH3N TIM9_CH2N_1	TIM3_CH4 TIM3_CH4_2	UART4_RX_1					ETH_MII_RXD3 ETH_RGMII_125IN			OPA4_CH0N	
PB2		TIM9_CH3N_1				BOOT1						OPA3_CH0N	
PB3		TIM10_CH1_1	TIM2_CH2_1 TIM2_CH2_3					SPI1_SCK SPI3_SCK I²S3_CK					

Alternate Pins	ADC DAC	TIM1 8/9/10	TIM2 3/4/5	UART USART	USB	SYS	I²C	SPI I²S	ETH	FSMC SDIO	DVP	OPA	CAN
PB4		TIM10_CH2_1	TIM3_CH1_2	UART5_TX_1				SPI1_MISO SPI3_MISO					
PB5		TIM10_CH3_1	TIM3_CH2_2	UART5_RX_1			I²C1_SMBA	SPI1_MOSI SPI3_MOSI I²S3_SD	ETH_MII_PPS_OUT ETH_RMII_PPS_OUT				CAN2_RX
PB6		TIM8_CHI_1	TIM4_CH1	USART1_TX_1	USBFS_DM USBHS_DM		I²C1_SCL				DVP_D5		CAN2_TX
PB7		TIM8_CH2_1	TIM4_CH2	USART1_RX_1	USBFS_DP USBHS_DP		I²C1_SDA			FSMC_NADV			
PB8		TIM8_CH3_1 TIM10_CH1	TIM4_CH3	UART6_TX_1			I²C1_SCL		ETH_ MII_TXD3	SDIO_D4	DVP_D6		CAN1_RX
PB9		TIM8_BKIN_1 TIM10_CH2	TIM4_CH4	UART6_RX_1			I²C1_SDA			SDIO_D5	DVP_D7		CAN1_TX
PB10		TIM10_BKIN_1	TIM2_CH3_2 TIM2_CH3_3	USART3_TX			I²C2_SCL		ETH_ MII_RX_ER			OPA2_CH0N	
PB11		TIM10_ETR_1	TIM2_CH4_2 TIM2_CH4_3	USART3_RX			I²C2_SDA		ETH_MII_TX_EN ETH_RMII_TX_EN			OPA1_CH0N	
PB12		TIM1_BKIN		USART3_CK			I²C2_SMBA	SPI2_NSS I²S2_WS	ETH_MII_TXD0 ETH_RMII_TXD0			OPA4_CH0P	CAN2_RX
PB13		TIM1_CH1N		USART3_CTS USART3_CTS_1				SPI2_SCK I²S2_CK	ETH_MII_TXD1 ETH_RMII_TXD1			OPA3_CH0P	CAN2_TX
PB14		TIM1_CH2N		USART3_RTS USART3_RTS_1				SPI2_MISO				OPA2_CH0P	
PB15		TIM1_CH3N		USART1_TX_2				SPI2_MOSI I²S2_SD				OPA1_CH0P	
PC0	ADC_IN10	TIM9_CH1N		UART6_TX					ETH_RGMII_RXC				
PC1	ADC_IN11	TIM9_CH2N		UART6_RX					ETH_MII_MDC ETH_RMII_MDC ETH_RGMII_RXCTL				
PC2	ADC_IN12	TIM9_CH3N		UART7_TX					ETH_MII_TXD2 ETH_RGMII_RXD0			OPA3_CH1N	
PC3	ADC_IN13	TIM10_CH3		UART7_RX					ETH_MII_TX_CLK ETH_RGMII_RXD1			OPA4_CH1N	
PC4	ADC_IN14	TIM9_CH4		USART1_CTS_3 UART8_TX					ETH_MII_RXD0 ETH_RMII_RXDO ETH_RGMII_TXD1			OPA4_CH1P	
PC5	ADC_IN15	TIM9_BKIN		USART1_RTS_3 UART8_RX					ETH_MII_RXD1 ETH_RMII_RXD1 ETH_RGMII_TXD2			OPA3_CH1P	
PC6		TIM8_CH1	TIM3_CH1_3					I²S2_MCK	ETH_RXP	SDIO_D6			
PC7		TIM8_CH2	TIM3_CH2_3					I²S3_MCK	ETH_RXN	SDIO_D7			
PC8		TIM8_CH3	TIM3_CH3_3						ETH_TXP	SDIO_D0	DVP_D2		
PC9		TIM8_CH4	TIM3_CH4_3						ETH_TXN	SDIO_D1	DVP_D3		
PC10		TIM10_ETR		USART3_TX_1 UART4_TX				SPI3_SCK I²S3_CK		SDIO_D2	DVP_D8		
PC11		TIM10_CH4		USART3_RX_1 UART4_RX				SPI3_MISO		SDIO_D3	DVP_D4		
PC12		TIM10_BKIN		USART3_CK_1 UART5_TX				SPI3_MOSI I²S3_SD		SDIO_CK	DVP_D9		
PC13		TIM8_CH4_1				TAMPER-RTC							
PC14		TIM9_CH4_1				OSC32_IN							
PC15		TIM10_CH4_1				OSC32_OUT							
PD0		TIM10_ETR_2				OSC_IN				FSMC_D2			CAN1_RX
PD1		TIM10_CH1_2				OSC_OUT				FSMC_D3			CAN1_TX
PD2			TIM3_ETR TIM3_ETR_2 TIM3_ETR_3	UART5_RX						SDIO_CMD	DVP_D11		

Alternate Pins	ADC DAC	TIM1 8/9/10	TIM2 3/4/5	UART USART	USB	SYS	I²C	SPI I²S	ETH	FSMC SDIO	DVP	OPA	CAN
PD3		TIM10_CH2_2		USART2_CTS_1						FSMC_CLK			
PD4				USART2_RTS_1						FSMC_NOE			
PD5		TIM10_CH3_2		USART2_TX_1						FSMC_NWE			
PD6				USART2_RX_1						FSMC_NWAIT	DVP_D10		
PD7		TIM10_CH4_2		USART2_CK_1						FSMC_NE1 FSMC_NCE2			
PD8		TIM9_CH1N_2		USART3_TX_3					ETH_MII_RX_DV ETH_RMII_CRS_DV	FSMC_D13			
PD9		TIM9_CH1_ETR_2		USART3_RX_3					ETH_MII_RXD0 ETH_RMII_RXD0	FSMC_D14			
PD10		TIM9_CH2N_2		USART3_CK_3					ETH_MII_RXD1 ETH_RMII_RXD1	FSMC_D15			
PD11		TIM9_CH2_2		USART3_CTS_3					ETH_MII_RXD2	FSMC_A16			
PD12		TIM9_CH3N_2	TIM4_CH1_1	USART3_RTS_3					ETH_MII_RXD3	FSMC_A17			
PD13		TIM9_CH3_2	TIM4_CH2_1							FSMC_A18			
PD14		TIM9_BKIN_2	TIM4_CH3_1							FSMC_D0			
PD15		TIM9_CH4_2	TIM4_CH4_1							FSMC_D1			
PE0			TIM4_ETR TIM4_ETR_1	UART4_TX_2						FSMC_NBL0			
PE1				UART4_RX_2						FSMC_NBL1			
PE2		TIM10_BKIN_2								FSMC_A23			
PE3		TIM10_CH1N_2								FSMC_A19			
PE4		TIM10_CH2N_2								FSMC_A20			
PE5		TIM10_CH3N_2								FSMC_A21			
PE6										FSMC_A22			
PE7		TIM1_ETR_3								FSMC_D4		OPA3_OUT1	
PE8		TIM1_CH1N_3		UART5_TX_2						FSMC_D5		OPA4_OUT1	
PE9		TIM1_CH1_3		UART5_RX_2						FSMC_D6			
PE10		TIM1_CH2N_3		UART6_TX_2						FSMC_D7			
PE11		TIM1_CH2_3		UART6_RX_2						FSMC_D8			
PE12		TIM1_CH3N_3		UART7_TX_2						FSMC_D9			
PE13		TIM1_CH3_3		UART7_RX_2						FSMC_D10			
PE14		TIM1_CH4_3		UART8_TX_2						FSMC_D11		OPA2_OUT1	
PE15		TIM1_BKIN_3		UART8_RX_2						FSMC_D12		OPA1_OUT1	

Chapter 4 Electrical characteristics

4.1 Test conditions

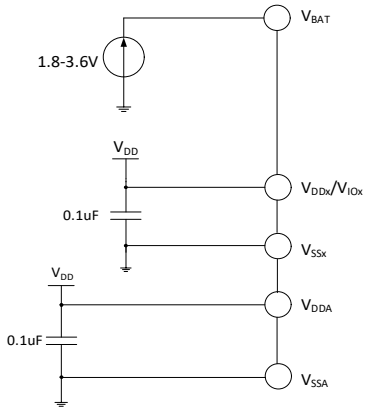
Unless otherwise specified and marked, all voltages are referenced to V_{SS}.

All minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and clock frequency. Typical values are based on normal temperature (25℃) and V_{DD} = 3.3V environment, which are given only as design guidelines.

The data based on comprehensive evaluation, design simulation or technology characteristics are not tested in production. On the basis of comprehensive evaluation, the minimum and maximum values refer to sample tests. Unless otherwise specified that is tested, the characteristic parameters are guaranteed by comprehensive evaluation or design.

Power supply scheme:

Figure 4-1 Typical circuit for conventional power supply



4.2 Absolute maximum ratings

Stresses at or above the absolute maximum ratings listed in the table below may cause permanent damage to the device.

Table 4-1 Absolute maximum ratings

Symbol	Description	Min.	Max.	Unit
T_A	Ambient temperature during operation	-40	85	℃
T_S	Ambient temperature during storage	-40	125	℃
V_{DD}-V_{SS}	External main supply voltage (includingV_{DDA} and V_{DD})	-0.3	4.0	V
V_{IO}-V_{SS}	I/O domain supply voltage	-0.3	4.0	V
V_{IN}	Input voltage on the FT (5V tolerance) pin	V_{SS}-0.3	5.5	V
	Input voltage on other pins	V_{SS}-0.3	V_{DD}+0.3	
$\|\triangle V_{DD\_x}\|$	Variations between different main power supply pins		50	mV
$\|\triangle V_{IO\_x}\|$	Variations between different I/O power supply pins		50	mV

$\|\triangle V_{SS\_x}\|$	Variations between different ground pins		50	mV
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model, non-contact)	4K		V
	USB pins (PA11, PA12)	3K		V
I_{VDD}	Total current into $V_{DD}/V_{DDA}/V_{I/O}$ power lines (supply current)		150	mA
I_{Vss}	Total current out of V_{SS} ground lines (outflow current)		150	
$I_{I/O}$	Sink current on any I/O and control pin		25	
	Output current on any I/O and control pin		-25	
$I_{INJ(PIN)}$	Injected current on NRST pin		+/-5	
	Injected current on HSE's OSC_IN pin and LSE's OSC_IN pin		+/-5	
	Injected current on other pins		+/-5	
$\sum I_{INJ(PIN)}$	Total injected current on all I/Os and control pins		+/-25	

4.3 Electrical characteristics

4.3.1 Operating conditions

Table 4-2 General operating conditions

Symbol	Parameter	Condition	Min.	Max.	Unit
F_{HCLK}	Internal AHB clock frequency			144	MHz
F_{PCLK1}	Internal APB1 clock frequency			144	MHz
F_{PCLK2}	Internal APB2 clock frequency			144	MHz
V_{DD}	Standard operating voltage		2.4	3.6	V
		Use USB or ETH	3.0	3.6	
$V_{I/O}$	Output voltage on most I/O pins	$V_{I/O}$ cannot be more than V_{DD}	2.4	3.6	V
V_{DDA}	Analog operating voltage (ADC is not used)	V_{DDA} must be the same as $V_{I/O}$, V_{REF+} cannot be higher than V_{DDA}, V_{REF-} is equal to V_{SS}.	2.4	3.6	V
	Analog operating voltage (ADC is used)				
V_{BAT}(1)	Backup operating voltage	Cannot be more than V_{DD}	1.8	3.6	V
T_A	Ambient temperature		-40	85	℃
T_J	Junction temperature range		-40	85	℃

Note: 1. The connection line from the battery to V_{BAT} should be as short as possible.

Table 4-3 Power-on and power-down conditions

Symbol	Parameter	Condition	Min.	Max.	Unit
t_{VDD}	V_{DD} rise time rate		0	∞	us/V
	V_{DD} fall time rate		30	∞	

4.3.2 Embedded reset and power control block characteristics

Table 4-4 Reset and voltage monitor (For PDR, select high threshold gear)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit

V_{PVD}(1)	Programmable voltage detector level selection	PLS[2:0] = 000 (rising edge)		2.39		V
		PLS[2:0] = 000 (falling edge)		2.31		V
		PLS[2:0] = 001 (rising edge)		2.56		V
		PLS[2:0] = 001 (falling edge)		2.48		V
		PLS[2:0] = 010 (rising edge)		2.65		V
		PLS[2:0] = 010 (falling edge)		2.57		V
		PLS[2:0] = 011 (rising edge)		2.78		V
		PLS[2:0] = 011 (falling edge)		2.69		V
		PLS[2:0] = 100 (rising edge)		2.89		V
		PLS[2:0] = 100 (falling edge)		2.81		V
		PLS[2:0] = 101 (rising edge)		3.05		V
		PLS[2:0] = 101 (falling edge)		2.96		V
		PLS[2:0] = 110 (rising edge)		3.17		V
		PLS[2:0] = 110 (falling edge)		3.08		V
		PLS[2:0] = 111 (rising edge)		3.31		V
		PLS[2:0] = 111 (falling edge)		3.21		V
$V_{PVDhyst}$	PVD hysteresis			0.08		V
$V_{POR/PDR}$	Power-on/power-down reset threshold	Rising edge	1.9	2.2	2.4	V
		Falling edge	1.9	2.2	2.4	V
$V_{PDRhyst}$	PDR hysteresis			20		mV
$t_{RSTTEMPO}$	Power on reset		24	28	30	mS
	Other resets		8	10	30	

Note: 1. Normal temperature test value.

4.3.3 Embedded reference voltage

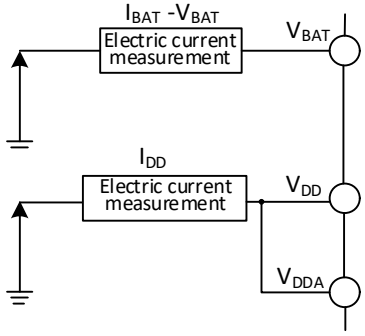
Table 4-5 Embedded reference voltage

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{REFINT}	Internal reference voltage	T_A = -40°C~85°C	1.17	1.2	1.23	V
$T_{S\_vrefint}$	ADC sampling time when reading the internal reference voltage				17.1	us

4.3.4 Supply current characteristics

Current consumption is a comprehensive index of a variety of parameters and factors. These parameters and factors include operating voltage, ambient temperature, I/O pin load, the software configuration of the product, the operating frequency, flip rate of the I/O pin, the location of the program in memory and the executed code, etc. The current consumption measurement method is as follows:

Figure 4-2 Current consumption measurement



The microcontroller is in the following conditions:
Under normal temperature conditions and when V_{DD} = 3.3V, all I/O ports are configured with pull-up inputs, only one of HSE and HIS is enabled, HSE=8M, HIS=8M (calibrated), F_{PLCK1}=F_{HCLK}, F_{PLCK2}=F_{HCLK}, PLL is enabled when FHCLK>8MHz. Enable or disable the power consumption of all peripheral clocks.

Table 4-6-1 Typical current consumption in Run mode, the data processing code runs from the internal Flash (For CH32F207)

Symbol	Parameter	Condition		Typ.		Unit
				All peripherals enabled	All peripherals disabled(2)	
I_{DD}(1)	Supply current in Run mode	External clock	F_{HCLK} = 144MHz	25.97	14.68	mA
			F_{HCLK} = 72MHz	13.34	7.71	
			F_{HCLK} = 48MHz	9.15	5.40	
			F_{HCLK} = 36MHz	6.98	4.28	
			F_{HCLK} = 24MHz	4.97	3.09	
			F_{HCLK} = 16MHz	3.86	2.51	
			F_{HCLK} = 8MHz	2.26	1.44	
			F_{HCLK} = 4MHz	1.38	1.07	
			F_{HCLK} = 500KHz	0.79	0.74	
		Runs on the high-speed internal RC oscillator (HSI). Uses AHB prescaler to reduce the frequency.	F_{HCLK} = 144MHz	25.54	14.61	
			F_{HCLK} = 72MHz	13.11	9.46	
			F_{HCLK} = 48MHz	8.98	6.54	
			F_{HCLK} = 36MHz	7.19	4.25	
			F_{HCLK} = 24MHz	4.84	3.63	
			F_{HCLK} = 16MHz	3.59	2.82	
			F_{HCLK} = 8MHz	1.97	1.35	
			F_{HCLK} = 4MHz	1.31	0.99	
			F_{HCLK} = 500KHz	0.72	0.67	

Note: The above are the actual measured parameters of similar chips, the actual value will be slightly deviated.

Table 4-6-2 Typical current consumption in Run mode, the data processing code runs from the internal Flash (For CH32F203 high capacity)

Symbol	Parameter	Condition		Typ.		Unit
				All peripherals enabled	All peripherals disabled(2)	
I_{DD}(1)	Supply current in Run mode	External clock	F_{HCLK}= 144MHz	23.61	14.59	mA
			F_{HCLK} = 72MHz	12.15	7.64	
			F_{HCLK} = 48MHz	8.35	5.34	
			F_{HCLK} = 36MHz	7.24	4.69	
			F_{HCLK} = 24MHz	4.55	3.05	
			F_{HCLK} = 16MHz	3.61	2.47	
			F_{HCLK} = 8MHz	1.88	1.38	
			F_{HCLK} = 4MHz	1.29	1.04	
			F_{HCLK}= 500KHz	0.76	0.71	
		Runs on the high-speed internal RC oscillator (HSI). Uses AHB prescaler to reduce the frequency.	F_{HCLK}= 144MHz	23.19	14.12	
			F_{HCLK} = 72MHz	11.9	7.29	
			F_{HCLK} = 48MHz	8.13	5.09	
			F_{HCLK} = 36MHz	6.45	4.07	
			F_{HCLK} = 24MHz	4.36	2.84	
			F_{HCLK} = 16MHz	3.19	2.13	
			F_{HCLK} = 8MHz	1.78	1.28	
			F_{HCLK} = 4MHz	1.12	0.86	
			F_{HCLK}= 500KHz	0.59	0.55	

Note: The above are the actual measured parameters of similar chips, the actual value will be slightly deviated.

Table 4-7-1 Typical current consumption in Sleep mode, data processing code runs from internal Flash or SRAM (For CH32F207)

Symbol	Parameter	Condition		Typ.		Unit
				All peripherals enabled	All peripherals disabled(2)	
I_{DD}(1)	Supply current in Sleep mode (In this case, peripheral power supply and clock are maintained)	External clock	F_{HCLK} = 144MHz	15.12	4.06	mA
			F_{HCLK} = 72MHz	7.92	2.39	
			F_{HCLK} = 48MHz	5.54	1.85	
			F_{HCLK} = 36MHz	4.62	1.91	
			F_{HCLK} = 24MHz	3.17	1.32	
			F_{HCLK} = 16MHz	2.68	1.32	
			F_{HCLK} = 8MHz	1.45	0.84	
			F_{HCLK} = 4MHz	1.08	0.77	
			F_{HCLK} = 500KHz	0.76	0.71	
		Runs on the high-speed internal RC oscillator (HSI).	F_{HCLK} = 144MHz	15.13	4.01	
			F_{HCLK} = 72MHz	7.89	2.32	
			F_{HCLK} = 48MHz	5.49	1.78	

		Uses AHB prescaler to reduce the frequency.	F_{HCLK} = 36MHz	4.53	1.65	
			F_{HCLK} = 24MHz	3.11	1.25	
			F_{HCLK} = 16MHz	2.40	1.13	
			F_{HCLK} = 8MHz	1.38	0.77	
			F_{HCLK} = 4MHz	1.01	0.70	
			F_{HCLK} = 500KHz	0.69	0.64	

Note: The above are the actual measured parameters of similar chips, the actual value will be slightly deviated.

Table 4-7-2 Typical current consumption in Sleep mode, data processing code runs from internal Flash or SRAM (For CH32F203 high capacity)

Symbol	Parameter	Condition		Typ.		Unit
				All peripherals enabled	All peripherals disabled(2)	
I_{DD}(1)	Supply current in Sleep mode (In this case, peripheral power supply and clock are maintained)	External clock	F_{HCLK} = 144MHz	13.16	4.15	mA
			F_{HCLK} = 72MHz	6.93	2.42	
			F_{HCLK} = 48MHz	4.86	1.86	
			F_{HCLK} = 36MHz	4.58	2.06	
			F_{HCLK} = 24MHz	2.81	1.31	
			F_{HCLK} = 16MHz	2.43	1.30	
			F_{HCLK} = 8MHz	1.31	0.82	
			F_{HCLK} = 4MHz	1.01	0.76	
			F_{HCLK} = 500KHz	0.72	0.68	
		Runs on the high-speed internal RC oscillator (HSI). Uses AHB prescaler to reduce the frequency.	F_{HCLK} = 144MHz	13.12	3.97	
			F_{HCLK} = 72MHz	6.82	2.22	
			F_{HCLK} = 48MHz	4.74	1.65	
			F_{HCLK} = 36MHz	3.94	1.52	
			F_{HCLK} = 24MHz	2.67	1.1	
			F_{HCLK} = 16MHz	2.08	0.97	
			F_{HCLK} = 8MHz	1.67	0.67	
			F_{HCLK} = 4MHz	0.85	0.60	
			F_{HCLK} = 500KHz	0.55	0.51	

Note: The above are the actual measured parameters of similar chips, the actual value will be slightly deviated.

Table 4-8 Typical current consumption in Stop and Standby mode

Symbol	Parameter	Condition	Typ.	Unit
I_{DD}	Supply current in Stop mode	Voltage regulator in Run mode, low-speed and high-speed internal RC oscillators and external oscillators off (no independent watchdog)	127	uA

		Voltage regulator in low-power mode, low-speed and high-speed internal RC oscillators and external oscillators off (no independent watchdog, PVD off), RAM enters low-power mode	41.5	
	Supply current in Standby mode	Low-speed internal RC oscillator and independent watchdog on, all RAM not powered	2.0	
		Low-speed internal RC oscillator on, independent watchdog off, all RAM not powered	2.0	
		LSI/LSE/RTC/IWDG off, 32K_RAM powered and in low-power mode	3.2	
		LSI/LSE/RTC/IWDG off, 2K_RAM powered and in low-power mode	1.5	
		LSI/LSE/RTC/IWDG off, all RAM not powered	1.27	
I_{DD_VBAT}	Backup domain supply current (Remove V_{DD} and V_{DDA}, only powered by V_{BAT}	Low-speed external oscillator and RTC on	1.9	

Note: The above are measured parameters.

4.3.5 External clock source characteristics

Table 4-9 From external high-speed clock

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{HSE_ext}	External clock frequency		3	8	25	MHz
V_{HSEH}(1)	OSC_IN input pin high level voltage		$0.8V_{I/O}$		$V_{I/O}$	V
V_{HSEL}(1)	OSC_IN input pin low-level voltage		0		$0.2V_{I/O}$	V
$C_{in(HSE)}$	OSC_IN input capacitance			5		pF
$DuCy_{(HSE)}$	Duty cycle			50		%
I_L	OSC_IN input leakage current				±1	uA

Note: 1. Failure to meet this condition may cause level recognition error.

Figure 4-3 External high-frequency clock source circuit

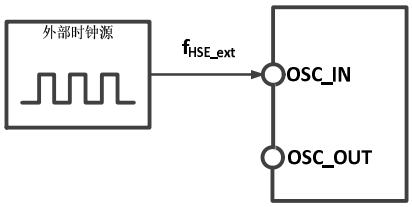


Table 4-10 From external low-speed clock

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{LSE_ext}	User external clock frequency			32.768	1000	KHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.8V_{DD}$		V_{DD}	V
V_{LSEL}	OSC32_IN input pin low voltage		0		$0.2V_{DD}$	V
$C_{in(LSE)}$	OSC32_IN input capacitance			5		pF
$DuCy_{(LSE)}$	Duty cycle			50		%
I_L	OSC32_IN input leakage current				±1	uA

Figure 4-4 External low-frequency clock source circuit

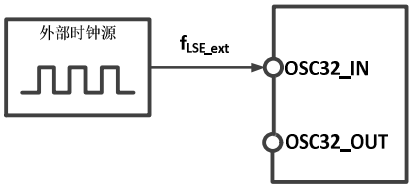


Table 4-11 High-speed external clock generated from a crystal/ceramic resonator

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{OSC_IN}	Resonator frequency		3	8	25	MHz
R_F	Feedback resistance			250		kΩ
C	Recommended load capacitance and corresponding crystal series impedance R_S	R_S=60Ω(1)		30		pF
I_2	HSE drive current	V_{DD} = 3.3V，20p load		0.53		mA
g_m	Oscillator transconductance	Startup		17.5		mA/V
$t_{SU(HSE)}$	Startup time	V_{DD} is stable, 8M crystal		2.5		ms

Note 1: It is recommended that the ESR of 25M crystal should not exceed 60 Ω, and it can be relaxed if it is lower than 25M.

Circuit reference design and requirements:

The load capacitance of the crystal is subject to the recommendation of the crystal manufacturer, C_{L1}=C_{L2}, generally C_{L1}=C_{L2}.

Figure 4-5 Typical circuit of external 8M crystal

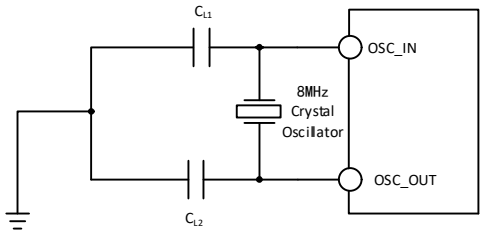


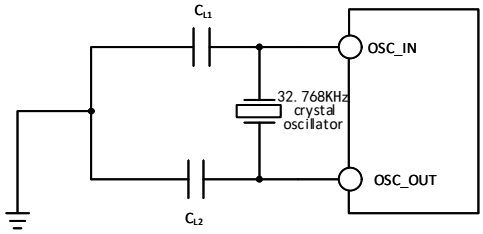
Table 4-12 Low-speed external clock generated by generated from a crystal/ceramic resonator (f(LSE)=32.768KHz)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
R_F	Feedback resistance			5		MΩ
C	Recommended load capacitance and corresponding crystal serial impedance R_S	R_S<70kΩ			15	pF
i_2	LSE drive current	VDD = 3.3V		0.35		uA
g_m	Oscillator transconductance	Startup		25.3		uA/V
$t_{SU(LSE)}$	Startup time	VDD is stable		800		mS

Circuit reference design and requirements:

The load capacitance of the crystal is subject to the recommendation of the crystal manufacturer, C_{L1}=C_{L2}, generally C_{L1}=C_{L2}.

Figure 4-6 Typical circuit of external 32.768K crystal



Note: The load capacitance C_L is calculated by the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$. C_{stray} is the capacitance of the pin and the PCB board or PCB-related capacitance. Its typical value is between 2pF and 7pF.

4.3.6 Internal clock source characteristics

Table 4-13 Internal high-speed (HSI) RC oscillator characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{HSI}	Frequency (after calibration)			8		MHz
$DuCy_{HSI}$	Duty cycle		45	50	55	%
ACC_{HSI}	Accuracy of HSI oscillator (after calibration)	TA = 0℃～70℃	-1.0		1.6	%
		TA = -40℃～85℃	-2.2		2.2	%
$t_{SU(HSI)}$	HSI oscillator startup stabilization time			10		us

$I_{DD(HSI)}$	HSI oscillator power consumption		120	180	270	uA

Table 4-14 Internal low-speed (LSI) RC oscillator characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{LSI}	Frequency		25	39	60	KHz
$DuCy_{LSI}$	Duty cycle		45	50	55	%
$t_{SU(LSI)}$	LSI oscillator startup stabilization time			100		us
$I_{DD(LSI)}$	LSI oscillator power consumption			0.6		uA

4.3.7 PLL characteristics

Table 4-15 PLL characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{PLL_IN}	PLL input clock		3	8	25	MHz
	PLL input clock duty cycle		40		60	%
F_{PLL_OUT}	PLL multiplier output clock		18		144(1)	MHz
t_{LOCK}	PLL lock time				200	us

Note 1: The frequency multiplier must be selected to meet the PLL output frequency range.

Table 4-16 PLL2 and PLL3 characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{PLL_IN}	PLL input clock		3		25	MHz
	PLL input clock duty cycle1		40		60	%
F_{PLL_OUT}	PLL multiplier output clock		30		75(1)	MHz
F_{VCO}	VCO output clock		60		150	MHz
t_{LOCK}	PLL lock time				200	us

4.3.8 Wakeup time from low-power mode

Table 4-17 Wakeup time from low-power mode(1)

Symbol	Parameter	Condition	Typ.	Unit
$t_{wusleep}$	Wakeup from Sleep mode	Wake up using HSI RC clock	2.4	us
t_{wustop}	Wakeup from Stop mode (voltage regulator is in Run mode)	Wake on HSI RC clock	23.1	us
	Wakeup from Stop mode (voltage regulator is in low-power mode)	Voltage regulator wakeup time from low-power mode + HSI RC clock wake up	76.7	us
$t_{WUSTDBY}$	Wakeup from Standby mode	LDO stabilization time + HSI RC clock wake up + code load time(2) (take 128K as example)	8.9	ms

Note: 1. The above parameters are measured parameters.

2. The code load time is calculated based on the current zero-wait area capacity configured by the chip

and the size of the loading configuration clock.

4.3.9 Memory characteristics

Table 4-18 Flash memory characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{prog}	Programming frequency(1)	T_A = -40℃～85℃			60	MHz
t_{prog_page}	Page (256 bytes) programming time	T_A = -40℃～85℃		2		ms
t_{erase_page}	Page (256 bytes) erase time	T_A = -40℃～85℃		16		ms
t_{erase_sec}	Sector (4K bytes) erase time	T_A = -40℃～85℃		16		ms
V_{prog}	Programming voltage		2.4		3.6	V

Note: 1. For the programming frequency of flash, read operation, program operation and erase operation are included. The clock is from HCLK.

Table 4-19 Flash memory endurance and data retention

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
N_{END}	Endurance	T_A = 25℃	10K	80K(1)		times
t_{RET}	Data retention		20			year

Note: The endurance parameter is actual measured, which is not guaranteed.

4.3.10 I/O port characteristics

Table 4-20 General-purpose I/O static characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	Standard I/O pin, input high level voltage		0.41*(V_{DD}-1.8)+1.3		V_{DD}+0.3	V
	FT I/O pin, input high level voltage		0.42*(V_{DD}-1.8)+1		5.5	V
V_{IL}	Standard I/O pin, input low-level voltage		-0.3		0.28*(V_{DD}-1.8)+0.6	V
	FT I/O pin, input low-level voltage		-0.3		0.32*(V_{DD}-1.8)+0.55	V
V_{hys}	Standard I/O pin Schmitt trigger voltage hysteresis		150			mV
	FT I/O pin Schmitt trigger voltage hysteresis		90			
I_{lkg}	Input leakage current	Standard I/O port			1	uA
		FT I/O port			3	
R_{PU}	Weak pull-up equivalent resistance		30	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistance		30	40	55	kΩ
$C_{I/O}$	I/O pin capacitance			5		pF

Output drive current characteristics

GPIO (General-Purpose Input/Output Port) can sink or output up to ±8mA current, and sink or output ±20mA current (not strictly to V_{OL}/V_{OH}). In user applications, the total driving current of all I/O pins cannot exceed the absolute maximum ratings given in Section 4.2:

Table 4-21 Output voltage characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{OL}	Output low level when 8 pins are sunk	TTL port, $I_{I/O}$ = +8mA		0.4	V
V_{OH}	Output high level when 8 pins are sourced	2.7V< V_{DD} <3.6V	V_{DD}-0.4		
V_{OL}	Output low level when 8 pins are sunk	CMOS port, $I_{I/O}$ = +8mA		0.4	V
V_{OH}	Output high level when 8 pins are sourced	2.7V< V_{DD} <3.6V	2.3		
V_{OL}	Output low level when 8 pins are sunk	$I_{I/O}$ = +20mA		1.3	V
V_{OH}	Output high level when 8 pins are sourced	2.7V< V_{DD} <3.6V	V_{DD}-1.3		
V_{OL}	Output low level when 8 pins are sunk	$I_{I/O}$ = +6mA		0.4	V
V_{OH}	Output high level when 8 pins are sourced	2.4V< V_{DD} <2.7V	V_{DD}-1.3		

Note: In the above conditions, if multiple I/O pins are driven at the same time, the total current cannot exceed the absolute maximum ratings given in Table 4.2. In addition, when multiple I/O pins are driven at the same time, the current on the power/ground point is very large, which will cause the voltage drop to make the internal I/O voltage not reach the power supply voltage in the table, resulting in the drive current being less than the nominal value.

Table 4-22 Input/output AC characteristics

MODEx[1:0] configuration	Symbol	Parameter	Condition	Min.	Max.	Unit
10 （2MHz）	$F_{max(IO)out}$	Maximum frequency	CL=50pF,V_{DD}=2.7-3.6V		2	MHz
	$t_{f(IO)out}$	Output high to low fall time	CL=50pF,V_{DD}=2.7-3.6V		125	ns
	$t_{r(IO)out}$	Output low to high rise time			125	ns
01 （10MHz）	$F_{max(IO)out}$	Maximum frequency	CL=50pF,V_{DD}=2.7-3.6V		10	MHz
	$t_{f(IO)out}$	Output high to low fall time	CL=50pF,V_{DD}=2.7-3.6V		25	ns
	$t_{r(IO)out}$	Output low to high rise time			25	ns
11 （50MHz）	$F_{max(IO)out}$	Maximum frequency	CL=30pF,V_{DD}=2.7-3.6V		50	MHz
			CL=50pF,V_{DD}=2.7-3.6V		30	MHz
	$t_{f(IO)out}$	Output high to low fall time	CL=30pF,V_{DD}=2.7-3.6V		20	ns
			CL=50pF,V_{DD}=2.7-3.6V		5	ns
	$t_{r(IO)out}$	Output low to high rise time	CL=30pF,V_{DD}=2.7-3.6V		8	ns
			CL=50pF,V_{DD}=2.7-3.6V		12	ns
	t_{EXTIpw}	The EXTI controller detects the pulse width of the external signal		10		ns

4.3.11 NRST pin characteristics

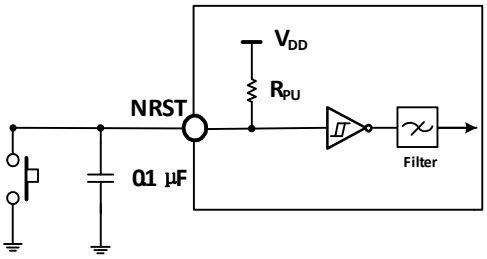
Table 4-23 External reset pin characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{IL(NRST)}$	NRST input low-level voltage		-0.3		$0.28*(V_{DD}-1.8)+0.6$	V
$V_{IH(NRST)}$	NRST input high-level voltage		$0.41*(V_{DD}-1.8)+1.3$		$V_{DD}+0.3$	V
$V_{hys(NRST)}$	NRST Schmitt Trigger voltage hysteresis		150			mV
R_{PU}(1)	Weak pull-up equivalent resistance		30	40	55	kΩ
$V_{F(NRST)}$	NRST input filtered pulse width				100	ns
$V_{NF(NRST)}$	NRST input not filtered pulse width		300			ns

Note: 1. The pull-up resistor is a real resistor in series with a switchable PMOS implementation. The resistance of this PMOS/NMOS switch is very small (approximately 10%).

Circuit reference design and requirements:

Figure 4-7 Typical circuit of external reset pin



4.3.12 TIM timer characteristics

Table 4-24 TIMx characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
$t_{res(TIM)}$	Timer reference clock		1		$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72MHz	13.9		ns
F_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 72MHz	0	36	MHz
R_{esTIM}	Timer resolution			16	bit
$t_{COUNTER}$	16-bit counter clock cycle when the internal clock is selected		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72MHz	0.0139	910	us
t_{MAX_COUNT}	Maximum possible count			65535	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72MHz		59.6	s

4.3.13 I2C interface characteristics

Figure 4-8 I²C bus timing diagram

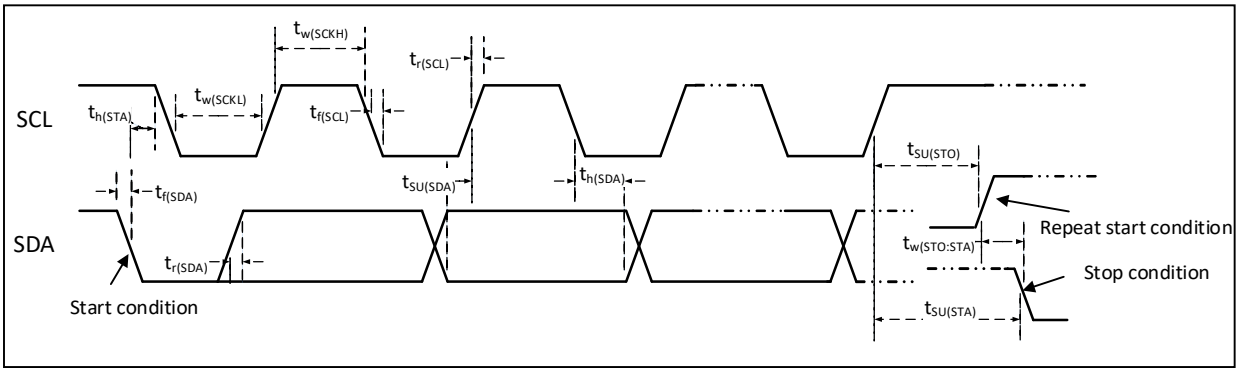


Table 4-25 I²C interface characteristics

Symbol	Parameter	Standard I²C		Fast I²C		Unit
		Min.	Max.	Min.	Max.	
$t_{w(SCKL)}$	SCL clock low time	4.7		1.2		us
$t_{w(SCKH)}$	SCL clock high time	4.0		0.6		us
$t_{SU(SDA)}$	SDA data setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0		0	900	ns
$t_{r(SDA)}/t_{r(SCL)}$	SDA and SCL rise time		1000	20		ns
$t_{f(SDA)}/t_{f(SCL)}$	SDA and SCL fall time		300			ns
$t_{h(STA)}$	Start condition hold time	4.0		0.6		us
$t_{SU(STA)}$	Repeated start condition setup time	4.7		0.6		us
$t_{SU(STO)}$	Stop condition setup time	4.0		0.6		us
$t_{w(STO:STA)}$	Time from stop condition to start condition (bus free)	4.7		1.2		us
C_b	Capacitive load for each bus		400		400	pF

4.3.14 SPI interface characteristics

Figure 4-9 SPI timing diagram in Master mode

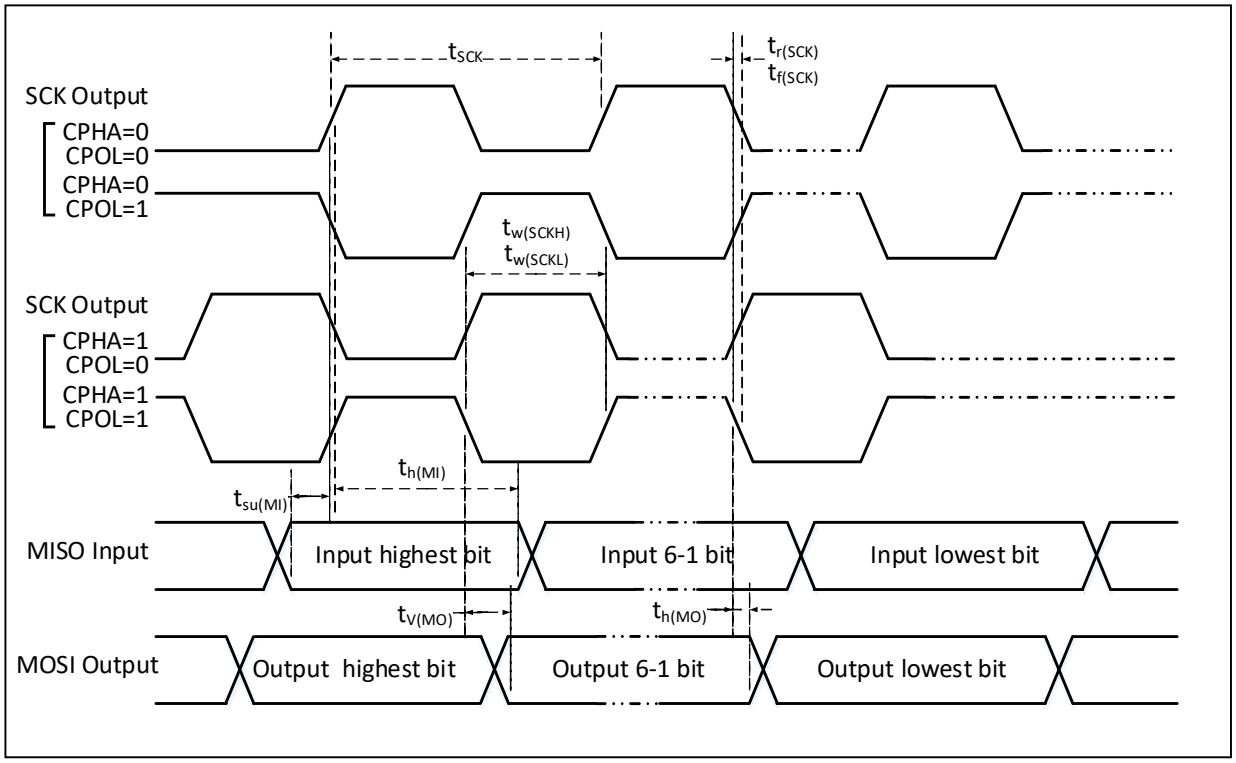


Figure 4-10 SPI timing diagram in Slave mode (CPHA=0)

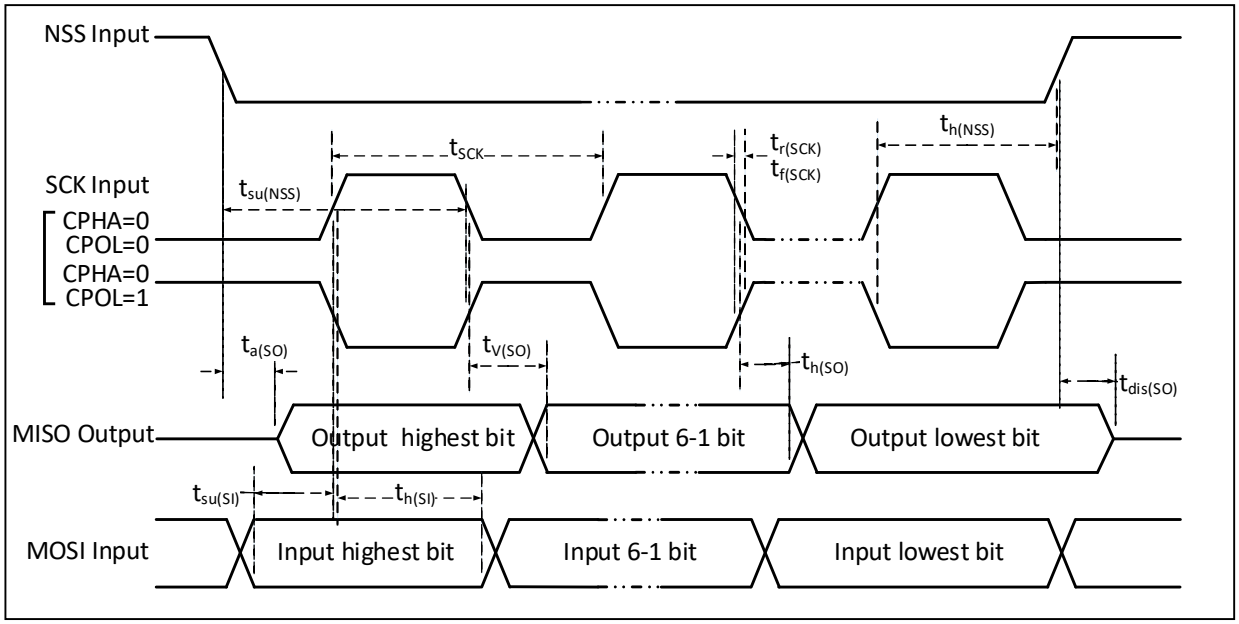


Figure 4-11 SPI timing diagram in Slave mode (CPHA=1)

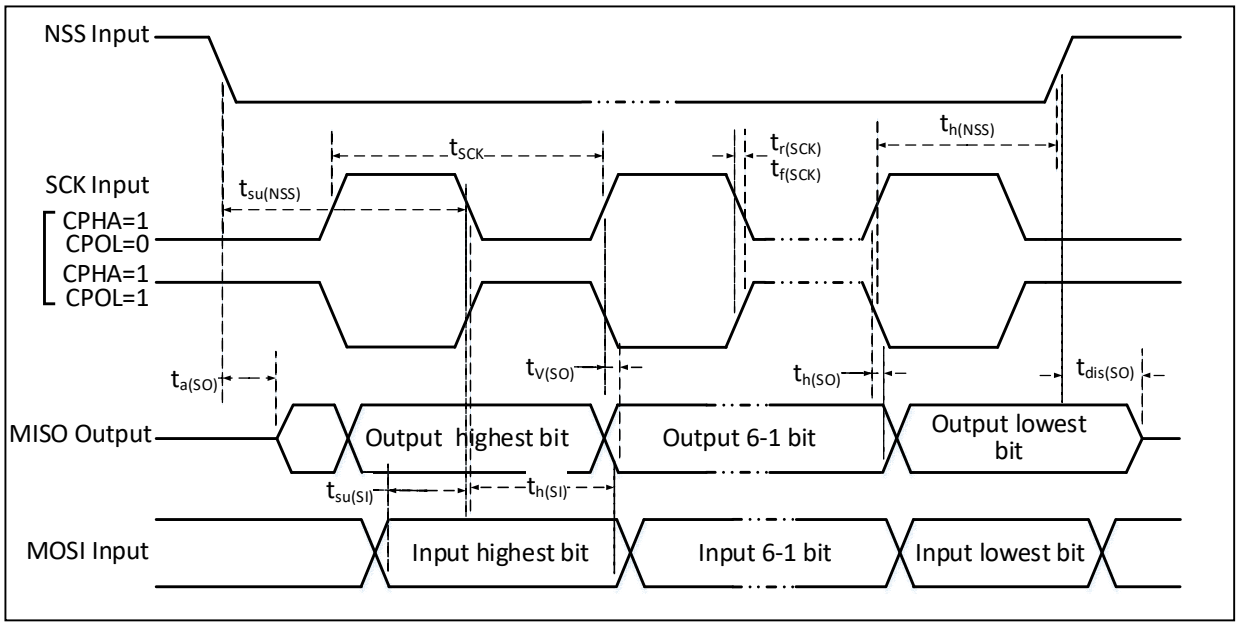


Table 4-26 SPI interface characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
f_{SCK}/t_{SCK}	SPI clock frequency	Master mode		36	MHz
		Slave mode		36	MHz
$t_{r(SCK)}/t_{f(SCK)}$	SPI clock rise and fall time	Load capacitance:C = 30pF		20	ns
$t_{SU(NSS)}$	NSS setup time	Slave mode	$2t_{PCLK}$		ns
$t_{h(NSS)}$	NSS hold time	Slave mode	$2t_{PCLK}$		ns
$t_{w(SCKH)}/t_{w(SCKL)}$	SCK high and low time	Master mode, f_{PCLK} = 36MHz, Prescaler factor = 4	40	60	ns
$t_{SU(MI)}$	Data input setup time	Master mode	5		ns
$t_{SU(SI)}$		Slave mode	5		ns
$t_{h(MI)}$	Data input hold time	Master mode	5		ns
$t_{h(SI)}$		Slave mode	4		ns
$t_{a(SO)}$	Data output access time	Slave mode, f_{PCLK} = 20MHz	0	$1t_{PCLK}$	ns
$t_{dis(SO)}$	Data output disable time	Slave mode	0	10	ns
$t_{V(SO)}$	Data output valid time	Slave mode (After enable edge)		25	ns
$t_{V(MO)}$		Master mode (After enable edge)		5	ns
$t_{h(SO)}$	Data output hold time	Slave mode (After enable edge)	15		ns
$t_{h(MO)}$		Master mode (After enable edge)	0		ns

4.3.15 I2S interface characteristics

Figure 4-12 I²S bus Master mode timing diagram (Philips protocol)

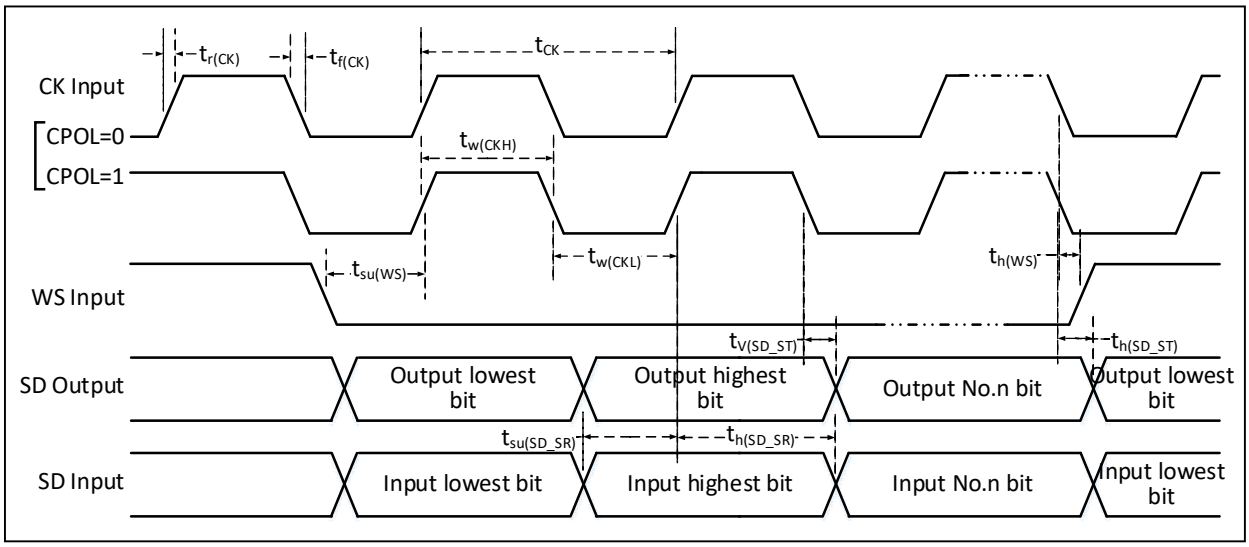


Figure 4-13 I²S bus Slave mode timing diagram (Philips protocol)

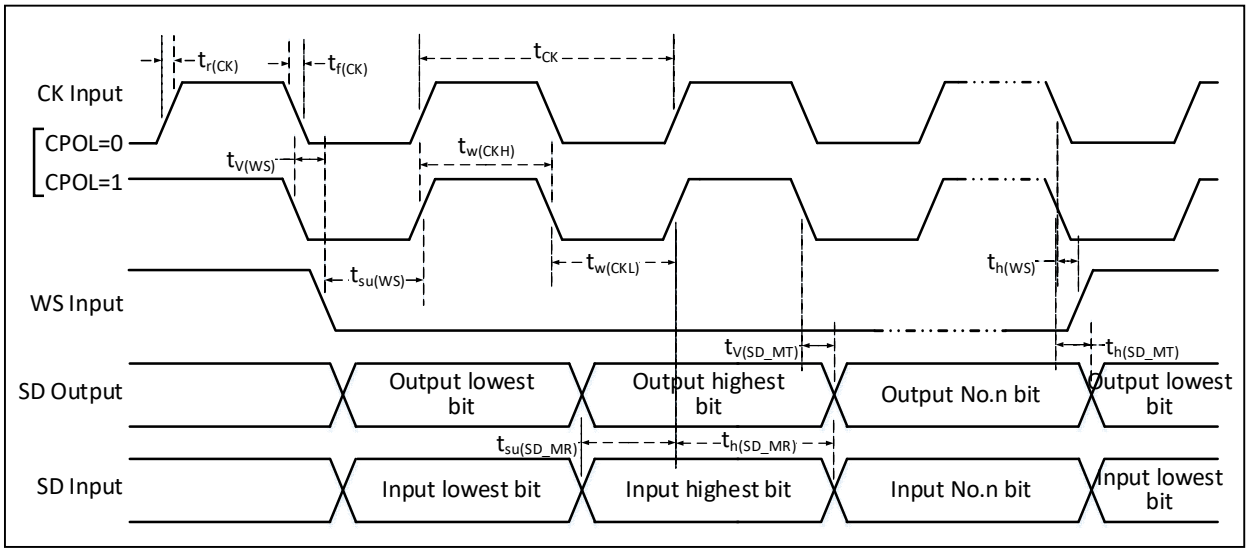


Table 4-27 I²S interface characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
f_{CK}/t_{CK}	I²S clock frequency	Master mode		8	MHz
		Slave mode		8	MHz
$t_{r(CK)}/t_{f(CK)}$	I²S clock rise and fall time	Load capacitance: C = 30pF		20	ns
$t_{V(WS)}$	WS valid time	Master mode		5	ns
$t_{SU(WS)}$	WS setup time	Slave mode	10		ns
$t_{h(WS)}$	WS hold time	Master mode	0		ns
		Slave mode	0		ns
$t_{w(CKH)}/t_{w(CKL)}$	SCK high and low time	Master mode, f_{PCLK} = 36MHz,	40	60	ns

		Prescaler factor =4			
$t_{SU(SD\_MR)}$	Data input setup time	Master mode	8		ns
$t_{SU(SD\_SR)}$		Slave mode	8		ns
$t_{h(SD\_MR)}$	Data input hold time	Master mode	5		ns
$t_{h(SD\_SR)}$		Slave mode	4		ns
$t_{h(SD\_MT)}$	Data output hold time	Master mode (After enable edge)		5	ns
$t_{h(SD\_ST)}$		Slave mode (After enable edge)		5	ns
$t_{V(SD\_MT)}$	Data output valid time	Master mode (After enable edge)		5	ns
$t_{v(SD\_ST)}$		Slave mode (After enable edge)		4	ns

4.3.16 USB interface characteristics

Table 4-28 USB characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{DD}	USB operating voltage		3.0	3.6	V
V_{SE}	Single-ended receiver threshold	V_{DD} = 3.3V	1.2	1.9	V
V_{OL}	Static output low level			0.3	V
V_{OH}	Static output high level		2.8	3.6	V
V_{HSSQ}	High-speed suppression information detection threshold		100	150	mV
V_{HSDSC}	High-speed disconnection detection threshold		500	625	mV
V_{HSOI}	High-speed idle level		-10	10	mV
V_{HSOH}	High-speed data high level		360	440	mV
V_{HSOL}	High-speed data low level		-10	10	mV

4.3.17 SD/MMC interface characteristics

Figure 4-14 SD high-speed timing diagram

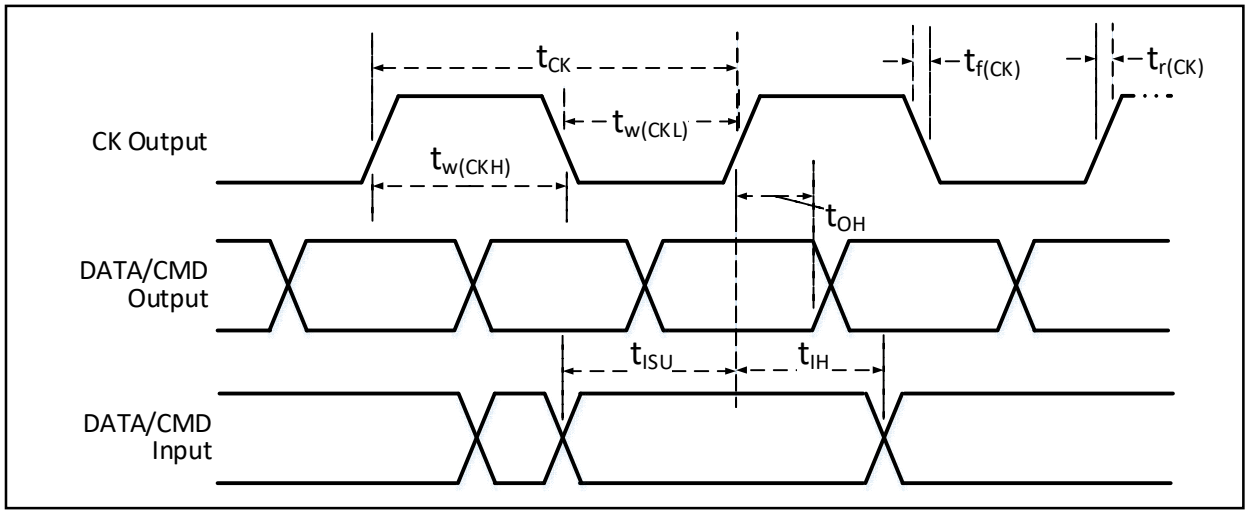


Figure 4-15 SD default timing diagram

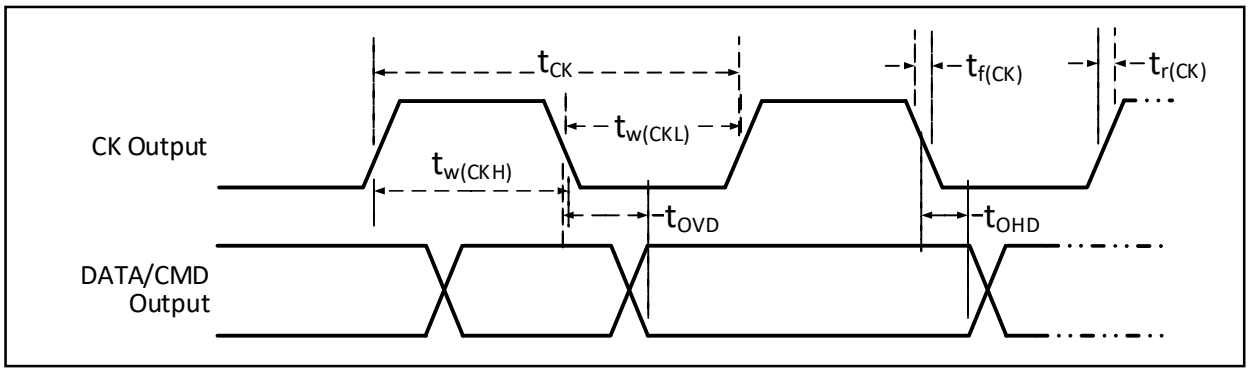


Table 4-29 SD/MMC interface characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
f_{CK}/t_{CK}	Clock frequency in data transfer mode	CL≤30pF		48	MHz
$t_{W(CKL)}$	Clock low time	CL≤30pF	6		ns
$t_{W(CKH)}$	Clock high time	CL≤30pF	6		
$t_{r(CK)}$	Rise Time	CL≤30pF		4	
$t_{f(CK)}$	Fall time	CL≤30pF		4	
CMD/DAT input (refer to CK)					
t_{ISU}	Input setup time	CL≤30pF	7		ns
t_{IH}	Input hold time	CL≤30pF	2		
CMD/DAT output in MMC and SD high-speed mode (refer to CK)					
t_{OV}	Output valid time	CL≤30pF		5	ns
t_{OH}	Output hold time	CL≤30pF	20		
CMD/DAT output in SD default mode (refer to CK)					
t_{OVD}	Output valid default time	CL≤30pF		8	ns
t_{OHD}	Output hold default time	CL≤30pF	20		

4.3.18 FSMC characteristics

Figure 4-16 Asynchronous multiplexed PSRAM/NOR read waveform

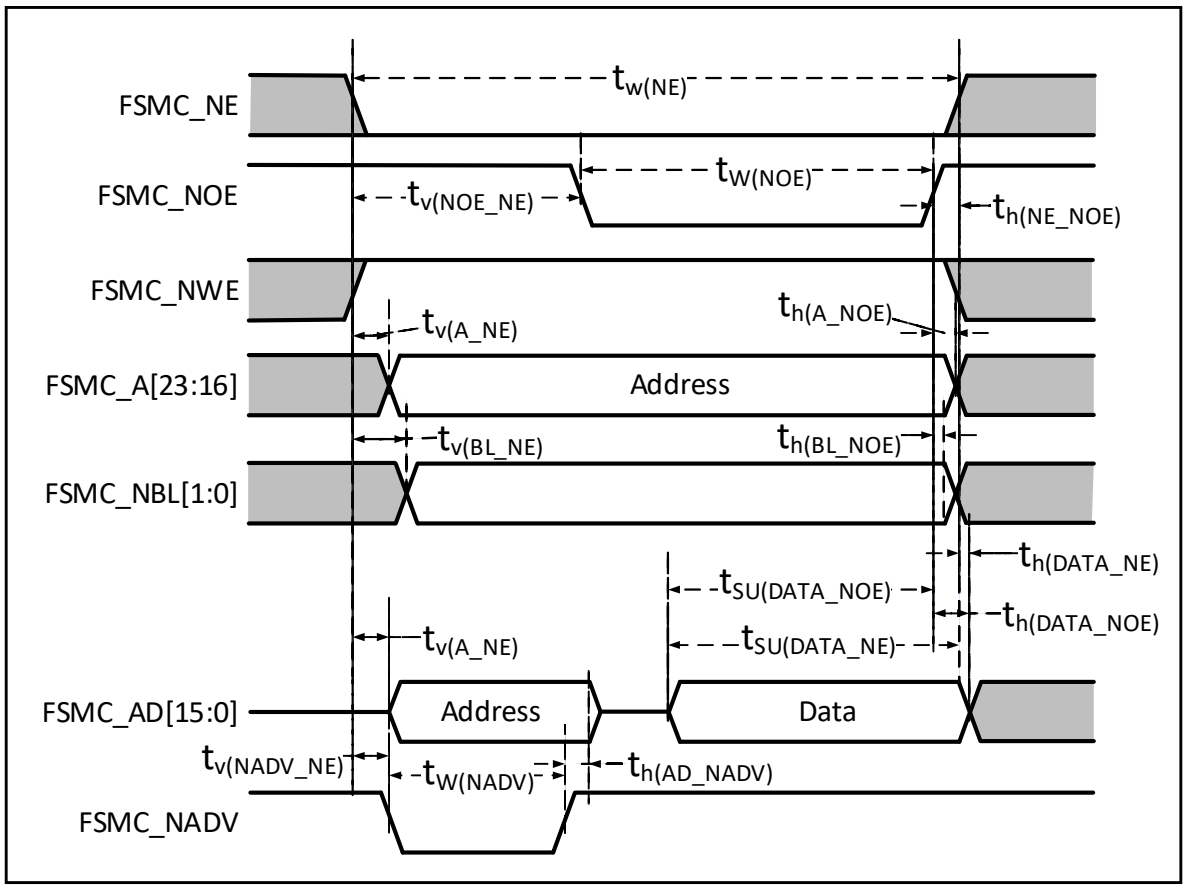


Table 4-30 Asynchronous multiplexed PSRAM/NOR read timings

Symbol	Parameter	Min.	Max.	Unit
$t_{W(NE)}$	FSMC_NE low time	$7t_{HCLK}$		ns
$t_{V(NOE\_NE)}$	FSMC_NE low to FSMC_NOE low	0		
$t_{W(NOE)}$	FSMC_NOE low time	$7t_{HCLK}$		
$t_{h(NE\_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	0		
$t_{V(A\_NE)}$	FSMC_NE low to FSMC_A valid	0	5	
$t_{V(NADV\_NE)}$	FSMC_NE low to FSMC_NADV low	0	5	
$t_{W(NADV)}$	FSMC_NADV low time	t_{HCLK}		
$t_{h(AD\_NADV)}$	FSMC_AD (address) valid hold time after FSMC_NADV high	$2t_{HCLK}$		
$t_{h(A\_NOE)}$	Address hold time after FSMC_NOE high	0		
$t_{h(BL\_NOE)}$	FSMC_BL hold time after FSMC_NOE high	0		
$t_{V(BL\_NE)}$	FSMC_NE low to FSMC_BL valid	0	5	
$t_{SU(DATA\_NE)}$	Data to FSMC_NE high setup time	$3t_{HCLK}$		
$t_{SU(DATA\_NOE)}$	Data to FSMC_NOE high setup time	$3t_{HCLK}$		
$t_{h(DATA\_NE)}$	Data hold time after FSMC_NE high	0		
$t_{h(DATA\_NOE)}$	Data hold time after FSMC_NOE high	0		

Figure 4-17 Asynchronous multiplexed PARAM/NOR write waveform

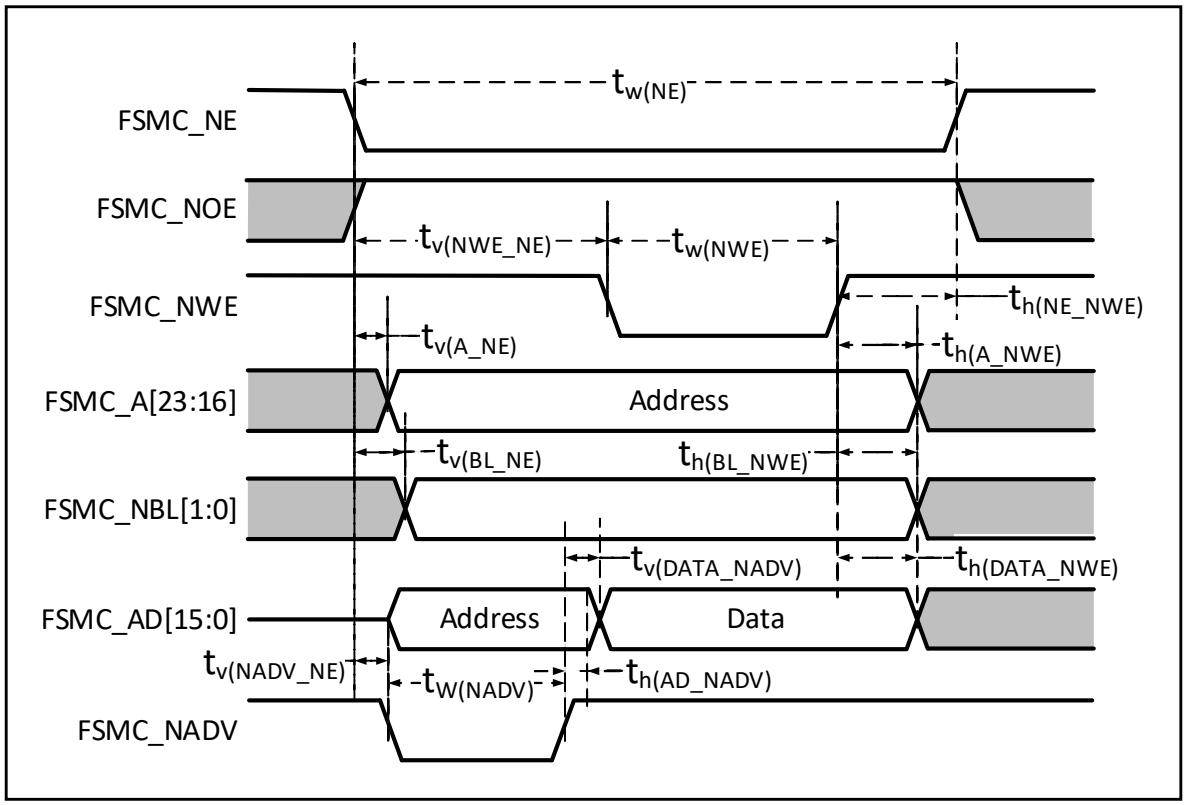


Table 4-31 Asynchronous multiplexed PARAM/NOR write timings

Symbol	Parameter	Min.	Max.	Unit
$t_{W(NE)}$	FSMC_NE low time	$5t_{HCLK}$		ns
$t_{V(NEW\_NE)}$	FSMC_NE low to FSMC_NWE low	$3t_{HCLK}$		
$t_{W(NWE)}$	FSMC_NWE low time	$2t_{HCLK}$		
$t_{h(NE\_NWE)}$	FSMC_NWE high to FSMC_NE high hold time	t_{HCLK}		
$t_{V(A\_NE)}$	FSMC_NE low to FSMC_A valid	0	5	
$t_{V(NADV\_NE)}$	FSMC_NE low to FSMC_NADV low	0	5	
$t_{W(NADV)}$	FSMC_NADV low time	t_{HCLK}		
$t_{h(AD\_NADV)}$	FSMC_AD (address) valid hold time after FSMC_NADV high	$2t_{HCLK}$		
$t_{h(A\_NWE)}$	Address hold time after FSMC_NWE high	t_{HCLK}		
$t_{V(BL\_NE)}$	FSMC_NE low to FSMC_BL valid	0	5	
$t_{h(BL\_NWE)}$	FSMC_BL hold time after FSMC_NWE high	t_{HCLK}		
$t_{V(DATA\_NADV)}$	FSMC_NADV high to data hold time	$2t_{HCLK}$		
$t_{h(DATA\_NWE)}$	Data hold time after FSMC_NWE high	t_{HCLK}		

Figure 4-18 Synchronous multiplexed NOR/PARAM read waveform

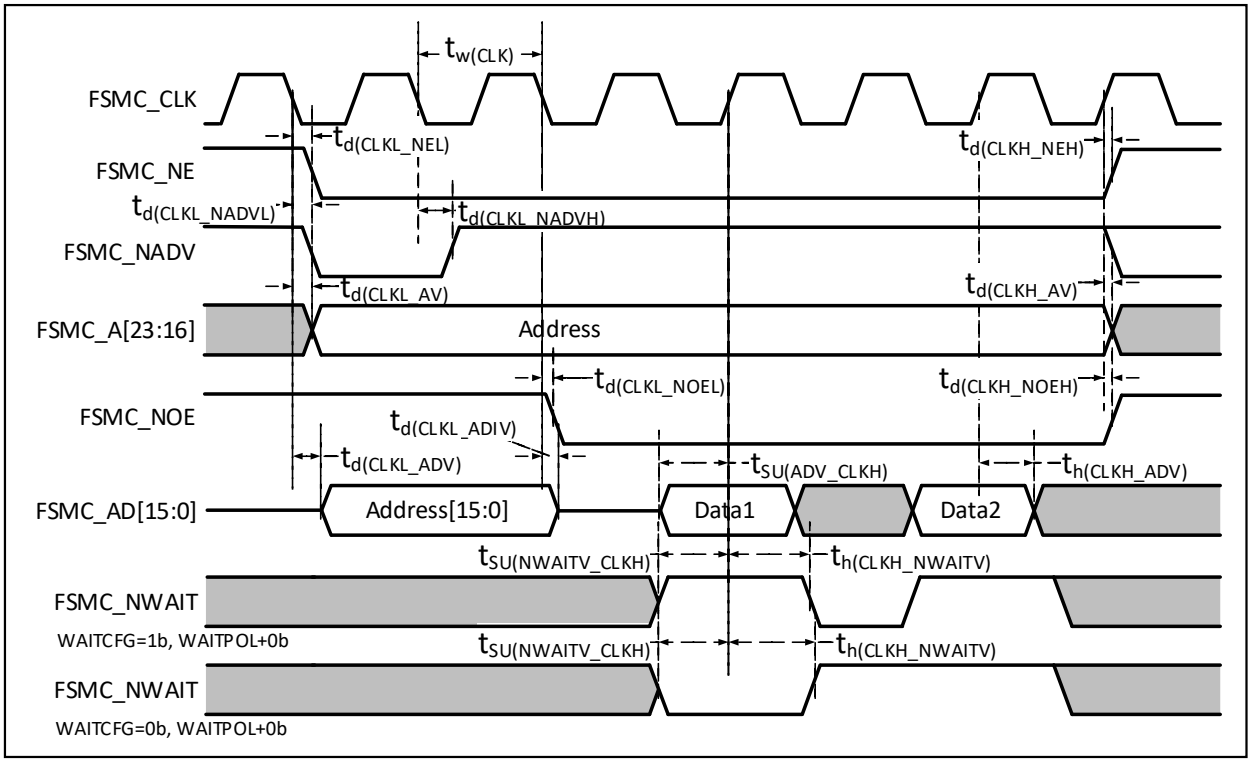


Table 4-32 Synchronous multiplexed NOR/PSRAM read timings

Symbol	Parameter	Min.	Max.	Unit
$t_{W(CLK)}$	FSMC_CLK period	$2t_{HCLK}$		ns
$t_{d(CLKL\_NEL)}$	FSMC_CLK low to FSMC_NE low	0	5	
$t_{d(CLKH\_NEH)}$	FSMC_CLK high to FSMC_NE high	$0.5t_{HCLK}$	$0.5t_{HCLK}$	
$t_{d(CLKL\_NADVL)}$	FSMC_CLK low to FSMC_NADV low	0	5	
$t_{d(CLKL\_NADVH)}$	FSMC_CLK low to FSMC_NADV high	0	5	
$t_{d(CLKL\_AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 16…23)	0	5	
$t_{d(CLKH\_AIV)}$	FSMC_CLK high to FSMC_Ax invalid (x = 16…23)	0	5	
$t_{d(CLKL\_NOEL)}$	FSMC_CLK low to FSMC_NOE low	$2t_{HCLK}$		
$t_{d(CLKH\_NOEH)}$	FSMC_CLK high to FSMC_NOE high	t_{HCLK}		
$t_{d(CLKL\_ADV)}$	FSMC_CLK low to FSMC_AD[15:0] valid	0	5	
$t_{d(CLKL\_ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	0	5	
$t_{SU(ADV\_CLKH)}$	FSMC_AD[15:0] valid data before FSMC_CLK high	8		
$t_{h(CLKH\_ADV)}$	FSMC_AD[15:0] valid data after FSMC_CLK high	8		
$t_{SU(NWAITV\_CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	6		
$t_{h(CLKH\_NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	2		

Figure 4-19 Synchronous multiplexed PSRAM write waveform

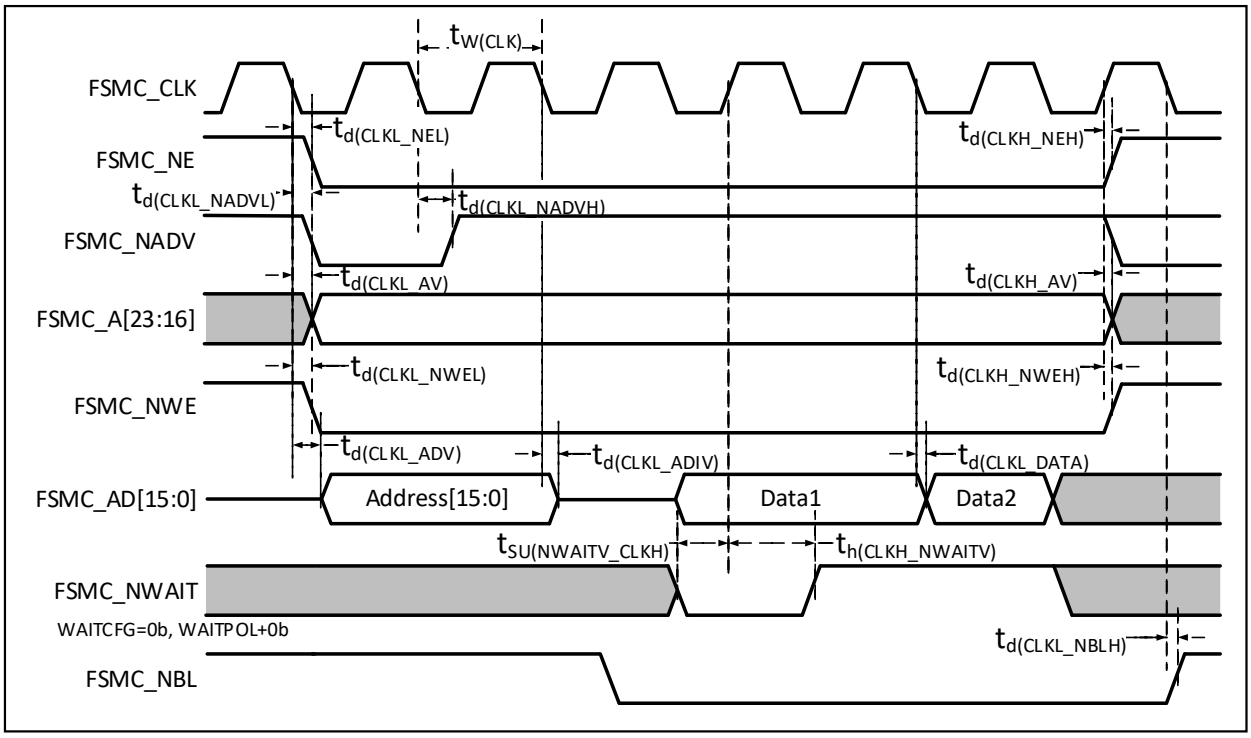


Table 4-33 Synchronous multiplexed PSRAM write timings

Symbol	Parameter	Min.	Max.	Unit
$t_{W(CLK)}$	FSMC_CLK period	$2t_{HCLK}$		ns
$t_{d(CLKL\_NEL)}$	FSMC_CLK low to FSMC_NE low	0	5	
$t_{d(CLKH\_NEH)}$	FSMC_CLK high to FSMC_NE high	$0.5t_{HCLK}$	$0.5t_{HCLK}$	
$t_{d(CLKL\_NADVL)}$	FSMC_CLK low to FSMC_NADV low	0	5	
$t_{d(CLKL\_NADVH)}$	FSMC_CLK low to FSMC_NADV high	0	5	
$t_{d(CLKL\_AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 16…23)	0	5	
$t_{d(CLKH\_AIV)}$	FSMC_CLK high to FSMC_Ax invalid (x = 16…23)	0	5	
$t_{d(CLKL\_NWEL)}$	FSMC_CLK low to FSMC_NWE low	0		
$t_{d(CLKH\_NWEH)}$	FSMC_CLK high to FSMC_NWE high	0		
$t_{d(CLKL\_ADV)}$	FSMC_CLK low to FSMC_AD[15:0] valid	0	5	
$t_{d(CLKL\_ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	0	5	
$t_{d(CLKL\_DATA)}$	FSMC_AD[15:0] valid after FSMC_CLK low	2		
$t_{SU(NWAITV\_CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	6		
$t_{h(CLKH\_NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	2		
$t_{d(CLKL\_NBLH)}$	FSMC_CLK low to FSMC_NBL high	2		

NAND controller waveform and timing

Test conditions: NAND operation area, 16-bit data width is selected, ECC calculation circuit is enabled, 512-byte page size, other timing configurations are setting registers FSMC_PCR2=0x0002005E, FSMC_PMEM2=0x01020301, FSMC_PATT2=0x01020301.

Figure 4-20 NAND controller read waveform

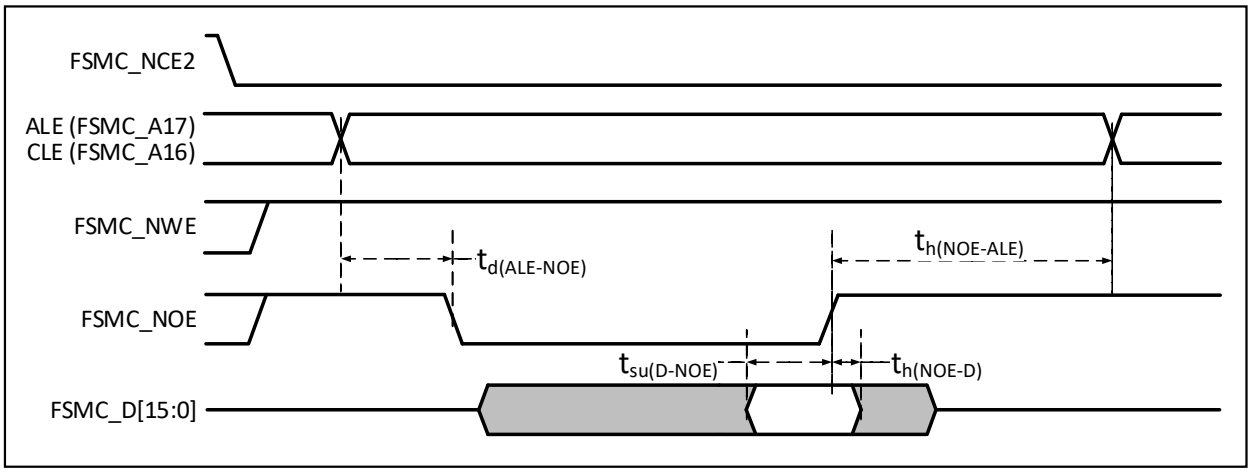


Figure 4-21 NAND controller write waveform

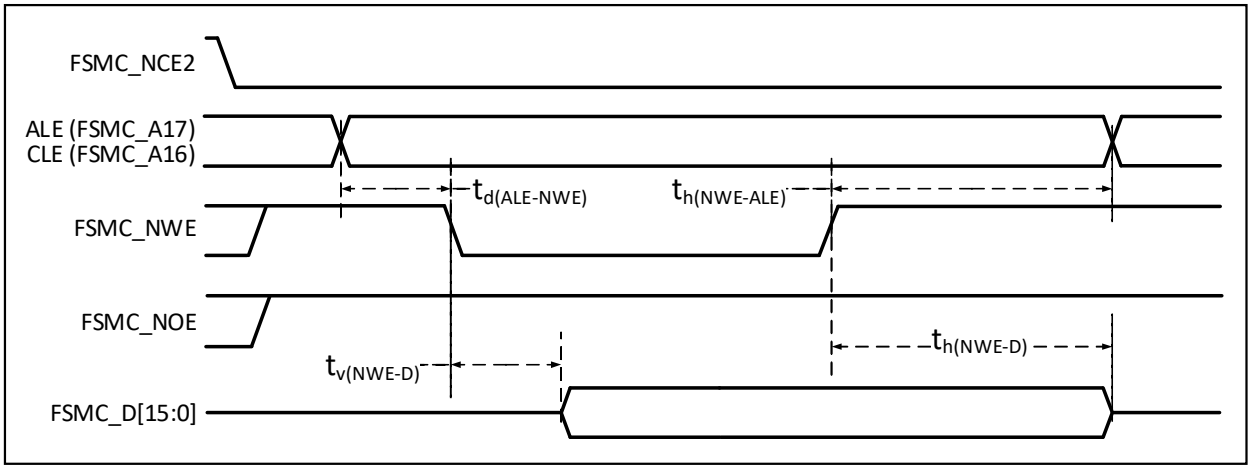


Figure 4-22 NAND controller read waveform in general-purpose storage space

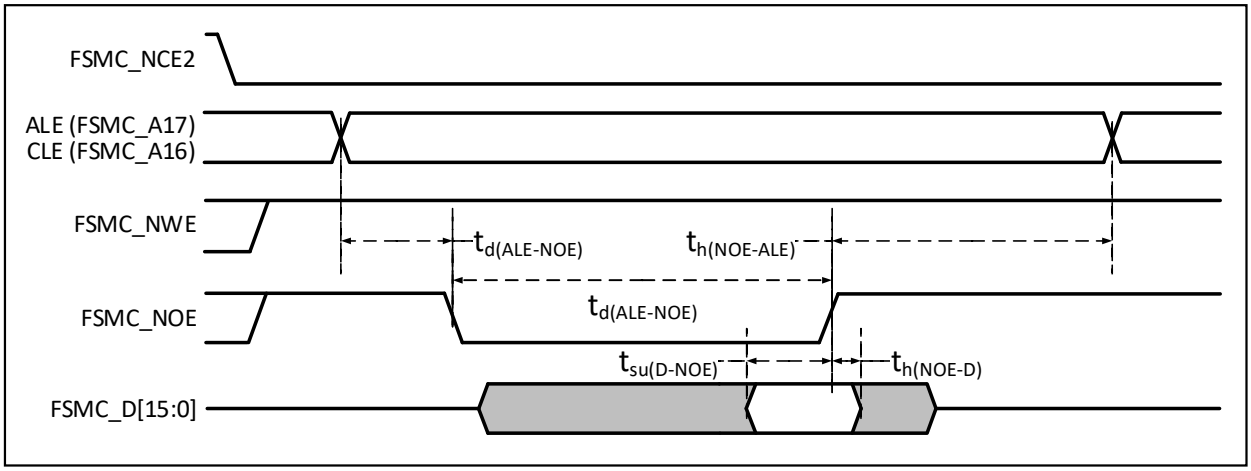


Figure 4-23 NAND controller write waveform in general-purpose storage space

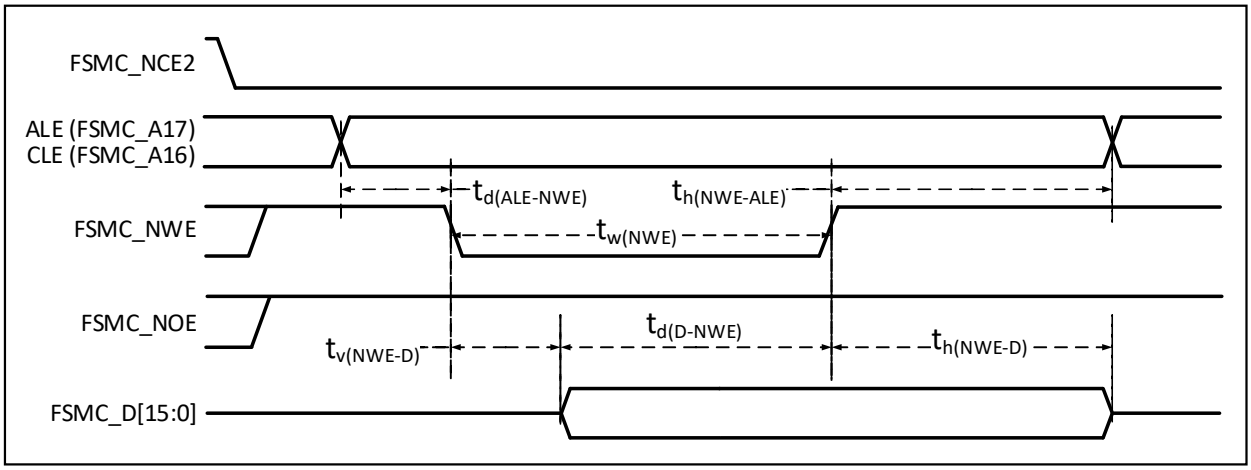


Table 4-34 Timing characteristics of NAND Flash read and write cycles

Symbol	Parameter	Min.	Max.	Unit
$t_{d(D-NWE)}$	Before FSMC_NWE high to FSMC_D[15:0] data valid	$4t_{HCLK}$		ns
$t_{w(NOE)}$	FSMC_NOE low time	$4t_{HCLK}$		
$t_{su(D-NOE)}$	Before FSMC_NOE high to FSMC_D[15:0] data valid	20		
$t_{h(NOE-D)}$	After FSMC_NOE high to FSMC_D[15:0] data valid	15		
$t_{w(NWE)}$	FSMC_NWE low time	$4t_{HCLK}$		
$t_{v(NWE-D)}$	FSMC_NWE low to FSMC_D[15:0] data valid	0		
$t_{h(NWE-D)}$	FSMC_NWE high to FSMC_D[15:0] data invalid	$2t_{HCLK}$		
$t_{d(ALE-NWE)}$	Before FSMC_NWE low to FSMC_ALE valid	$2t_{HCLK}$		
$t_{h(NWE-ALE)}$	FSMC_NWE high to FSMC_ALE invalid	$2t_{HCLK}$		
$t_{d(ALE-NOE)}$	Before FSMC_NOE low to FSMC_ALE valid	$2t_{HCLK}$		
$t_{h(NOE-ALE)}$	FSMC_NOE high to FSMC_ALE invalid	$4t_{HCLK}$		

4.3.19 DVP interface characteristics

Figure 4-24 DVP timing waveform

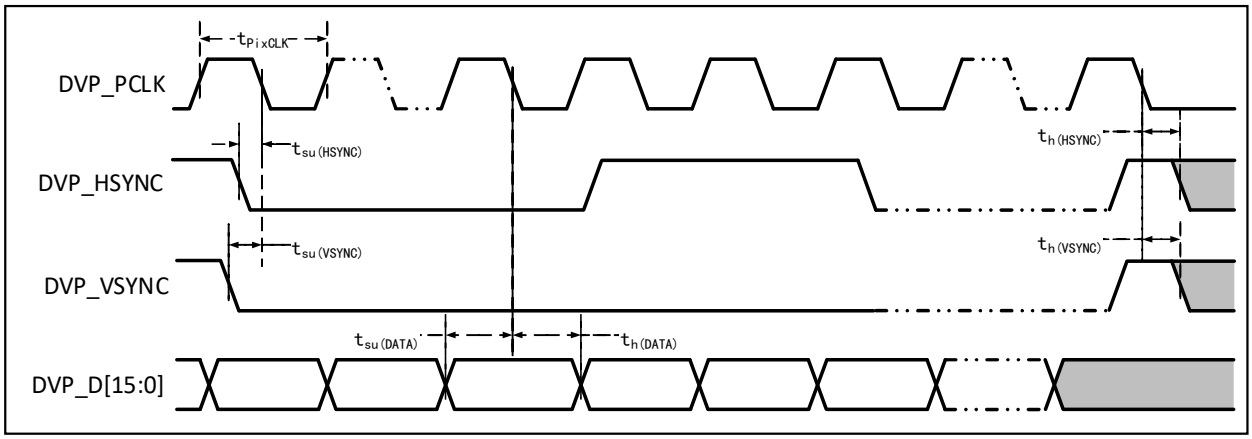


Table 4-35 DVP characteristics

Symbol	Parameter	Min.	Max.	Unit
f_{PixCLK}/t_{PixCLK}	Pixel clock input frequency		144	MHz
$DuCy_{(PixCLK)}$	Pixel clock duty cycle	15		%
$t_{su(DATA)}$	Data setup time	2		ns
$t_{h(DATA)}$	Data hold time	1		
$t_{su(HSYNC)}/t_{su(VSYNC)}$	HSYNC/VSYNC signal input setup time	2		
$t_{h(HSYNC)}/t_{h(VSYNC)}$	HSYNC/VSYNC signal input hold time	1		

4.3.20 Gigabit Ethernet interface characteristics

Figure 4-25 ETH-SMI timing waveform

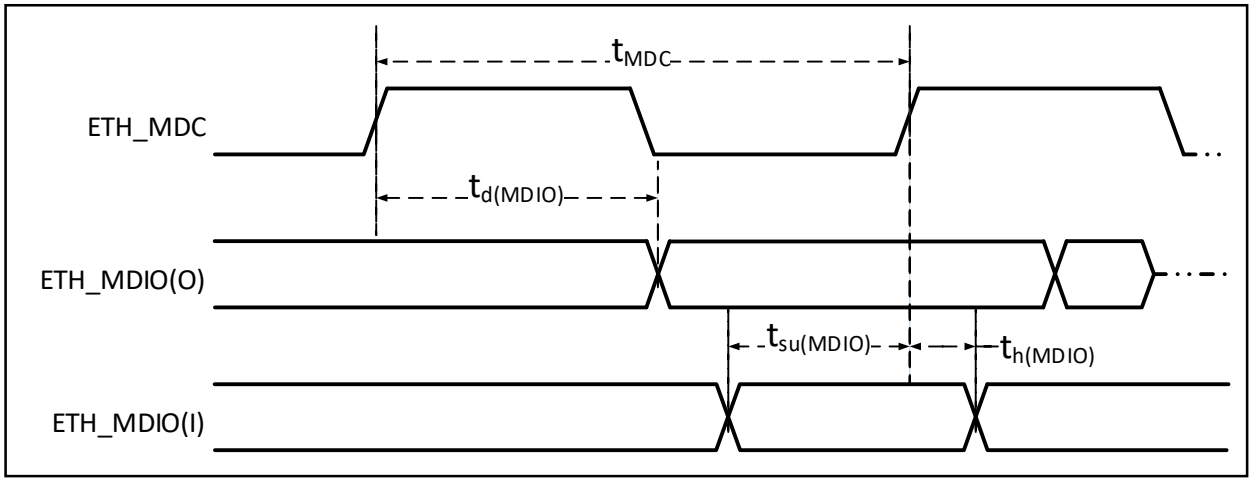


Table 4-36 SMI signal characteristics of Ethernet MAC

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{MDC}/t_{MDC}	MDC clock frequency			2.5	MHz
$t_{d(MDIO)}$	MDIO write data valid time	0		300	ns
$t_{su(MDIO)}$	Read data setup time	10			
$t_{h(MDIO)}$	Read data hold time	10			

Figure 4-26 ETH-RMII signal timing waveform

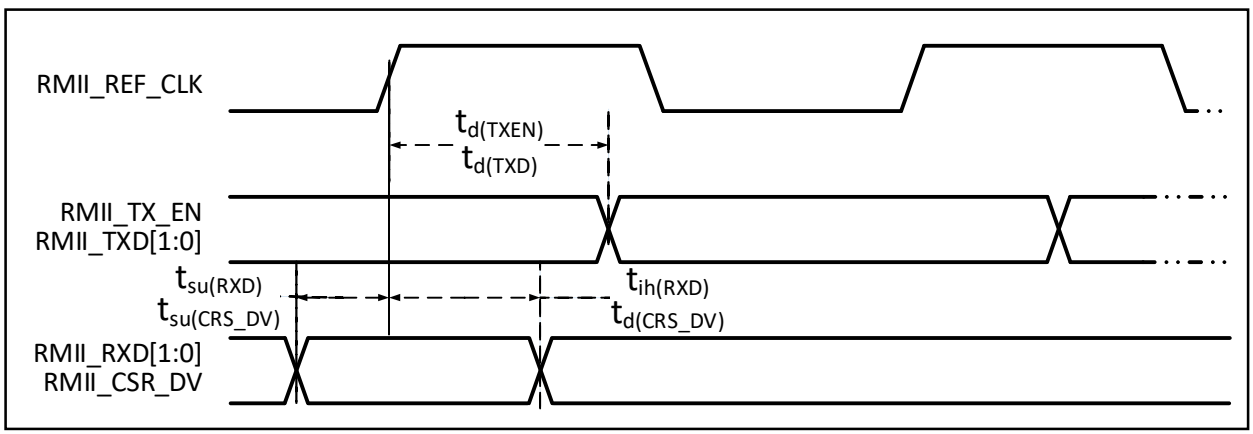


Table 4-37 RMII signal characteristics of Ethernet MAC

Symbol	Parameter	Min.	Typ.	Max.	Unit
$t_{su(RXD)}$	Setup time of received data	4			ns
$t_{ih(RXD)}$	Hold time of received data	2			
$t_{su(CRS\_DV)}$	Carrier detect signal setup time	4			
$t_{ih(CRS\_DV)}$	Carrier detect signal hold time	2			
$t_{d(TXEN)}$	Transmission enable effective delay time			16	
$t_{d(TXD)}$	Data transmission effective delay time			16	

Figure 4-27 ETH-MII signal timing waveform

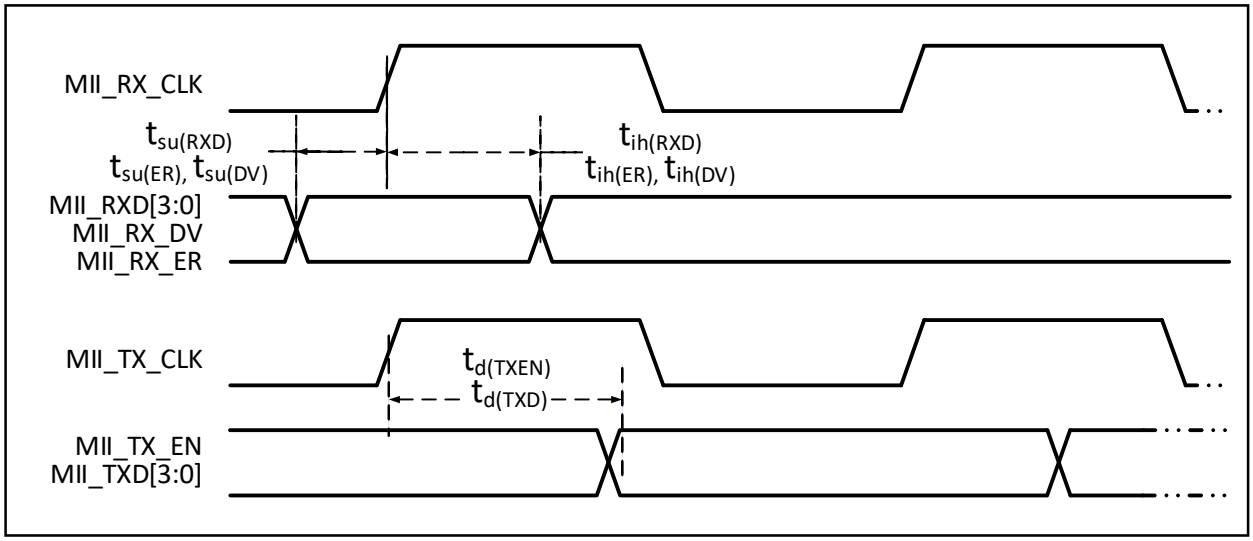


Table 4-38 MII signal characteristics of Ethernet MAC

Symbol	Parameter	Min.	Typ.	Max.	Unit
$t_{su(RXD)}$	Setup time of received data	10			ns
$t_{ih(RXD)}$	Hold time of received data	10			
$t_{su(DV)}$	Data valid signal setup time	10			
$t_{ih(DV)}$	Data valid signal hold time	10			
$t_{su(ER)}$	Error signal setup time	10			
$t_{ih(ER)}$	Error signal hold time	10			
$t_{d(TXEN)}$	Transmission enable effective delay time			16	
$t_{d(TXD)}$	Data transmission effective delay time			16	

Figure 4-28 ETH-RGMII signal timing waveform

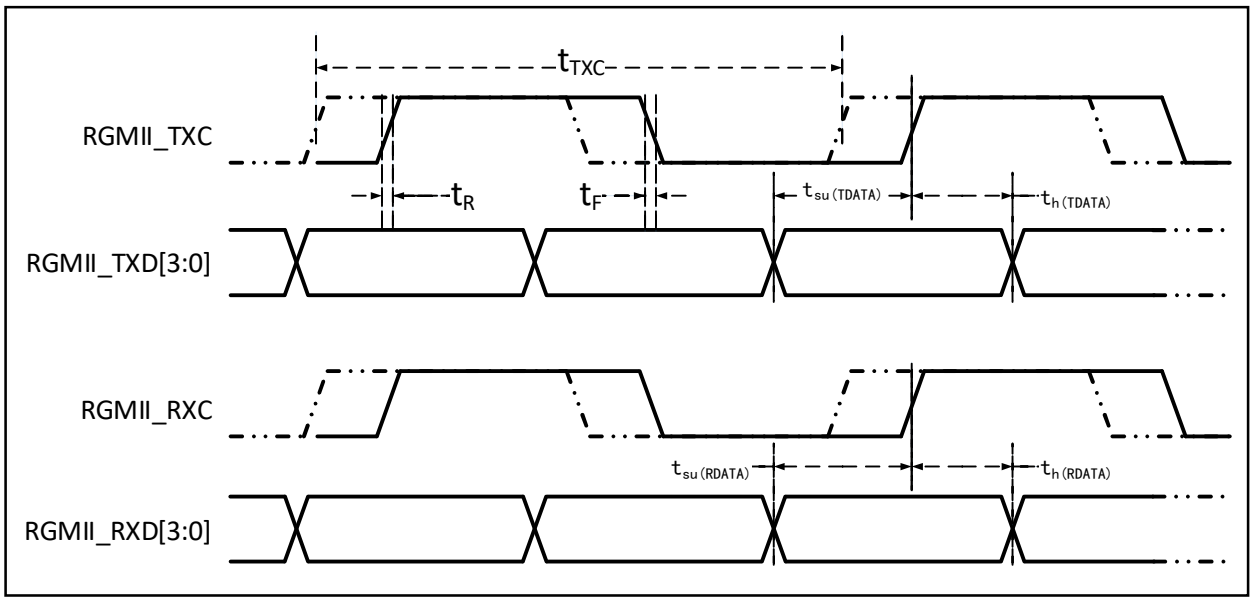


Table 4-39 RGMII signal characteristics of Ethernet MAC

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{TXC}/t_{TXC}	TXC/RXC clock frequency	7.2	8	8.8	ns
t_R	TXC/RXC rise time			2.0	
t_F	TXC/RXC fall time			2.0	
$t_{su(TDATA)}$	Transmit data setup time	1.2	2.0		
$t_{h(TDATA)}$	Transmit data hold time	1.2	2.0		
$t_{su(RDATA)}$	Input data setup time	1.2	2.0		
$t_{h(RDATA)}$	Input data hold time	1.2	2.0		

4.3.21 12-bit ADC characteristics

Table 4-40 ADC characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage		2.4		3.6	V
V_{REF+}	Positive reference voltage	V_{REF+} cannot be more than V_{DDA}	2.4		V_{DDA}	V
I_{VREF}	Reference current			160	220	uA
I_{DDA}	Supply current			480	530	uA
f_{ADC}	ADC clock frequency				14	MHz
f_S	Sampling rate		0.05		1	MHz
f_{TRIG}	External trigger frequency				16	$1/f_{ADC}$
V_{AIN}	Conversion voltage range		0		V_{REF+}	V
R_{AIN}	External input impedance				50	kΩ
R_{ADC}	Sampling switch resistance			0.6	1	kΩ
C_{ADC}	Internal sample and hold capacitor			8		pF

				40		
t_{Iat}	Injected trigger conversion latency				2	$1/f_{ADC}$
t_{Iatr}	Regular trigger conversion latency				2	$1/f_{ADC}$
t_s	Sampling time		1.5		239.5	$1/f_{ADC}$
t_{STAB}	Power-on time				1	us
t_{CONV}	Total conversion time (including sampling time)		14		252	$1/f_{ADC}$

Note: Above parameters are guaranteed by design.

Formula: Maximum R_{AIN}

$$R_{AIN} < \frac{Ts}{f_{ADC} \times C_{ADC} \times \ln 2^{N+2}} - R_{ADC}$$

The above formula is used to determine the maximum external impedance so that the error can be less than 1/4 LSB. Where N=12 (representing 12-bit resolution).

Table 4-41 Maximum RAIN when f_{ADC} = 14MHz

T_S(cycle)	t_S (us)	Maximum R_{AIN}(kΩ)
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	Invalid
239.5	17.1	Invalid

Table 4-42 ADC error

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
EO	Offset error	f_{PCLK2} = 56 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 3.3V		±2		LSB
ED	Differential nonlinearity error			±0.5	±3	
EL	Integral nonlinearity error			±1	±4	

C_p represents the parasitic capacitance on the PCB and the pad (about 5pF), which may be related to the quality of the pad and PCB layout. A larger C_p value will reduce the conversion accuracy, the solution is to reduce the f_{ADC} value.

Figure 4-29 ADC typical connection diagram

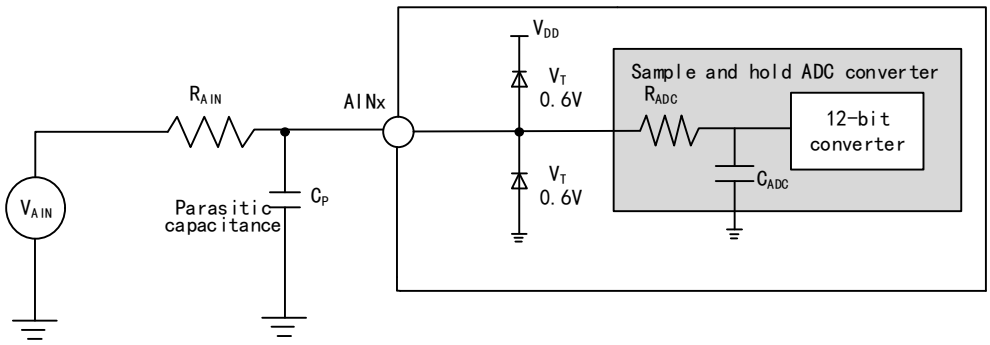
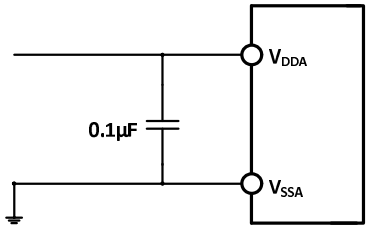


Figure 4-30 Analog power supply and decoupling circuit reference



4.3.22 Temperature sensor characteristics

Table 4-43 Temperature sensor characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
R_{TS}	Measurement range of temperature sensor		-40		85	℃
A_{TSC}	Measurement range of temperature sensor after software calibration			±12		℃
Avg_Slope	Average slope (negative temperature coefficient)		3.8	4.3	4.7	mV/℃
V_{25}	Voltage at 25℃		1.34	1.40	1.46	V
T_{S_temp}	ADC sampling time when reading temperature	f_{ADC} = 14MHz			17.1	us

4.3.23 DAC characteristics

Table 4-44 DAC characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage		2.4	3.3	3.6	V
V_{REF+}	Positive reference voltage	$V_{REF+} \leq V_{DDA}$	2.4	3.3	3.6	V
R_L(1)	Resistive load with buffer ON		5			kΩ
C_L(1)	Capacitive load with buffer ON				50	pF
V_{OUT_MIN}(1)	12-bit DAC conversion with buffer ON		3			mV
V_{OUT_MAX}(1)					V_{REF+}-0.01	V
V_{OUT_MIN}(1)	12-bit DAC conversion with buffer			0.1		mV

V_{OUT_MAX}(1)	OFF				V_{REF+}-1LSB	V
I_{VREF+}	With no load, 0x800 on the inputs			58		uA
	With no load, 0xF1C at V_{REF+}=3.6V on the inputs			194		
	With no load, 0x555 (worst) at V_{REF+}=3.6V on the inputs			331		
I_{DDA}	With buffer ON and no load, 0x800 on the inputs			170		uA
	With buffer ON and no load, 0xF1C on the inputs at V_{REF+}=3.6V,			150		
	With buffer ON and no load, 0x555 (worst) at V_{REF+}=3.6V on the inputs			170		
DNL	Differential nonlinearity error			±2		LSB
INL	Integral nonlinearity error	After calibration of offset error and gain error		±4		LSB
Offset	Offset error				±8	mV
		V_{REF+}=3.6V			±10	LSB
Gain error		DAC in 12-bit configuration		±0.4		%
Amplifier gain(1)	Amplifier gain in open loop	5kΩ load (max)	80	85		dB
$t_{SETTLING}$	Setting time (full scale: for an input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1 LSB)	C_{LOAD}≤50pF R_{LOAD}≥5kΩ		3	4	us
Update rate	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB),	C_{LOAD}≤50pF R_{LOAD}≥5kΩ			1	MS/s
t_{WAKEUP}	Time to wake up from off state (PDV18 changes from 1 to 0)	C_{LOAD}≤50pF, R_{LOAD}≥5kΩ, input codes between the lowest and highest possible ones		6.5	10	us
PSRR+(1)	Power supply rejection ratio (relative to V_{DDA}) (static DC measurement)	No R_{LOAD}, C_{LOAD}≤50pF		-100	-75	dB

Note: 1. Guaranteed by design, not tested in production.

4.3.18 OPA characteristics

Table 4-45 OPA characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage		2.4	3.3	3.6	V
C_{MIR}	Common mode input voltage		0		V_{DDA}-0.9	V
$V_{IOFFSET}$	Input offset voltage			1.5	6	mV
I_{LOAD}	Drive current				600	uA
$I_{DDOPAMP}$	Current consumption	No load, static mode		195		uA
C_{MRR}(1)	Common mode rejection ratio	@1KHz		96		dB
P_{SRR}(1)	Power supply rejection ratio	@1KHz		86		dB
A_V(1)	Open loop gain	C_{LOAD}=5pF		136		dB
G_{BW}(1)	Unit gain bandwidth	C_{LOAD}=5pF		19		MHz
P_M(1)	Phase margin	C_{LOAD}=5pF		93		
S_R(1)	Slew rate limited	C_{LOAD}=5pF		8		V/us
t_{WAKUP}(1)	Setup time from shutdown to wake up, 0.1%	Input V_{DDA}/2, C_{LOAD}=5pF,R_{LOAD}=4kΩ			368	ns
R_{LOAD}	Resistive load		4			kΩ
C_{LOAD}	Capacitive load				50	pF
V_{OHSAT}(2)	High saturation output voltage	R_{LOAD}=4kΩ, input V_{DDA}	V_{DDA}-45			mV
		R_{LOAD}=20kΩ, input V_{DDA}	V_{DDA}-10			
V_{OLSAT}(2)	Low saturation output voltage	R_{LOAD}=4kΩ, input 0			0.5	mV
		R_{LOAD}=20kΩ, input 0			0.5	
EN(1)	Equivalent input voltage noise	R_{LOAD}=4kΩ,@1KHz		83		$\frac{nv}{\sqrt{Hz}}$
		R_{LOAD}=4kΩ,@10KHz		42		

Note: 1. Design parameters are guaranteed.

2. The load current limits the saturated output voltage.

Chapter 5 Package and ordering information

Packages

Part No.	Package	Body size	Lead pitch	Description	Packing type
CH32F203CBT6	LQFP48	7*7mm	0.5mm	LQFP48(7*7) patch	Tray
CH32F203RBT6	LQFP64M	10*10mm	0.5mm	LQFP64M(10*10) patch	Tray
CH32F203RCT6	LQFP64M	10*10mm	0.5mm	LQFP64M(10*10) patch	Tray
CH32F203VCT6	LQFP100	14*14mm	0.5mm	LQFP100(14*14) patch	Tray
CH32F205RBT6	LQFP64M	10*10mm	0.5mm	LQFP64M(10*10) patch	Tray
CH32F207VCT6	LQFP100	14*14mm	0.5mm	LQFP100(14*14) patch	Tray

Note: 1. The packing type of QFP/QFN is usually tray. Please confirm with the packaging factory for specific part number.

*2. Size of tray: The size of tray is generally a uniform size (322.6*135.9*7.62). There are differences in the size of the restriction holes for different package types, and there are differences between different packaging factories for tubes, please confirm with the manufacturer for details.*

Note: All dimensions are in millimeters. The pin center spacing values are nominal values, with no error. Other than that, the dimensional error is not greater than the greater of ±0.2mm or 10%.

Figure 5-1 LQFP48 package

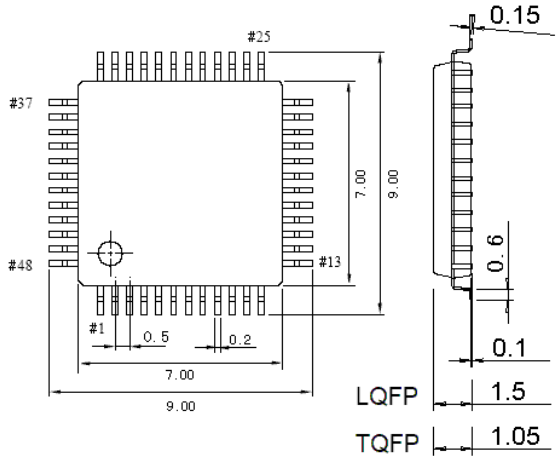


Figure 5-2 LQFP64M package

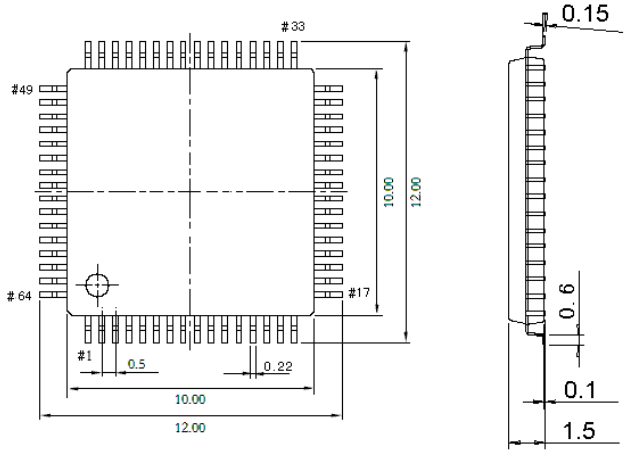
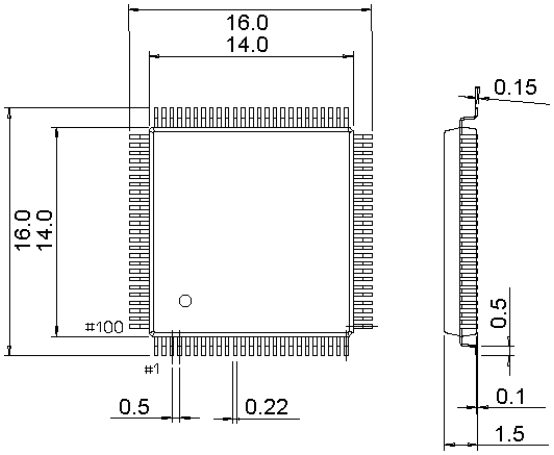


Figure 5-3 LQFP100 package



Series product naming rules

Example: CH32 V 3 03 R 8 T 6

Device family

F = ARM-based

V = QingKe RISC-V-based

Product type

0 = QingKe V2 core

1 = M3/ QingKe V3A core, clock speed @72M

2 = M3/ QingKe V4B_C core, clock speed @144M

3 = QingKe V4F floating-point core, clock speed @144M

Device subfamily

03 = General-purpose

05 = Connectivity (USB high-speed, SDIO, dual CAN)

07 = Interconnectivity (USB high-speed, dual CAN, Ethernet, DVP, SDIO, FSMC)

08 = Wireless (BLE5.3, CAN, USB, Ethernet)

Pin count

J = 8 pins	A = 16 pins	F = 20 pins
G = 28 pins	K = 32 pins	T = 36 pins
C = 48 pins	R = 64 pins	W = 68 pins
V = 100 pins	Z = 144 pins	

Flash memory size

4 = 16 Kbytes of Flash memory

6 = 32 Kbytes of Flash memory

8 = 64 Kbytes of Flash memory

B = 128 Kbytes of Flash memory

C = 256 Kbytes of Flash memory

Package

T = LQFP

U = QFN R = QSOP

P = TSSOP M = SOP

Temperature range

6 = -40°C～85°C (industrial-grade)

7 = -40°C～105°C (automotive-grade 2)

3 = -40°C～125°C (automotive-grade 1)

D = -40°C～150°C (automotive-grade 0)