1. DESCRIPTION

The XL1057GT/3 is a high-speed CAN transceivers.
It provides an interface between a Controller Area Network (CAN) protocol controller and the physical two-wireCAN bus.
The transceiver is designed for high-speed CAN applications in the automotive industry, providing the differential transmit and receive capability to (a microcontroller with) a CAN protocol controller.The XL1057GT/3 offers a feature set optimized for 12V automotive applications, with significantimprovements over first-generation CAN transceivers from XINLUDA, such as the XL1050, andexcellent ElectroMagnetic Compatibility (EMC) performance.
The XL1057GT/3 also displays idealpassive behavior to the CAN bus when the supply voltage is off.
The XL1057GT/3 implements the CAN physical layer as defined in ISO 11898-2:2016. This implementation enables reliable communication in the CAN FD fast phase at data rates up to 5 Mbit/s. The XL1057GT/3 featureshorter propagation delay, supporting larger network topologies.These features make the XL1057GT3 an excellent choice for HS-CAN networks that only requirebasic CAN functionality.

2. FEATURES

- Fully ISO 11898-2:2016
- Optimized for use in 12V automotive systems
- Low Electromagnetic Emission (EME) and high Electromagnetic Immunity (EMI), according to proposed EMC Standards IEC 62228-3 and SAE J2962-2
- VIO pin can be interfaced directly with microcontrollers with supply voltages from 3.3V to 5V
- Functional behavior predictable under all supply conditions
- Transceiver disengages from the bus (high-ohmic) when the supply voltage drops below the undervoltage threshold
- Transmit Data (TXD) dominant time-out function
- Internal biasing of TXD and S input pins
- High ESD handling capability on the bus pins (8 kV IEC and HBM)
- Bus pins protected against transients in automotive environments
- Undervoltage detection on pins VCC and VIO
- Thermally protected

3. QUICK REFERENCE DATA

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
V_{IO}	supply voltage on pin V_{IO}		2.90	-	5.5	V
$V_{uvd(VCC)}$	undervoltage detection voltage on pin V_{CC}		3.5	4	4.3	V
$V_{uvd(VIO)}$	undervoltage detection voltage on pin V_{IO}		2.1	-	2.8	V
I_{CC}	supply current	Silent mode	0.1	-	0.3	mA
		Normal mode; bus recessive	2	5	10	mA
		Normal mode; bus dominant	20	45	70	mA
I_{IO}	supply current on pin V_{IO}	Silent mode	-	11	20	µA
		Normal mode				
		recessive; $V_{TXD} = V_{IO}$	-	7	30	µA
		dominant; V_{TXD} = 0 V	-	110	320	µA
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 at pins CANH and CANL	-8	-	+8	kV
V_{CANH}	voltage on pin CANH	limiting value according to IEC60134	-42	-	+42	V
V_{CANL}	voltage on pin CANL	limiting value according to IEC60134	-42	-	+42	V
T_{vj}	virtual junction temperature		-40	-	+125	°C

4. BLOCK DIAGRAM

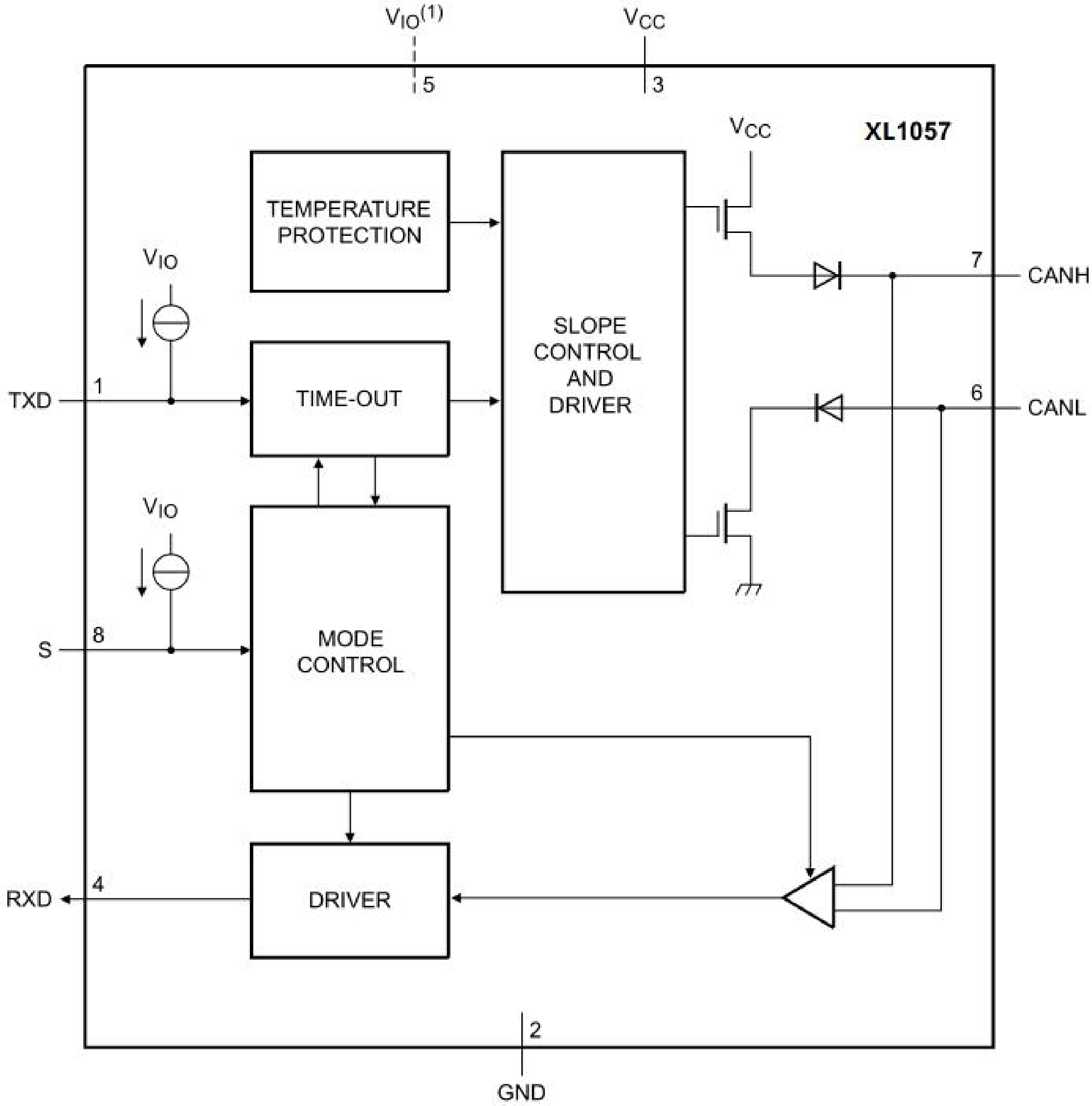


Figure 1. Block diagram

5. PINNING INFORMATION

5.1 Pinning

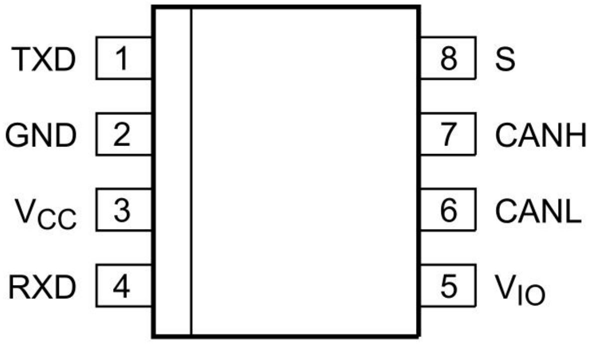


Figure 2. Pin configuration diagrams

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Type[1]	Description
TXD	1	I	transmit data input
GND	2	G	ground
V_{CC}	3	P	supply voltage
RXD	4	O	receive data output; reads out data from the bus lines
V_{IO}	5	P	supply voltage for I/O level adapter
CANL	6	AIO	LOW-level CAN bus line
CANH	7	AIO	HIGH-level CAN bus line
S	8	I	Silent mode control input

[1] I: digital input; O: digital output; AIO: analog input/output; P: power supply; G: ground.

6. FUNCTIONAL DESCRIPTION

6.1 Operating modes

The XL1057 supports two operating modes, Normal and Silent. The operating mode is selected via pin S. See Table 3 for a description of the operating modes under normal supply conditions.

Table 3. Operating modes

Mode	Inputs		Outputs	
	Pin S	Pin TXD	CAN driver	Pin RXD
Normal	LOW	LOW	dominant	LOW
		HIGH	recessive	LOW when bus dominant
				HIGH when bus recessive
Silent	HIGH	x[1]	biased to recessive	LOW when bus dominant
				HIGH when bus recessive

6.1.1 Normal mode

A LOW level on pin S selects Normal mode. In this mode, the transceiver can transmit and receive data via the bus lines, CANH and CANL (see Figure 1 for the block diagram). The differential receiver converts the analog data on the bus lines into digital data which is output on pin RXD. The slopes of the output signals on the bus lines are controlled internally and are optimized in a way that guarantees the lowest possible EME.

6.1.2 Silent mode

A HIGH level on pin S selects Silent mode. The transmitter is disabled in Silent mode, releasing the bus pins to recessive state. All other IC functions, including the receiver, continue to operate as in Normal mode. Silent mode can be used to prevent a faulty CAN controller disrupting all network communications.

6.2 Fail-safe features

6.2.1 TXD dominant time-out function

A 'TXD dominant time-out' timer is started when pin TXD is set LOW. If the LOW state on this pin persists for longer than tto(dom)TXD, the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when pin TXD is set HIGH.

6.2.2 Internal biasing of TXD and S input pins

Pins TXD and S have internal pull-ups to VIO to ensure a safe, defined state in case one or both of these pins are left floating. Pull-up currents flow in these pins in all states; both pins should be held HIGH in Silent mode to minimize supply current.

6.2.3 Undervoltage detection on pins VCC and VIO

If VCC or VIO drops below the undervoltage detection level, Vuvd(VCC)/Vuvd(VIO), the transceiver switches off and disengages from the bus (zero load; bus pins floating) until the supply voltage has recovered. The output drivers are enabled once both VCC and VIO are again within their operating ranges and TXD has been reset to HIGH.

6.2.5 Overtemperature protection

The output drivers are protected against overtemperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature, Tj(sd), the output drivers will be disabled until the virtual junction temperature falls below Tj(sd) and TXD becomes recessive again. Including the TXD condition ensures that output driver oscillation due to temperature drift is avoided.

6.3 VIO supply pin

Pin VIO on the XL1057GT/3 should be connected to the microcontroller supply voltage (see Figure 5). This will adjust the signal levels of pins TXD, RXD and STB to the I/O levels of the microcontroller. Pin VIO also provides the internal supply voltage for the low-power differential receiver of the transceiver. For applications running in low-power mode, this allows the bus lines to be monitored for activity even if there is no supply voltage on pin VCC.

7. LIMITING VALUES

Table 4. Limiting values

Symbol	Parameter	Conditions	Min	Max	Unit
V_x	voltage on pin x[1]	on pins CANH, CANL	-42	+42	V
		on pins V_{CC}, V_{IO}	-0.3	+7	V
		on any other pin	-0.3	V_{IO} +0.3	V
$V_{(CANH-CANL)}$	voltage between pin CANH and pin CANL		-27	+27	V
V_{trt}	transient voltage	on pins CANH, CANL			
		pulse 1	-100	-	V
		pulse 2a	-	75	V
		pulse 3a	-150	-	V
		pulse 3b	-	100	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (150 pF, 330 Ω discharge circuit)			
		on pins CANH and CANL	-8	+8	kV
		Human Body Model (HBM)			
		on any pin	-4	+4	kV
		on pins CANH and CANL	-8	+8	kV
		Machine Model (MM); 200 pF, 0.75 µH, 10 Ω			
		on any pin	-150	+150	V
		Charged Device Model (CDM)			
		on corner pins	-500	+500	V
		on any other pin	-300	+300	V
T_{vj}	virtual junction temperature		-40	+150	°C
T_{stg}	storage temperature		-55	+150	°C

[1] The device can sustain voltages up to the specified values over the product lifetime, provided applied voltages (including transients) never exceed these values.

[2] Maximum voltage should never exceed 7 V.

[3] Verified by an external test house according to IEC TS 62228, Section 4.2.4; parameters for standard pulses defined in ISO 7637.

[4] Verified by an external test house according to IEC TS 62228, Section 4.3.

[5] In accordance with IEC 60747-1. An alternative definition of virtual junction temperature is: $T_{vj} = T_{amb} + P \times R_{th(vj-a)}$, where $R_{th(vj-a)}$ is a fixed value to be used for the calculation of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).

[6] T_{stg} in application according to IEC61360-4. For component transport and storage conditions, see instead IEC61760-2.

8. THERMAL CHARACTERISTICS

Table 5. Thermal characteristics

Symbol	Parameter	Conditions[1]	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	SOP8 package; in free air	108	K/W
Ψ_{j-top}	thermal characterization parameter from junction to top of package	SOP8 package; in free air	20	K/W

9. STATIC CHARACTERISTICS

Table 6. Static characteristics

T_{vj} = -40 °C to +125°C; V_{CC} = 4.5 V to 5.25V; V_{IO} = 2.90 V to 5.25 V[1]; R_L = 60 Ω; C_L = 100 pF unless otherwise specified; all voltages are defined with respect to ground; positive currents flow into the IC.[2]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply; pin V_{CC}						
V_{CC}	supply voltage		4.5	-	5.5	V
$V_{uvd(VCC)}$	undervoltage detection voltage on pin V_{CC}		3.5	4	4.3	V
I_{CC}	supply current	Silent mode; V_{TXD} = V_{IO}	0.1	-	0.3	mA
		Normal mode				
		recessive; V_{TXD} = V_{IO}	2	5	10	mA
		dominant; V_{TXD} = 0 V	20	45	70	mA
		dominant; short circuit on bus lines; V_{TXD} = 0 V; -3 V < (V_{CANH} = V_{CANL}) < +18 V	2	80	110	mA
I/O level adapter supply; pin V_{IO} [1]						
V_{IO}	supply voltage on pin V_{IO}		2.90	-	5.5	V
$V_{uvd(VIO)}$	undervoltage detection voltage on pin V_{IO}		2.1	-	2.8	V
I_{IO}	supply current on pin V_{IO}	Silent mode	-	11	20	µA
		Normal mode				
		recessive; V_{TXD} = V_{IO}	-	7	30	µA
		dominant; V_{TXD} = 0 V	-	110	320	µA
Silent mode control input; pin S						
V_{IH}	HIGH-level input voltage		2	-	V_{IO} +0.3	V
V_{IL}	LOW-level input voltage		-0.3	-	0.8	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{IH}	HIGH-level input current	V_S = V_{IO}	-1	-	+1	µA
I_{IL}	LOW-level input current	V_S = 0 V	-15	-	-1	µA
CAN transmit data input; pin TXD						
V_{IH}	HIGH-level input voltage		2	-	V_{IO} +0.3	V
V_{IL}	LOW-level input voltage		-0.3	-	0.8	V
I_{IH}	HIGH-level input current	V_{TXD} = V_{IO}	-5	-	+5	µA
I_{IL}	LOW-level input current	V_{TXD} = 0 V	-260	-	-30	µA
C_i	input capacitance		-	5	10	pF
CAN receive data output; pin RXD						
I_{OH}	HIGH-level output current	V_{RXD} = V_{IO} - 0.4 V	-9	-3	-1	mA
I_{OL}	LOW-level output current	V_{RXD} = 0.4 V; bus dominant	1	-	12	mA
Bus lines; pins CANH and CANL						
$V_{O(dom)}$	dominant output voltage	V_{TXD} = 0 V; t < $t_{to(dom)TXD}$				

		pin CANH; R_L = 50 Ω to 65 Ω	2.75	3.5	4.5	V
		pin CANL; R_L = 50 Ω to 65 Ω	0.5	1.5	2.25	V
$V_{dom(TX)sym}$	transmitter dominant voltage symmetry	$V_{dom(TX)sym} = V_{CC} - V_{CANH} - V_{CANL}$	-500	-	+500	mV
V_{TXsym}	transmitter voltage symmetry	$V_{TXsym} = V_{CANH} + V_{CANL}$;	$0.9V_{CC}$	-	$1.1V_{CC}$	V
$V_{O(dif)}$	differential output voltage	dominant; V_{TXD} = 0 V; $t < t_{to(dom)TXD}$				
		R_L = 50 Ω to 65 Ω	1.3	-	3	V
		R_L = 45 Ω to 70 Ω	1.2	-	3.3	V
		R_L = 2240 Ω	1.3	-	5	V
		recessive; $V_{TXD} = V_{IO}$; no load	-100	-	+100	mV
$V_{O(rec)}$	recessive output voltage	no load VTXD = V_{IO}	2	$0.5V_{CC}$	3	V
$V_{th(RX)dif}$	differential receiver threshold voltage	Normal/Silent mode; -12 V ≤ V_{CANL} ≤ +12 V; -12 V ≤ V_{CANH} ≤ +12 V	0.5	-	0.9	V
$V_{rec(RX)}$	receiver recessive voltage	-12 V ≤ V_{CANL} ≤ +12 V; -12 V ≤ V_{CANH} ≤ +12 V				
		Normal/Silent mode	-4	-	0.5	V
$V_{dom(RX)}$	receiver dominant voltage	-12 V ≤ V_{CANL} ≤ +12 V; -12 V ≤ V_{CANH} ≤ +12 V				
		Normal/Silent mode	0.9	-	9.0	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{hys(RX)dif}$	differential receiver hysteresis voltage	Normal mode; -12 V ≤ V_{CANL} ≤ +12 V; -12 V v V_{CANH} ≤ +12 V	50	-	300	mV
$I_{O(sc)dom}$	dominant short-circuit output current	V_{TXD} = 0 V; $t < t_{to(dom)TXD}$; V_{CC} = 5 V				
		pin CANH; V_{CANH} = -15 V to +40 V	-100	-70	-	mA
		pin CANL; V_{CANL} = -15 V to +40 V	-	70	100	mA
$I_{O(sc)rec}$	recessive short-circuit output current	Normal mode; $V_{TXD} = V_{CC}$; $V_{CANH} = V_{CANL}$ = -27 V to +32 V	-5	-	+5	mA
I_L	leakage current	V_{CC} = 0 V or $V_{CC} = V_{IO}$ = shorted to ground via 47 kΩ; $V_{CANH} = V_{CANL}$ = 5 V	-5	-	+5	µA
R_i	input resistance	-2 V ≤ V_{CANL} ≤ +7 V; -2 V ≤ V_{CANH} ≤ +7 V	-	-	60	kΩ
ΔR_i	input resistance deviation	0 V ≤ V_{CANL} ≤ +5 V; 0 V ≤ V_{CANH} ≤ +5 V	-5	-	+5	%
$R_{i(dif)}$	differential input resistance	-2 V ≤ V_{CANL} ≤ +7 V; -2 V ≤ V_{CANH} ≤ +7 V	20	49	60	kΩ
$C_{i(cm)}$	common-mode input capacitance		-	-	20	pF
$C_{i(dif)}$	differential input capacitance		-	-	10	pF

Temperature detection						
$T_{j(sd)}$	shutdown junction temperature		-	185	-	℃

[1] Only the XL1057GT/3 variants have a V_{IO} pin

[2] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

[3] Undervoltage is detected between min and max values. Undervoltage is guaranteed to be detected below min value and guaranteed not to be detected above max value.

[4] Not tested in production; guaranteed by design.

[5] The test circuit used to measure the bus output voltage symmetry (which includes C_{SPLIT}) is shown in Figure 8.

10. DYNAMIC CHARACTERISTICS

Table 7. Dynamic characteristics

T_{vj} = −40 ℃ to +125 ℃; V_{CC} = 4.75 V to 5.25 V; V_{IO} = 2.9 V to 5.5 V[1]; R_L = 60 Ω unless specified otherwise. All voltages are defined with respect to ground. Positive currents flow into the IC.[2]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Transceiver timing; pins CANH, CANL, TXD and RXD; see Figure 3, Figure 4 and Figure 7						
$t_{d(TXD-busdom)}$	delay time from TXD to bus dominant	Normal mode	-	62	100	ns
$t_{d(TXD-busrec)}$	delay time from TXD to bus recessive	Normal mode	-	75	100	ns
$t_{d(busdom-RXD)}$	delay time from bus dominant to RXD	Normal mode	-	60	110	ns
$t_{d(busrec-RXD)}$	delay time from bus recessive to RXD	Normal mode	-	90	120	ns
$t_{d(TXDL-RXDL)}$	delay time from TXD LOW to RXD LOW	Normal mode	50	-	210	ns
$t_{d(TXDH-RXDH)}$	delay time from TXD HIGH to RXD HIGH	Normal mode	50	-	210	ns
$t_{bit(bus)}$	transmitted recessive bit width	$t_{bit(TXD)}$ = 500 ns	435	-	530	ns
		$t_{bit(TXD)}$ = 200 ns	155	-	210	ns
$t_{bit(RXD)}$	bit time on pin RXD	$t_{bit(TXD)}$ = 500 ns	400	-	550	ns
		$t_{bit(TXD)}$ = 200 ns	120	-	220	ns
Δt_{rec}	receiver timing symmetry	$t_{bit(TXD)}$ = 500 ns	-65	-	+40	ns
		$t_{bit(TXD)}$ = 200 ns	-45	-	+15	ns
$t_{to(dom)TXD}$	TXD dominant time-out time	V_{TXD} = 0 V; Normal mode[4]	0.8	2	8	ms

[1] Only the XL1057GT/3 variants have a V_{IO} pin

[2] All parameters are guaranteed over the junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range..

[3] See Figure 4.

[4] Time-out occurs between the min and max values. Time-out is guaranteed not to occur below the min value; time-out is guaranteed to occur above the max value.

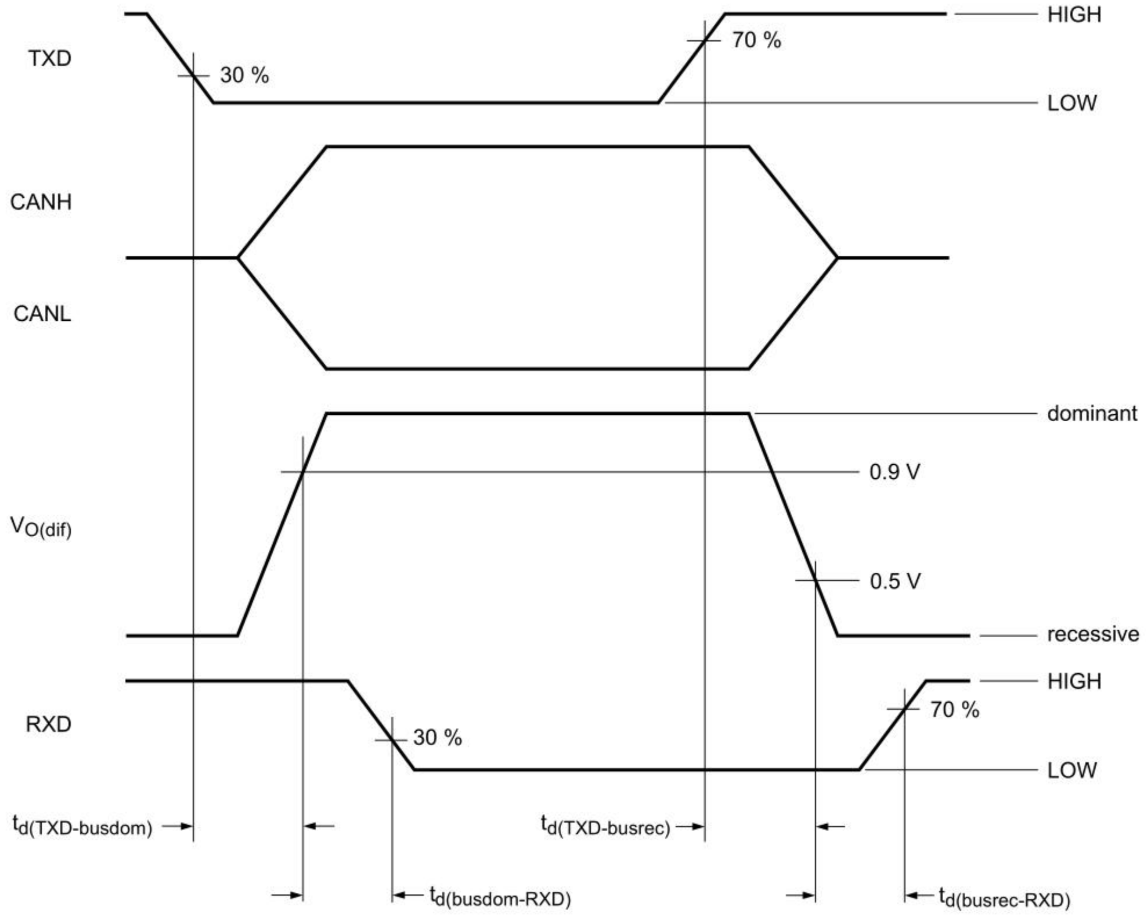


Figure 3. CAN transceiver timing diagram

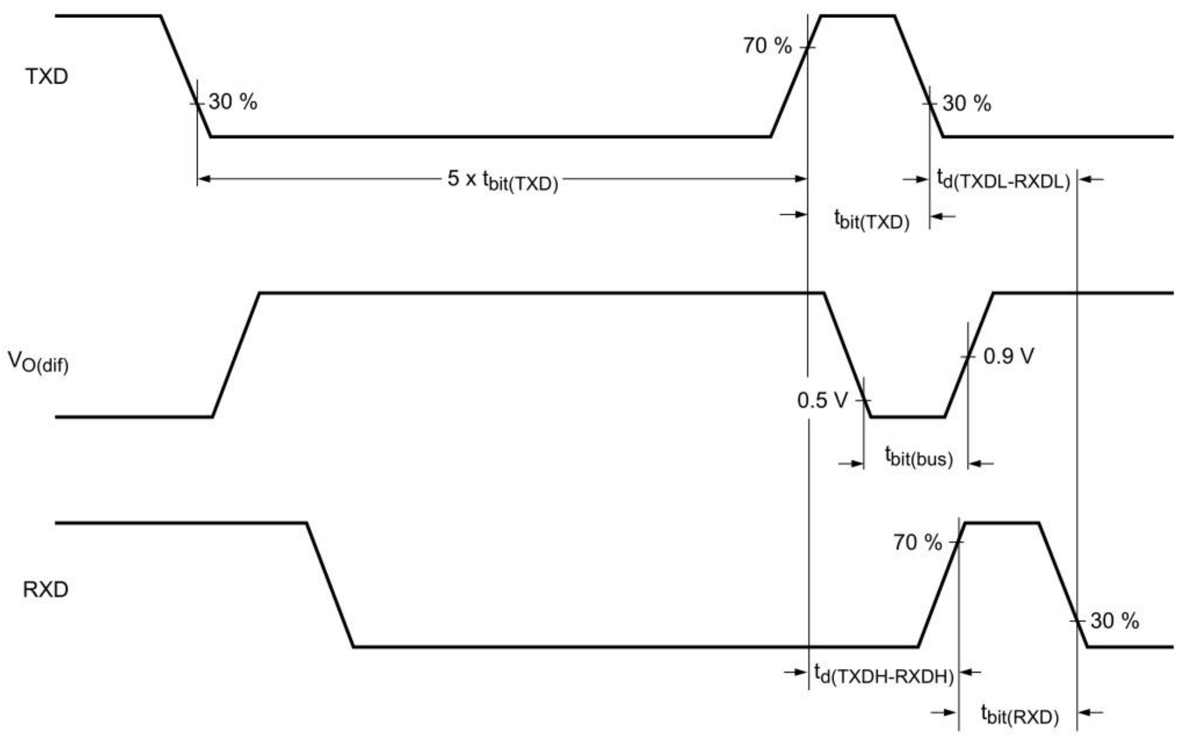


Figure 4. CAN FD timing definitions according to ISO 11898-2:2016

11. APPLICATION INFORMATION

11.1 Application diagrams

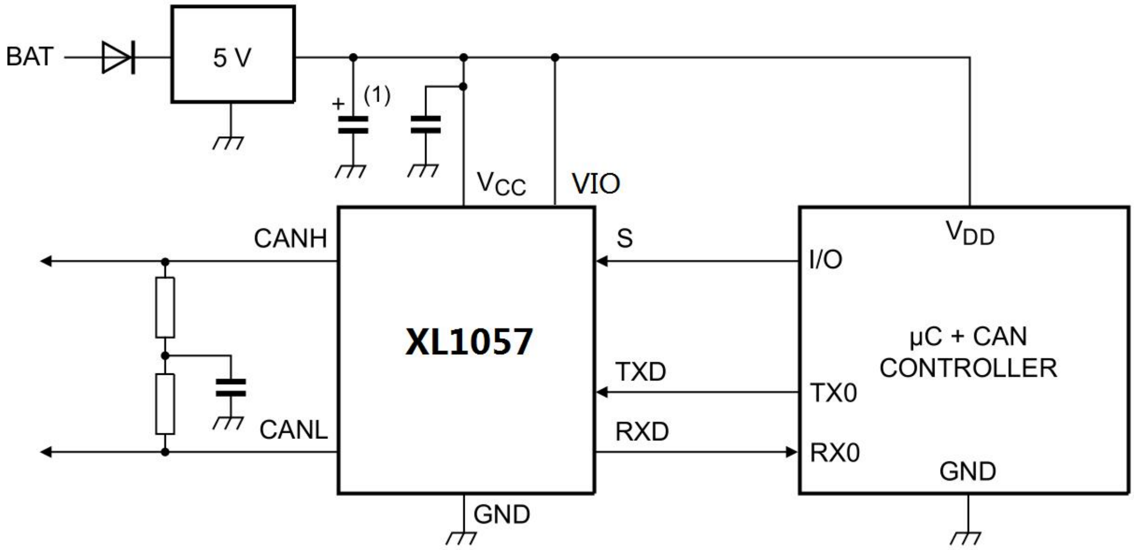


Figure 5. Typical XL1057 application with a 5 V microcontroller

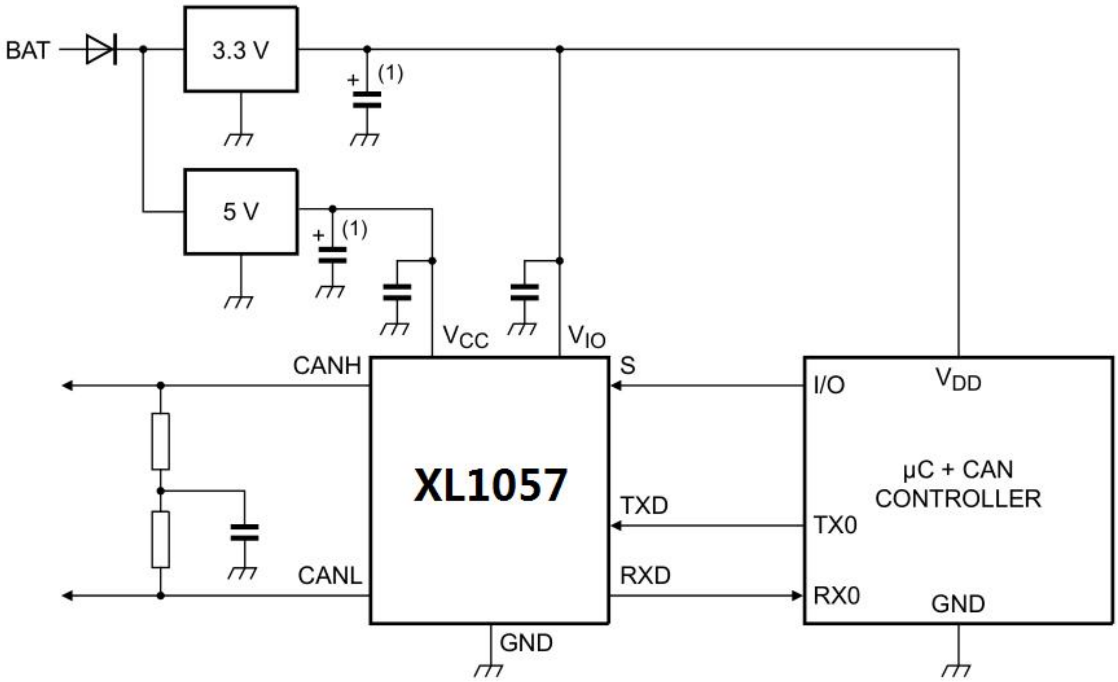


Figure 6. Typical XL1057 application with a 3.3 V microcontroller

12. TEST INFORMATION

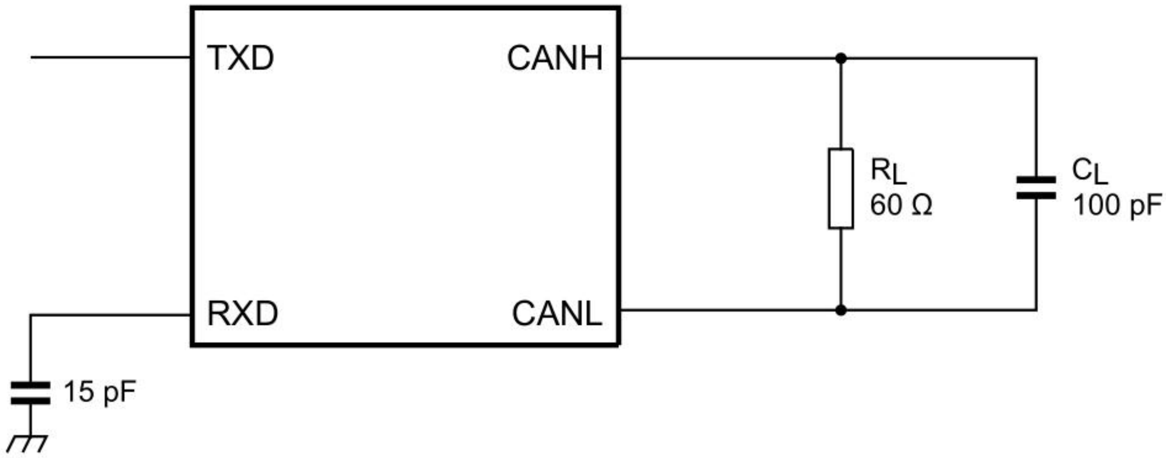


Figure 7. CAN transceiver timing test circuit

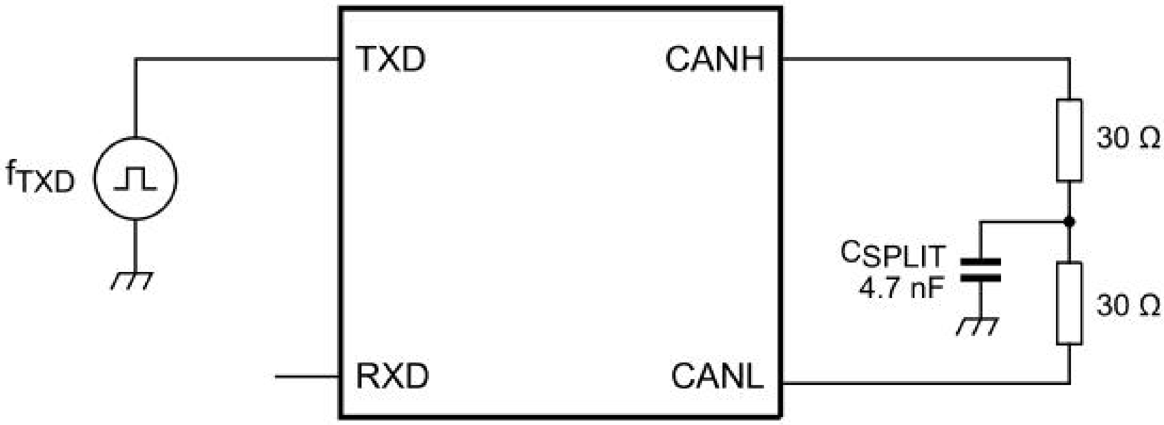


Figure 8. Test circuit for measuring transceiver driver symmetry

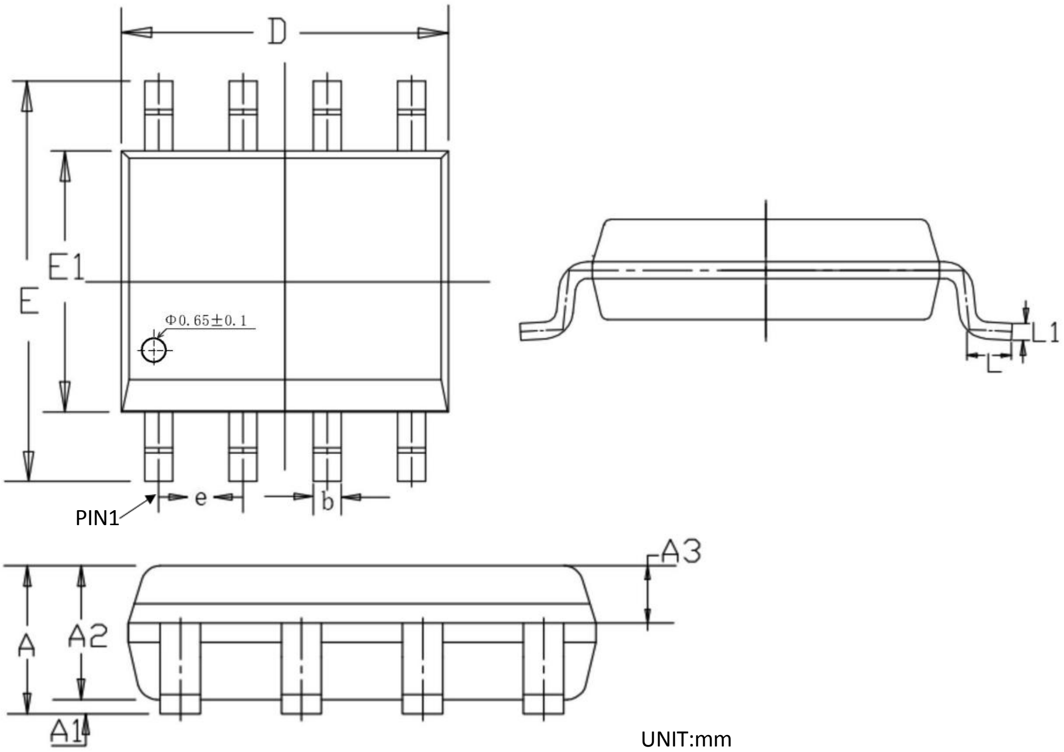
13. ORDERING INFORMATION

Ordering Information

Part Number	Device Marking	Package Type	Body size (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
XL1057GT/3	XL1057GT3	SOP8	4.90 * 3.90	-40 to +125	MSL3	T&R	2500

14. DIMENSIONAL DRAWINGS

SOP8



UNIT:mm

	MIN	NOM	MAX
A	1.450	1.550	1.650
A1	0.100	0.150	0.200
A2	1.300	1.400	1.500
A3	0.600	0.650	0.700
b	0.380	–	0.510
e	1.240	1.270	1.300
D	4.800	4.900	5.000
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
L	0.450	0.600	0.750
L1	—	0.25BSC	—

[if you need help contact us. Xinluda reserves the right to change the above information without prior notice]