



REALTEK

NOT FOR PUBLIC RELEASE

RTL8305NBI-VB-CG

SINGLE-CHIP 5-PORT 10/100M ETHERNET SWITCH CONTROLLER

DATASHEET

(CONFIDENTIAL: Development Partners Only)

Rev. 1.0

22 March 2022

Track ID: JATR-8275-15



Realtek Semiconductor Corp.

No. 2, Innovation Road II, Hsinchu Science Park, Hsinchu 300, Taiwan

Tel.: +886-3-578-0211. Fax: +886-3-577-6047

www.realtek.com

COPYRIGHT

©2022 Realtek Semiconductor Corp. All rights reserved. No part of this document may be reproduced, transmitted, transcribed, stored in a retrieval system, or translated into any language in any form or by any means without the written permission of Realtek Semiconductor Corp.

DISCLAIMER

Realtek provides this document ‘as is’, without warranty of any kind. Realtek may make improvements and/or changes in this document or in the product described in this document at any time. This document could include technical inaccuracies or typographical errors.

TRADEMARKS

Realtek is a trademark of Realtek Semiconductor Corporation. Other names mentioned in this document are trademarks/registered trademarks of their respective owners.

USING THIS DOCUMENT

This document is intended for the software engineer’s reference, and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

ELECTROSTATIC DISCHARGE (ESD) WARNING

This product can be damaged by Electrostatic Discharge (ESD). When handling, care must be taken. Damage due to inappropriate handling is not covered by warranty.

Do not open the protective conductive packaging until you have read the following, and are at an approved anti-static workstation.

- Use an approved anti-static mat to cover your work surface
- Use a conductive wrist strap attached to a good earth ground
- Always discharge yourself by touching a grounded bare metal surface or approved anti-static mat before picking up an ESD-sensitive electronic component
- If working on a prototyping board, use a soldering iron or station that is marked as ESD-safe
- Always disconnect the microcontroller from the prototyping board when it is being worked on

REVISION HISTORY

Revision	Release Date	Summary
1.0	2022/03/22	First release.

Table of Contents

1.	GENERAL DESCRIPTION	1
2.	FEATURES	2
3.	SYSTEM APPLICATIONS	3
4.	BLOCK DIAGRAM	4
5.	PIN ASSIGNMENTS	5
5.1.	PIN ASSIGNMENTS DIAGRAM	5
5.2.	PACKAGE IDENTIFICATION	5
5.3.	PIN ASSIGNMENTS TABLE	6
6.	PIN DESCRIPTIONS	7
6.1.	PIN ASSIGNMENT CODES	7
6.2.	MEDIA CONNECTION PINS	7
6.3.	MISCELLANEOUS PINS	8
6.4.	PORT LED PINS	8
6.5.	STRAPPING PINS	9
6.6.	REGULATOR PINS	9
6.7.	POWER AND GND PINS	9
7.	BASIC FUNCTION DESCRIPTIONS	10
7.1.	SWITCH CORE FUNCTION OVERVIEW	10
7.1.1.	<i>Flow Control</i>	10
7.1.1.1	IEEE 802.3x Full Duplex Flow Control	10
7.1.1.2	Half Duplex Back Pressure	10
7.1.2.	<i>Address Search, Learning, and Aging</i>	11
7.1.3.	<i>Half Duplex Operation</i>	11
7.1.4.	<i>InterFrame Gap</i>	11
7.1.5.	<i>Illegal Frame</i>	11
7.2.	PHYSICAL LAYER FUNCTIONAL OVERVIEW	12
7.2.1.	<i>Auto-Negotiation</i>	12
7.2.2.	<i>10Base-T Transmit Function</i>	12
7.2.3.	<i>10Base-T Receive Function</i>	12
7.2.4.	<i>Link Monitor</i>	12
7.2.5.	<i>100Base-TX Transmit Function</i>	12
7.2.6.	<i>100Base-TX Receive Function</i>	12
7.2.7.	<i>Power-Down Mode</i>	13
7.2.8.	<i>Crossover Detection and Auto Correction</i>	13
7.2.9.	<i>Polarity Detection and Correction</i>	13
7.3.	GENERAL FUNCTION OVERVIEW	14
7.3.1.	<i>Power-On Sequence</i>	14
7.3.2.	<i>Setup and Configuration</i>	15
7.3.3.	<i>Serial EEPROM Example</i>	16
7.3.3.1	EEPROM Device Operation	16
7.3.3.2	EEPROM Size Selection	18
7.3.4.	<i>SMI</i>	18
7.3.5.	<i>Head-Of-Line Blocking</i>	18
7.3.6.	<i>Filtering/Forwarding Reserved Control Frame</i>	19
7.3.7.	<i>Loop Detection</i>	19
7.3.8.	<i>Reg.0.14 PHY Digital Loopback Return to Internal</i>	21
7.3.9.	<i>LDO for 1.2V Power Generation</i>	22
7.3.10.	<i>Crystal/Oscillator</i>	22

8.	ADVANCED FUNCTION DESCRIPTIONS	23
8.1.	VLAN FUNCTION	23
8.1.1.	VLAN Description	23
8.1.2.	Port-Based VLAN	24
8.1.3.	IEEE 802.1Q Tagged-VID Based VLAN	24
8.1.4.	Insert/Remove/Replace Tag	24
8.1.5.	Ingress and Egress Rules	25
8.2.	IEEE 802.1P REMARKING FUNCTION	26
8.3.	QOS FUNCTION	27
8.3.1.	Bandwidth Control	27
8.3.1.1	Output (TX) Bandwidth Control	27
8.3.1.2	Input (RX) Bandwidth Control	28
8.3.2.	Priority Assignment	28
8.3.2.1	Queue Number Selection	28
8.3.2.2	Port-Based Priority Assignment	28
8.3.2.3	IEEE 802.1p/Q-Based Priority Assignment	29
8.3.2.4	DSCP-Based Priority Assignment	29
8.3.2.5	IP Address-Based Priority	29
8.3.2.6	Reassigned Priority	29
8.3.2.7	RLDP-Based Priority	29
8.3.2.8	Packet Priority Selection	29
8.4.	LOOKUP TABLE FUNCTION	31
8.4.1.	Function Description	31
8.4.2.	Address Search, Learning, and Aging	31
8.4.3.	Lookup Table Definition	32
8.5.	STORM FILTER FUNCTION	33
8.6.	INPUT AND OUTPUT DROP FUNCTION	33
8.7.	LED FUNCTION	34
8.8.	ENERGY-EFFICIENT ETHERNET (EEE)	35
8.9.	CABLE DIAGNOSIS	35
9.	CHARACTERISTICS	36
9.1.	ELECTRICAL CHARACTERISTICS/MAXIMUM RATINGS	36
9.2.	OPERATING RANGE	36
9.3.	DC CHARACTERISTICS	36
9.4.	THERMAL CHARACTERISTICS	37
9.4.1.	Simulation Conditions	37
9.4.2.	Thermal Characteristics Results	37
9.5.	DIGITAL TIMING CHARACTERISTICS	38
9.5.1.	LED Timing	38
9.5.2.	Reception/Transmission Data Timing of SMI Interface	38
9.5.3.	EEPROM Auto-Load Timing	39
10.	MECHANICAL DIMENSIONS	40
10.1.	MECHANICAL DIMENSIONS NOTES	40
11.	ORDERING INFORMATION	41

List of Tables

TABLE 1. PIN ASSIGNMENTS TABLE	6
TABLE 2. MEDIA CONNECTION PINS.....	7
TABLE 3. MISCELLANEOUS PINS	8
TABLE 4. PORT LED PINS.....	8
TABLE 5. STRAPPING PINS	9
TABLE 6. REGULATOR PINS	9
TABLE 7. POWER AND GND PINS	9
TABLE 8. BASIC SMI READ/WRITE CYCLES.....	18
TABLE 9. EXTENDED SMI MANAGEMENT FRAME FORMAT	18
TABLE 10. RESERVED ETHERNET MULTICAST ADDRESSES.....	19
TABLE 11. LOOP FRAME FORMAT	20
TABLE 12. CRYSTAL AND OSCILLATOR REQUIREMENTS.....	22
TABLE 13. VLAN TABLE.....	23
TABLE 14. VLAN ENTRY	23
TABLE 15. L2 TABLE 4-WAY HASH INDEX METHOD	32
TABLE 16. ELECTRICAL CHARACTERISTICS/MAXIMUM RATINGS	36
TABLE 17. OPERATING RANGE.....	36
TABLE 18. DC CHARACTERISTICS.....	36
TABLE 19. PCB DESCRIPTIONS	37
TABLE 20. CONDITION DESCRIPTIONS	37
TABLE 21. THERMAL CHARACTERISTICS RESULTS	37
TABLE 22. LED TIMING	38
TABLE 23. SMI TIMING.....	38
TABLE 24. EEPROM AUTO-LOAD TIMING CHARACTERISTICS	39
TABLE 25. ORDERING INFORMATION	41

List of Figures

FIGURE 1. BLOCK DIAGRAM.....	4
FIGURE 2. PIN ASSIGNMENTS	5
FIGURE 3. COLLISION-BASED BACKPRESSURE SIGNAL TIMING.....	10
FIGURE 4. POWER-ON SEQUENCE.....	14
FIGURE 5. RESET	15
FIGURE 6. START AND STOP DEFINITION	17
FIGURE 7. OUTPUT ACKNOWLEDGE	17
FIGURE 8. RANDOM READ	17
FIGURE 9. SEQUENTIAL READ	17
FIGURE 10. LOOP EXAMPLE	19
FIGURE 11. LED AND BUZZER CONTROL SIGNAL FOR LOOP DETECTION	20
FIGURE 12. LOOP EXAMPLE 2	21
FIGURE 13. REG. 0.14 LOOPBACK	21
FIGURE 14. PACKET-SCHEDULING DIAGRAM.....	27
FIGURE 15. RTL8305NBI-VB PRIORITY ASSIGNMENT DIAGRAM.....	28
FIGURE 16. BROADCAST INPUT DROP VS. OUTPUT DROP.....	33
FIGURE 17. MULTICAST INPUT DROP VS. OUTPUT DROP	33
FIGURE 18. FLOATING AND PULL-HIGH OF LED PINS FOR LED	34
FIGURE 19. RECEPTION DATA TIMING OF SMI INTERFACE	38
FIGURE 20. TRANSMISSION DATA TIMING OF SMI INTERFACE	38
FIGURE 21. EEPROM AUTO-LOAD TIMING.....	39

1. General Description

The RTL8305NBI-VB is a 5-port 10/100M Ethernet switch controller that integrates memory, five MACs, and five physical layer transceivers for 10Base-T and 100Base-TX operation into a single chip.

In order to accomplish diagnostics in complex network systems, the RTL8305NBI-VB provides a loopback feature in each port.

The RTL8305NBI-VB supports several advanced QoS functions with four-level priority queues to improve multimedia or real-time networking applications, including:

- Multi-priority assignment
- Differential queue weight
- Port-based rate limitation
- Queue-based rate limitation

The RTL8305NBI-VB supports 16 VLAN groups. These can be configured as port-based VLANs and/or 802.1Q tag-based VLANs. The RTL8305NBI-VB also supports VLAN learning, with four Independent VLAN Learning (IVL) filtering databases.

The RTL8305NBI-VB contains a 2K-entry address lookup table. A 4-way associative hash algorithm avoids hash collisions and maintains forwarding performance.

Maximum packet length can be 2048 bytes. Three types of independent storm filter are provided to filter packet storms, and an intelligent switch engine prevents Head-of-Line blocking problems.

The RTL8305NBI-VB supports Energy-Efficient Ethernet mode (EEE; defined in IEEE 802.3az) to minimize system power consumption. Energy-Efficient Ethernet (EEE) supports Low Power Idle Mode. When Low Power Idle Mode is enabled, systems on both sides of the link can disable portions of the functionality and save power during periods of low link utilization.

To simplify the peripheral power circuit, the RTL8305NBI-VB integrates one LDO regulator to generate 1.2V from a 3.3V input power, and needs only one external diode.

2. Features

Basic Switching Functions

- 5-port switch controller with memory and transceiver for 10Base-T and 100Base-TX
- Non-blocking wire-speed reception and transmission and non-head-of-line-blocking forwarding
- Complies with IEEE 802.3/802.3u auto-negotiation
- Built-in high efficiency SRAM for packet buffer, with 2K-entry lookup table and two 4-way associative hash algorithms
- 2048 byte maximum packet length
- Flow control fully supported
 - ◆ Half duplex: Back pressure flow control
 - ◆ Full duplex: IEEE 802.3x flow control

Service Quality

- Supports high performance QoS function on each port
 - ◆ Supports 4-level priority queues
 - ◆ Weighted round robin service
 - ◆ Supports strict priority
 - ◆ Input/Output port bandwidth control
 - ◆ Queue-based bandwidth control
 - ◆ 1Q-based, Port-based, DSCP-based, IP address-based, and other types of priority assignments
- Supports IEEE 802.1p Traffic Remarking

Security and Management

- Supports reserved control frame filtering
- Supports advanced storm filtering
- Optional EEPROM interface for configuration

VLAN Functions

- Supports up to 16 VLAN groups
- Flexible 802.1Q port/tag-based VLAN
- Supports four IVLs
- Leaky VLAN for unicast/multicast/broadcast/ARP packets

Power Saving Functions

- Supports Energy-Efficient Ethernet (EEE) function (IEEE 802.3az)
- Link Down Power Saving Mode

Diagnostic Functions

- Supports hardware loop detection function with LEDs and buzzer to indicate the existence of a loop
- Supports cable diagnosis (RTCT function)
- Flexible LED indicators
 - ◆ RTCT status indication
 - ◆ Loop status indication
 - ◆ LEDs blink upon reset for LED diagnostics

Other Features

- Optional MDI/MDIX auto crossover for plug-and-play
- Physical layer port Polarity Detection and Correction function
- Robust baseline wander correction for improved 100Base-TX performance
- 25MHz crystal or 3.3V OSC input
- Single 3.3V power input can be transformed by integrating an LDO regulator to generate 1.2V from 3.3V via a low-cost external diode
- Low power, 1.2/3.3V, 55nm CMOS technology
- 48-pin QFN ‘Green’ package

3. System Applications

- 5-port switch (10Base-T & 100Base-TX)

4. Block Diagram

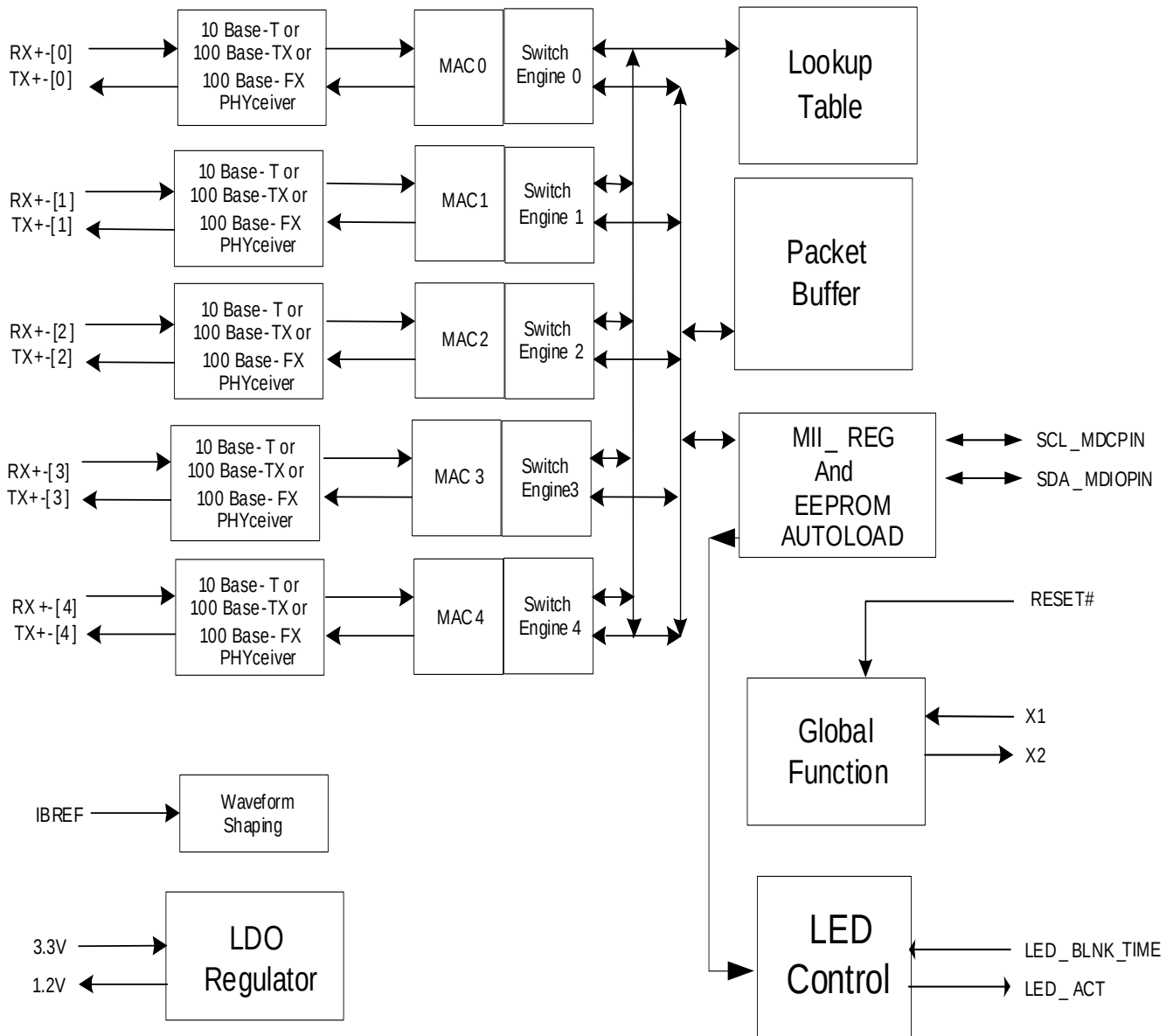


Figure 1. Block Diagram

5. Pin Assignments

5.1. Pin Assignments Diagram

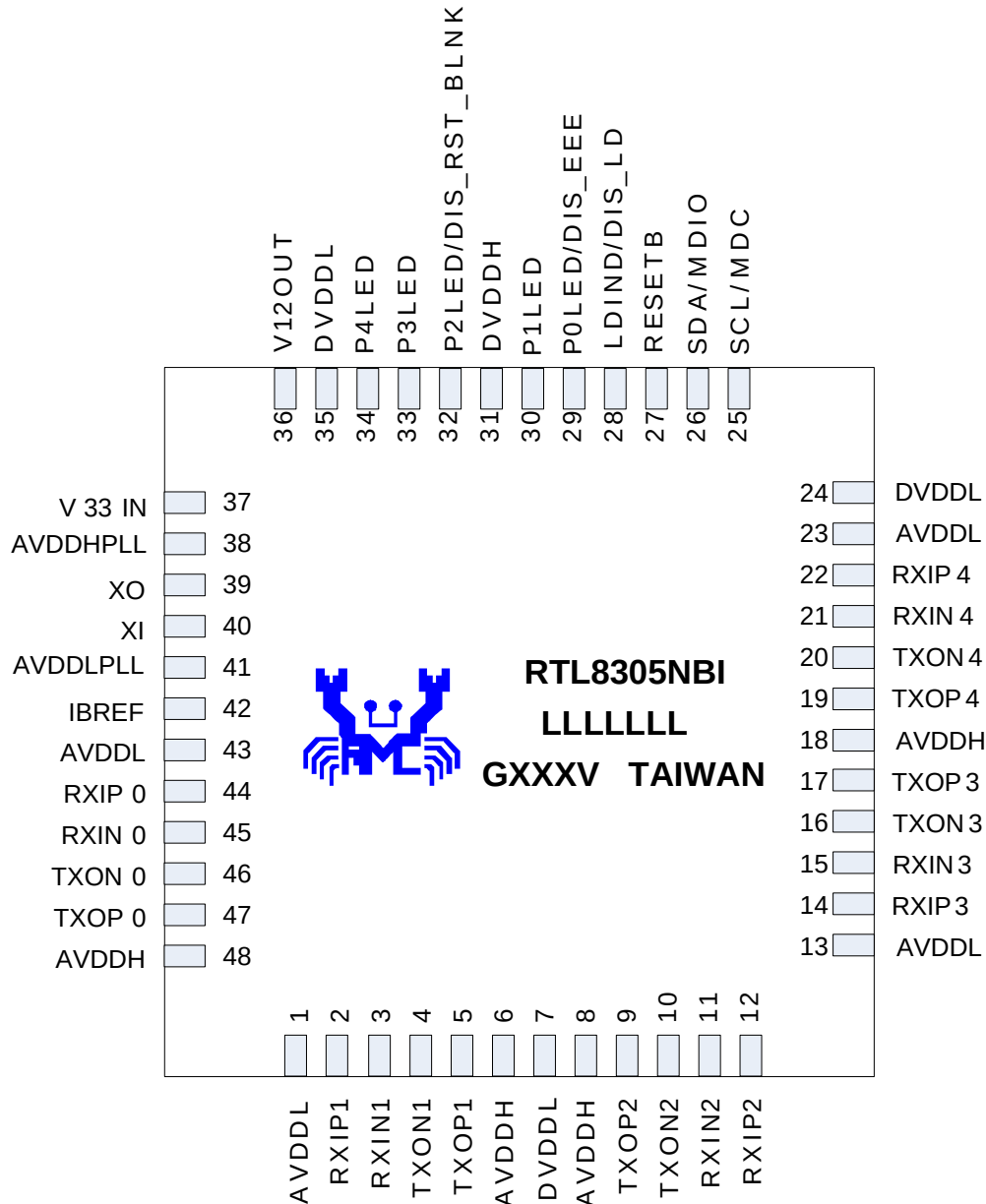


Figure 2. Pin Assignments

5.2. Package Identification

Green package is indicated by a ‘G’ in the location marked ‘GXXXV’ in Figure 2. The ‘V’ location indicates the version.

5.3. Pin Assignments Table

‘Type’ codes used in the following table: A=Analog, D=Digital, I=Input, O=Output, I/O=Input/Output, I_{PU}=Input Pin with Pull-Up Resistor, I_{PD}=Input Pin with Pull-Down Resistor.

Table 1. Pin Assignments Table

Name	Pin No.	Type	Name	Pin No.	Type
AVDDL	1	AP	SDA/MDIO	26	I/O _{PU}
RXIP1	2	AI/O	RESETB	27	I _{PU}
RXIN1	3	AI/O	LDIND/DIS_LD	28	I/O _{PU}
TXON1	4	AI/O	P0LED/DIS_EEE	29	I/O _{PD}
TXOP1	5	AI/O	P1LED	30	I/O _{PD}
AVDDH	6	AP	DVDDH	31	P
DVDDL	7	P	P2LED/DIS_RST_BLNK	32	I/O _{PD}
AVDDH	8	P	P3LED	33	I/O _{PD}
TXOP2	9	AI/O	P4LED	34	I/O _{PD}
TXON2	10	AI/O	DVDDL	35	P
RXIN2	11	AI/O	V12OUT	36	AO
RXIP2	12	AI/O	V33IN	37	AP
AVDDL	13	AP	AVDDHPLL	38	AP
RXIP3	14	AI/O	XO	39	AO
RXIN3	15	AI/O	XI	40	AI
TXON3	16	AI/O	AVDDLPLL	41	AP
TXOP3	17	AI/O	IBREF	42	AO
AVDDH	18	AP	AVDDL	43	AP
TXOP4	19	AI/O	RXIP0	44	AI/O
TXON4	20	AI/O	RXIN0	45	AI/O
RXIN4	21	AI/O	TXON0	46	AI/O
RXIP4	22	AI/O	TXOP0	47	AI/O
AVDDL	23	AP	AVDDH	48	AP
DVDDL	24	P	E-PAD	E-PAD	G
SCL/MDC	25	I/O _{PU}			

6. Pin Descriptions

6.1. Pin Assignment Codes

I:	Input Pin	AI:	Analog Input Pin
O:	Output Pin	AO:	Analog Output Pin
I/O:	Bi-Directional Input/Output Pin	AI/O:	Analog Bi-Directional Input/Output Pin
P:	Digital Power Pin	AP:	Analog Power Pin
G:	Digital Ground Pin	AG:	Analog Ground Pin
I _{PU} :	Input Pin With Pull-Up Resistor; (Typical Value is about 75KΩ)	O _{PU} :	Output Pin With Pull-Up Resistor; (Typical Value is about 75KΩ)
I _{PD} :	Input Pin With Pull-Down Resistor; (Typical Value is about 75KΩ)	O _{PD} :	Output Pin With Pull-Down Resistor; (Typical Value is about 75KΩ)
I/O _{PU} :	I _{PU} and O _{PU}	I/O _{PD} :	I _{PD} and O _{PD}

6.2. Media Connection Pins

Table 2. Media Connection Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
RXIP4/RXIN4 RXIP3/RXIN3 RXIP2/RXIN2 RXIP1/RXIN1 RXIP0/RXIN0	22, 21 14, 15 12, 11 2, 3 44, 45	AI/O	-	Differential Receive Data Input. Port0~4 support 10Base-T, 100Base-TX.
TXOP4/TXON4 TXOP3/TXON3 TXOP2/TXON2 TXOP1/TXON1 TXOP0/TXON0	19, 20 17, 16 9, 10 5, 4 47, 46	AI/O	-	Differential Transmit Data Output. Port0~4 support 10Base-T, 100Base-TX.

6.3. Miscellaneous Pins

As the output of the RTL8305NBI-VB is 3.3V, the serial EEPROM and external device must be 3.3V compatible.

Table 3. Miscellaneous Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
LDIND/DIS_LD	28	I/OPU	10	Loop Indication Used by LED and Buzzer.
SCL/MDC	25	I/OPU	4	I2C Interface Clock for EEPROM Auto Load when Power On. After power on, this pin is MDC/MDIO Interface Clock for access registers.
SDA/MDIO	26	I/OPU	4	I2C Interface Data Input/Output for EEPROM Auto Load when Power On. After power on, this pin is MDC/MDIO Interface Data Input/Output for access registers.
RESETB	27	IPU	-	System Pin Reset Input.
XI	40	AI	-	25MHz Crystal Clock Input. The clock tolerance is ± 50 ppm.
XO	39	AO	-	25MHz Crystal Clock Output Pin. When the pin of XI is using an oscillator, this pin should be floating.
IBREF	42	AO	-	Reference Resistor for PHY Bandgap. A 2.49K Ω (1%) resistor should be connected between IBREF and GND.

6.4. Port LED Pins

P0~P2 LED0 statuses are represented as active-low or high depending on input strapping.

P0~P2 LED0 pins that are dual-function pins are output for LED, or input for strapping. Below are LED descriptions only.

P3 LED0 and P4 LED0 statuses are represented as active-high only.

Table 4. Port LED Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
P0LED/DIS_EEE	29	I/OPD	10	LED for Port0 Status Indication.
P1LED	30	I/OPD	10	LED for Port1 Status Indication.
P2LED/DIS_RST_BLNK	32	I/OPD	10	LED for Port2 Status Indication.
P3LED	33	OPD	10	LED for Port3 Status Indication.
P4LED	34	OPD	10	LED for Port4 Status Indication.

6.5. Strapping Pins

Pins that are dual function pins are outputs for LED or inputs for strapping. Below are strapping descriptions only.

Table 5. Strapping Pins

Pin Name	Pin No.	Type	Default	Description
DIS_LD/LDIND	28	I/O _{PU}	-	Disable Loop Detection Function. 0: Enable 1: Disable (default)
DIS_EEE/P0LED	29	I/O _{PD}	-	Disable EEE Function. 0: Enable EEE function (default) 1: Disable EEE function
DIS_RST_BLNK/ P2LED	32	I/O _{PD}	-	Disable LED Power on Blinking. 0: Enable (default) 1: Disable

6.6. Regulator Pins

Table 6. Regulator Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
V12OUT	36	AO	-	Switch Regulator 1.2V Output.
V33IN	37	AP	-	Switch Regulator 3.3V Input.

6.7. Power and GND Pins

Table 7. Power and GND Pins

Pin Name	Pin No.	Type	Description
AVDDH	6, 8, 18, 48	AP	Analog Power 3.3V.
AVDDL	1, 13, 23, 43	AP	Analog Power 1.2V.
AVDDHPLL	38	AP	Power 3.3V for PLL.
AVDDLPLL	41	AP	Power 1.2V for PLL.
DVDDH	31	P	Digital Power 3.3V for IO Pin.
DVDDL	7, 24, 35	P	Digital Power 1.2V for Core Voltage.
GND	E-PAD	G	Ground for Whole Chip.

7. Basic Function Descriptions

7.1. Switch Core Function Overview

7.1.1. Flow Control

The RTL8305NBI-VB supports IEEE 802.3x full duplex flow control, force mode full duplex flow control, and optional half duplex backpressure.

7.1.1.1 IEEE 802.3x Full Duplex Flow Control

For UTP with auto-negotiation ability, the pause ability of full duplex flow control is enabled by internal registers via SMI on a per-port basis after reset. IEEE 802.3x flow control's ability is auto-negotiated between the remote device and the RTL8305NBI-VB. If the auto-negotiation result of the IEEE 802.3x pause ability is 'Enabled', the full duplex 802.3x flow control function is enabled. Otherwise, full duplex IEEE 802.3x flow control function is disabled.

7.1.1.2 Half Duplex Back Pressure

There are two mechanisms for half duplex backpressure; collision-based or carrier-based.

Collision-Based Backpressure (Jam Mode)

If the buffer is ready to overflow, this mechanism will force a collision. When the link partner detects this collision, the transmission is rescheduled.

The Reschedule procedure is:

- The RTL8305NBI-VB will drive TXEN to high and send the preamble; SFD and a 4-byte Jam signal (pattern is 0xAA). The RTL8305NBI-VB will then drive TXEN to low
- When the link partner receives the Jam signal, it will feedback a 4-byte signal (pattern is CRC^0x01), it will then drive RXDV to low
- The link partner waits for a random back-off time then re-sends the packet. The timing is shown in Figure 3

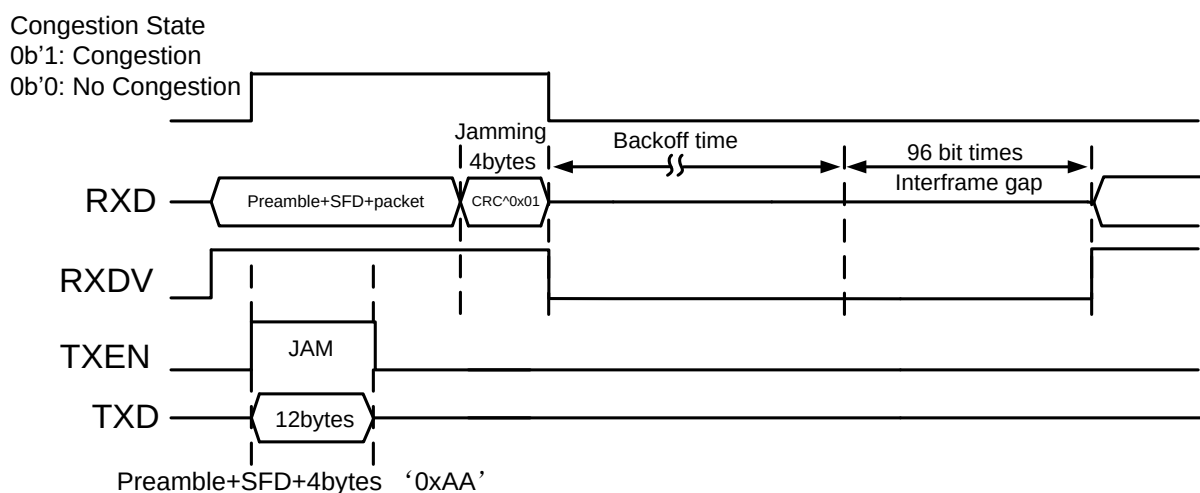


Figure 3. Collision-Based Backpressure Signal Timing

Carrier-Based Backpressure (Defer Mode)

If the buffer is about to overflow, this mechanism will send an 0xAA pattern to defer the other station's transmission. The RTL8305NBI-VB will continuously send the defer signal until the buffer overflow is resolved.

7.1.2. Address Search, Learning, and Aging

When a packet is received, the RTL8305NBI-VB will use the destination MAC address and FID to index the 2048-entry lookup table. If the indexed entry is valid, the received packet will be forwarded to the corresponding destination port. Otherwise, the RTL8305NBI-VB will broadcast the packet. This is the 'Address Search'.

The RTL8305NBI-VB then combines the source MAC address and the FID to index the 2048-entry lookup table. If the entry is not in the table, it will record the source MAC address and add switching information. If this is an occupied entry, it will update the entry with new information when LRU is enabled. This is called 'Learning'.

Address aging is used to keep the contents of the address table correct in a dynamic network topology. The lookup engine will update the time stamp information of an entry whenever the corresponding source MAC address appears. An entry will be invalid (aged-out) if its time stamp information is not refreshed by the address learning process during the aging time period. The aging time of the RTL8305NBI-VB is between 200 and 400 seconds.

7.1.3. Half Duplex Operation

In half duplex mode, the CSMA/CD media access method is the means by which two or more stations share a common transmission medium. To transmit, a station waits (defers) for a quiet period on the medium (that is, no other station is transmitting) and then sends the intended message in bit-serial form. If the message collides with that of another station, then each transmitting station intentionally transmits for an additional predefined period to ensure propagation of the collision throughout the system. The station remains silent for a random amount of time (backoff) before attempting to transmit again.

When a transmission attempt has terminated due to a collision, it is retried until it is successful. A controlled randomization process called 'truncated binary exponential backoff' determines the scheduling of the retransmissions. At the end of enforcing a collision (jamming), the switch delays before attempting to retransmit the frame. The delay is an integer multiple of slot time (512 bit times). The number of slot times to delay before the n^{th} retransmission attempt is chosen as a uniformly distributed random integer 'r' in the range:

$$0 \leq r < 2^k$$

where:

$k = \min(n, \text{backoffLimit})$. IEEE 802.3 defines the backoffLimit as 10.

7.1.4. InterFrame Gap

The InterFrame Gap is 9.6μs for 10Mbps Ethernet and 960ns for 100Mbps Fast Ethernet.

7.1.5. Illegal Frame

Illegal frames such as CRC error packets, runt packets (length < 64 bytes), and oversize packets (length > maximum length) will be discarded.

7.2. *Physical Layer Functional Overview*

7.2.1. Auto-Negotiation

The RTL8305NBI-VB obtains the states of duplex, speed, and flow control ability for each port through the auto-negotiation mechanism defined in the IEEE 802.3 specifications. During auto-negotiation, each port advertises its ability to its link partner and compares its ability with advertisements received from its link partner. By default, the RTL8305NBI-VB advertises full capabilities (100Full, 100Half, 10Full, 10Half) together with flow control ability. The RTL8305NBI-VB also advertises the Energy Efficient Ethernet (EEE) capability to the link partner.

7.2.2. 10Base-T Transmit Function

The output 10Base-T waveform is Manchester-encoded before it is driven onto the network media. The internal filter shapes the driven signals to reduce EMI emissions, eliminating the need for an external filter.

7.2.3. 10Base-T Receive Function

The Manchester decoder converts the incoming serial stream to NRZ data when the squelch circuit detects the signal level is above squelch level.

7.2.4. Link Monitor

The 10Base-T link pulse detection circuit continually monitors the RXIP/RXIN pins for the presence of valid link pulses. Auto-polarity is implemented to correct the detected reverse polarity of RXIP/RXIN signal pairs.

7.2.5. 100Base-TX Transmit Function

The 100Base-TX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ/NRZI conversion, and MLT-3 encoding. The 5-bit serial data stream after 4B/5B coding is then scrambled as defined by the TP-PMD Stream Cipher function to flatten the power spectrum energy such that EMI effects are significantly reduced.

The scrambled seed is based on PHY addresses and is unique for each port. After scrambling, the bit stream is driven into the network media in the form of MLT-3 signaling. The MLT-3 multi-level signaling technology moves the power spectrum energy from high frequency to low frequency, which further reduces EMI emissions.

7.2.6. 100Base-TX Receive Function

The receive path includes a receiver composed of an adaptive equalizer and DC restoration circuits (to compensate for an incoming distorted MLT-3 signal), an MLT-3 to NRZI and NRZI to NRZ converter to convert analog signals to digital bit-stream, and a PLL circuit to clock data bits with minimum bit error rate. A De-scrambler, 5B/4B decoder, and serial-to-parallel conversion circuits are followed by the PLL circuit. Finally, the converted parallel data is fed into the MAC.

7.2.7. Power-Down Mode

The RTL8305NBI-VB implements power-down mode on a per-port basis. Setting MII Reg.0.11 forces the corresponding port of the RTL8305NBI-VB to enter power-down mode. This disables all transmit/receive functions, except SMI (Serial Management Interface: MDC/MDIO, also known as MII Management Interface).

7.2.8. Crossover Detection and Auto Correction

During the link setup phase, the RTL8305NBI-VB checks whether it receives active signals on every port in order to determine if a connection can be established. In cases where the receiver data pin pair is connected to the transmitter data pin pair of the peer device and vice versa, the RTL8305NBI-VB automatically changes its configuration and swaps receiver/transmitter data pins as required. If a port is connected to a PC or NIC with MDI-X interface with a crossover cable, the RTL8305NBI-VB will reconfigure the port to ensure proper connection. This replaces the DIP switch commonly used for reconfiguring a port on a hub or switch.

Note: IEEE 802.3 compliant forced mode 100M ports with Autoxover have link problems with NWay (Auto-Negotiation) ports. It is recommended to not use Autoxover for forced 100M.

7.2.9. Polarity Detection and Correction

For better noise immunity and lower interference to ambient devices, the Ethernet electrical signal on a twisted-pair cable is transmitted in differential form. That is, the signal is transmitted on two wires in each direction with inverse polarities (+/-). If wiring on the connector is faulty, or a faulty transformer is used, the two inputs to a transceiver may carry signals with opposite but incorrect polarities. As a direct consequence, the transceiver will not work properly.

When the RTL8305NBI-VB operates in 10Base-T mode, it automatically reverses the polarity of its two receiver input pins if it detects that the polarities of the incoming signals on the pins is incorrect. However, this feature is unnecessary when the RTL8305NBI-VB is operating in 100Base-TX mode.

7.3. General Function Overview

7.3.1. Power-On Sequence

Two power voltage types are required for RTL8305NBI-VB's normal operation, 3.3V and 1.2V. The 1.2V is converted from 3.3V via the LDO of the RTL8305NBI-VB.

- Ta is the moment when 3.3V power is higher than 2.6V ($\pm 5\%$). 3.3V power never falls lower than 2.6V ($\pm 5\%$) after Ta
- Tb is the moment when 1.2V power is higher than 0.9V ($\pm 10\%$). 1.2V power never falls lower than 0.9V ($\pm 10\%$) after Tb
- Tc is the moment when both 3.3V and 1.2V power are stable (the voltage is always in the legal operating range)
- Td is the moment that the pin reset signal is de-asserted
- Te is the moment that the RTL8305NBI-VB device is ready to be accessed by an external CPU

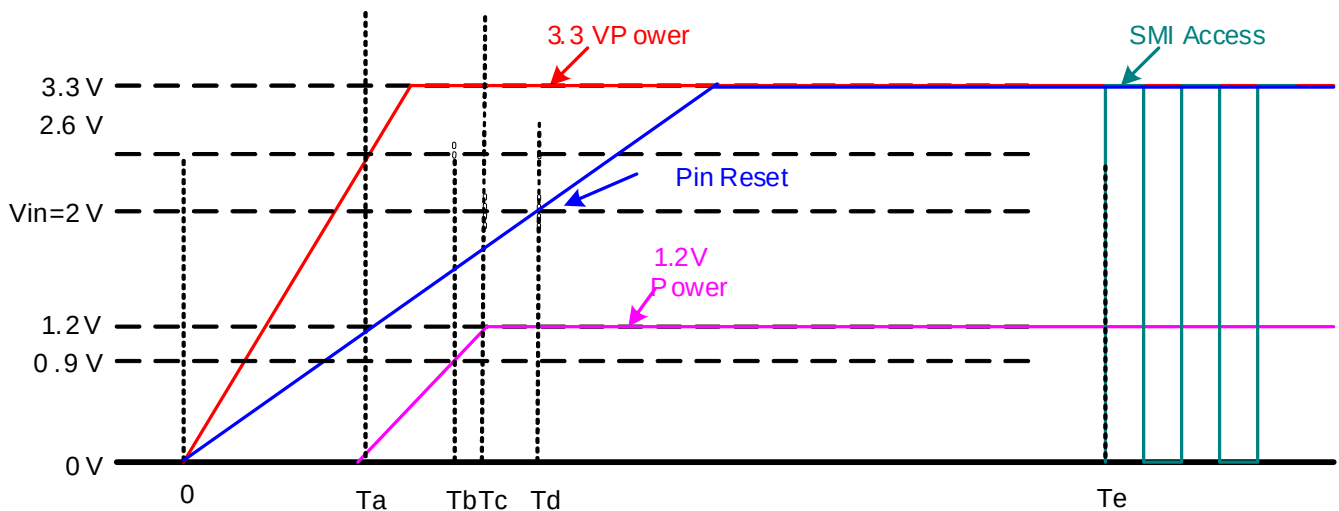


Figure 4. Power-On Sequence

The requirements are:

- The time of Ta should be between 500 μ s and 20ms
- The sequence of Ta is always less than Tb for the LDO of the RTL8305NBI-VB. In principle, the sequence of Td and Ta/Tb/Tc is also not required. The sequence of Td > 5ms is recommended
- The time from Te to the later of Ta/Tb/Td is the sum of the time of the EEPROM loading + 30ms. The EEPROM loading time varies according to the autoloading data bytes in the serial EEPROM
- Reset

Depending on the type of reset, the whole or just part of the RTL8305NBI-VB is initialized. There are several ways to reset the RTL8305NBI-VB.

- Hardware reset for the whole chip via pin RESET# or power-on
- Soft reset for packet buffer, queue, and MIB counter via register SoftReset
- PHY software reset for each PHY by register reset

Hardware Reset: Power-on, or pull the RESET# pin low for at least 1 μ s. The RTL8305NBI-VB resets the whole chip and after all power is ready and the RESET# pin is de-asserted, it gets initial values from pins and serial EEPROM.

Soft Reset: The RTL8305NBI-VB does not reset the LUT, LED circuit, and all registers, and does not load data from serial EEPROM and pins to registers. The packet buffer, queue, and MIB counter will be reset. After changing the queue number via SMI (Serial Management Interface), the external device must perform a soft reset in order to update the configuration.

PHY Software Reset: Write bit15 of Reg0 of a PHY as 1. The RTL8305NBI-VB will then reset this PHY.

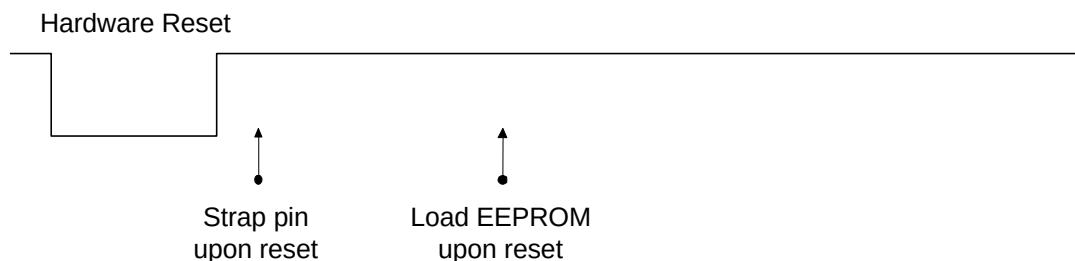


Figure 5. Reset

Some setting values for operation modes are latched from those corresponding mode pins upon hardware reset. ‘Upon reset’ is defined as a short time after the end of a hardware reset. Other advanced configuration parameters may be latched from serial EEPROM.

7.3.2. Setup and Configuration

The RTL8305NBI-VB can be configured easily and flexibly by:

- Hardware pins upon reset
- Optional serial EEPROM upon reset (contact Realtek for detailed EEPROM configuration settings)
- Internal registers (including PHY registers for each port and global MAC registers) accessed via SMI (Serial Management Interface: MDC/MDIO, also known as MII Management Interface)

There are three methods of configuration:

- Only hardware pins for normal switch applications
- Hardware pins and serial EEPROM for advanced switch applications
- Hardware pins and internal registers via SMI for applications with processor

Two types of pins, each with internal pull-high or pull-low resistors, are used for configuration:

- Input/Output pins used for strapping upon reset and used as output pins after reset
- Input/Output pins used for strapping upon reset and used as LED indicator pins after reset. The LED statuses are represented as active-low or high depending on input strapping

Pins with default value=0 are internal pull-low and use I/O pads. They can be left floating to set the input value as low, but should not be connected to VDD without a pull-high resistor.

The serial EEPROM shares two pins with SMI, SCL/MDC and SDA/MDIO, and is optional for advanced configuration. SCL/MDC and SDA/MDIO are tri-state during hardware reset (pin RESET#=0). The RTL8305NBI-VB will try to automatically find the serial EEPROM upon reset.

Internal registers can still be accessed after reset via SMI (pin SCL/MDC and SDA/MDIO). Serial EEPROM signals and SMI signals must not exist at the same time.

7.3.3. Serial EEPROM Example

Both the 24LC01/02/04/08/16 and 24C01/02/04/08/16 can be used with the RTL8305NBI-VB. The interface is a 2-wire serial EEPROM interface providing 1K/2K/4K/8K/16K bits of storage space. The EEPROM must be 3.3V compatible.

7.3.3.1 EEPROM Device Operation

Clock and Data Transitions: The SDA pin is normally pulled high with an external resistor. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods will indicate a start or stop condition as defined below. The SCL frequency is 200kHz.

Start Condition

A high-to-low transition of SDA with SCL high is the start condition and must precede any other command.

Stop Condition

A low-to-high transition of SDA with SCL high is a stop condition.

Acknowledge

All addresses and data are transmitted serially to and from the EEPROM in 8-bit words. The EEPROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

Random Read

A random read requires a ‘dummy’ byte write sequence to load in the data word address.

Sequential Read

For the RTL8305NBI-VB, the sequential reads are initiated by a random address read. After the EEPROM receives a data word, it responds with an acknowledgement. As long as the EEPROM receives an acknowledgement, it will continue to increment the data word address and clock out sequential data words in series.

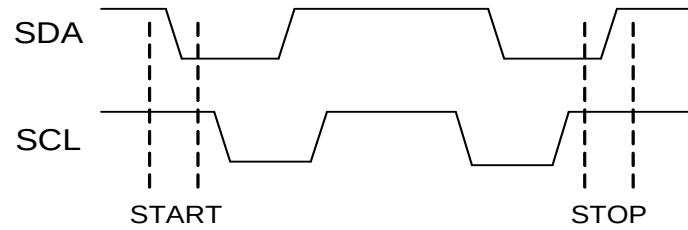


Figure 6. Start and Stop Definition

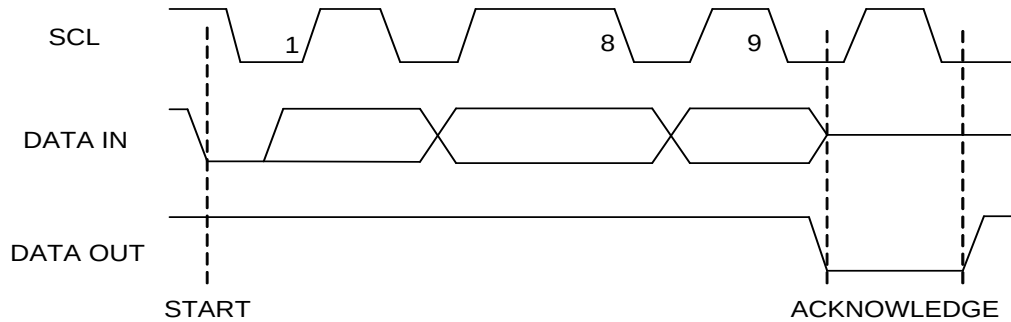


Figure 7. Output Acknowledge

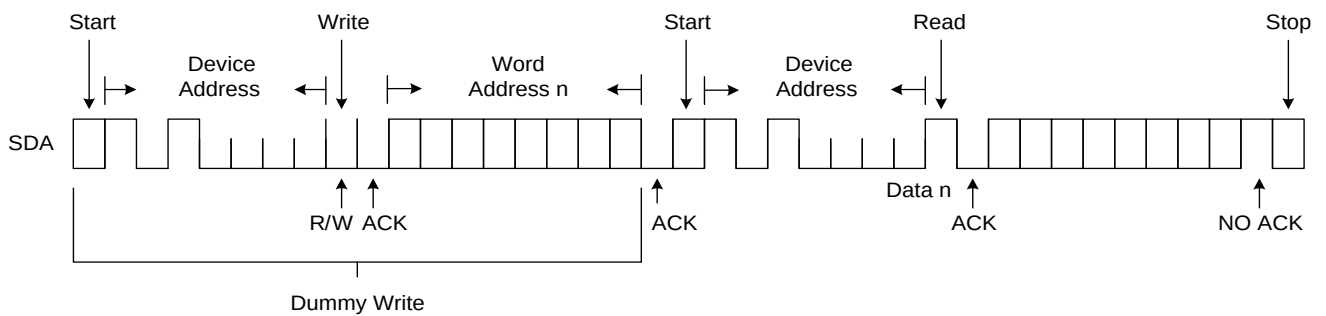


Figure 8. Random Read

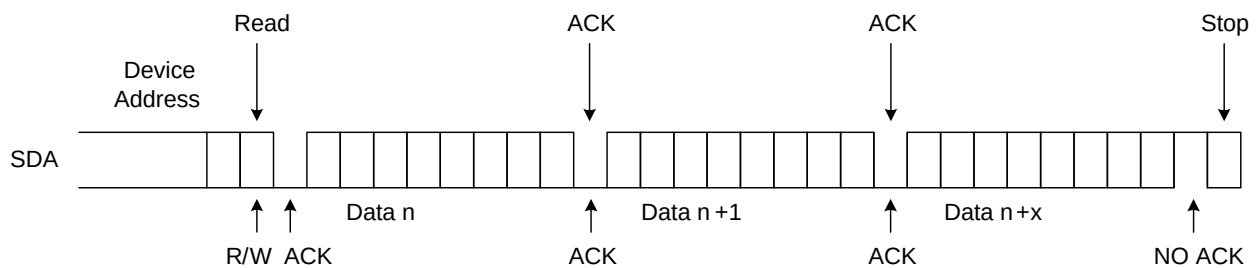


Figure 9. Sequential Read

7.3.3.2 EEPROM Size Selection

The RTL8305NBI-VB supports five serial EEPROM sizes —1k bits, 2k bits, 4k bits, 8k bits and 16k bits. Via the auto-download operation, the RTL8305NBI-VB decides the size of the data downloaded to the RTL8305NBI-VB from the EEPROM according to the value of the 2nd byte data in the serial EEPROM.

If the 2nd byte data = 0x01, 0x02, 0x04, 0x08 or 0x16, it means the data size is 1k bits, 2k bits, 4k bits, 8k bits or 16k bits respectively. The value of the 2nd byte should accord with the actual EEPROM data size. For example, the value of the 2nd byte cannot be ‘0x02’ when the 24(L)C02 is used.

7.3.4. SMI

The SMI (Serial Management Interface) is also known as the MII Management Interface, and consists of two signals (MDIO and MDC). It allows external devices with SMI master mode (MDC is output) to control the state of the PHY and internal registers (SMI slave mode: MDC is input). MDC is an input clock for the RTL8305NBI-VB to latch MDIO on its rising edge. The clock can run from DC to 2.5MHz. MDIO is a bi-directional connection used to write data to, or read data from the RTL8305NBI-VB. The PHY address is from 0 to 4.

Table 8. Basic SMI Read/Write Cycles

	Preamble (32 bits)	Start (2 bits)	OP Code (2 bits)	PHYAD (5 bits)	REGAD (5 bits)	Turn Around (2 bits)	Data (16 bits)	Idle
Read	1.....1	01	10	A ₄ A ₃ A ₂ A ₁ A ₀	R ₄ R ₃ R ₂ R ₁ R ₀	Z0	D ₁₅D ₀	Z*
Write	1.....1	01	01	A ₄ A ₃ A ₂ A ₁ A ₀	R ₄ R ₃ R ₂ R ₁ R ₀	10	D ₁₅D ₀	Z*

*Note: High-impedance. During idle time MDIO state is determined by an external 1.5K Ω pull-up resistor.

For MDIO Manageable Device (MMD) access, the RTL8305NBI-VB supports the extended SMI format.

Table 9. Extended SMI Management Frame Format

Frame	PRE	ST	OP	PHYAD	DEVAD	TA	DATA	IDLE
Address	1...1	00	00	AAAAA	EEEEEE	10	AAAAAAAAAAAAAAAAAAAA	Z
Write	1...1	00	01	AAAAA	EEEEEE	10	DDDDDDDDDDDDDDDDDDDD	Z
Read	1...1	00	11	AAAAA	EEEEEE	Z0	DDDDDDDDDDDDDDDDDDDD	Z
Post-Read-Increment-Address	1...1	00	10	AAAAA	EEEEEE	Z0	DDDDDDDDDDDDDDDDDDDD	Z

To guarantee the first successful SMI transaction after a power-on reset, the external device should delay a few moments before issuing the first SMI Read/Write Cycle relative to the rising edge of reset.

7.3.5. Head-Of-Line Blocking

The RTL8305NBI-VB incorporates a mechanism to prevent Head-Of-Line blocking problems when flow control is disabled. When the flow control function is disabled, the RTL8305NBI-VB first checks the destination address of the incoming packet. If the destination port is congested, the RTL8305NBI-VB will discard this packet to avoid blocking the next packet, which is going to a non-congested port.

7.3.6. Filtering/Forwarding Reserved Control Frame

The RTL8305NBI-VB supports the ability to forward or drop the frames of the IEEE 802.1 specified reserved Ethernet multicast addresses.

Table 10. Reserved Ethernet Multicast Addresses

B: Broadcast (Search the Look-Up Table) D: Drop

Assignment	Value	Available Action
Bridge Group Address	01-80-C2-00-00-00	D, B (Default)
IEEE Std 802.3, 1988 Edition, Full Duplex PAUSE Operation	01-80-C2-00-00-01	D (Default), B
IEEE 802.3ad Slow_Protocols-Multicast Address	01-80-C2-00-00-02	D (Default), B
IEEE 802.1X PAE Address	01-80-C2-00-00-03	D, B (Default)
Reserved for Future Standards	01-80-C2-00-00-04~01-80-C2-00-00-0D, 01-80-C2-00-00-0F	D (Default), B
LLDP IEEE Std 802.1AB Link Layer Discovery Protocol Multicast Address	01-80-C2-00-00-0E	D, B (Default)
All LANs Bridge Management Group Address	01-80-C2-00-00-10	D (Default), B
Reserved for 01-80-C2-00-00-1x	01-80-C2-00-00-11~01-80-C2-00-00-1F	D, B (Default)
GMRP Address	01-80-C2-00-00-20	D (Default), B
GVRP Address	01-80-C2-00-00-21	D, B (Default)
Reserved for use by Multiple Registration Protocol (MRP) Applications	01-80-C2-00-00-22~01-80-C2-00-00-2F	D (Default), B
802.1ag PDU CCM/LTM	01-80-C2-00-00-31~ 01-80-C2-00-00-3F	D, B (Default)

7.3.7. Loop Detection

Loops should be avoided between switch applications. The simplest loop as shown below results in: 1) Unicast frame duplication; 2) Broadcast frame multiplication; 3) Address table non-convergence. Frames are transmitted from Switch1 to Switch2 via Link1, and then returned to Switch1 via Link 2.

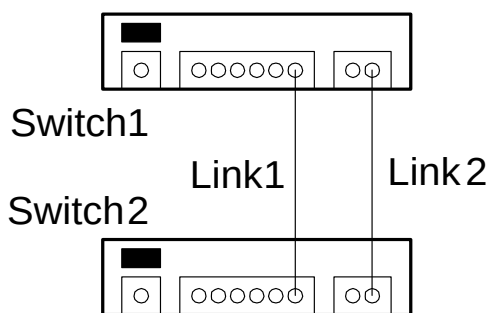


Figure 10. Loop Example

The loop detect function can be enabled/disabled via strapping pin or registers. When the loop detection function is enabled, the RTL8305NBI-VB sends out a broadcast 64-byte loop frame (the frequency is configured by register) and sniffs for the sent loop frame on each port to detect whether there is a network loop (or bridge loop). If a loop is detected, the RTL8305NBI-VB will drive the external LEDs and buzzer alarm.

- The LED driven by the LDIND pin will blink
- The LEDs driven by port LED pins (see Table 4, page 8) of the ports on which the network loop is detected will all blink simultaneously
- The buzzer driven by the LDIND pin will buzz at the same frequency as the LED blinking

Both passive and active buzzers can be supported. The resonant frequency for the passive buzzer is approximately 2kHz. The buzzer and all LEDs will turn on/off simultaneously. In Figure 11, T1 is the turned-off period and T2 is the turned-on period. T1 and T2 are equal and can be configured to 400ms or 800ms.

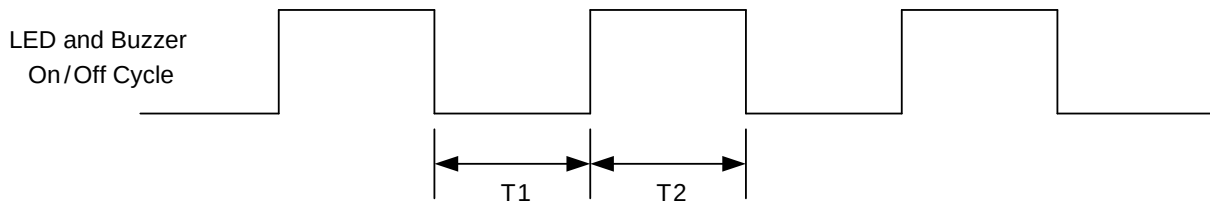


Figure 11. LED and Buzzer Control Signal for Loop Detection

Loop status, LED, and buzzer indications can be cleared when one of the following conditions occurs:

- Loop frame is not detected in the next loop detection period
- The loop port links down

The Loop frame length is 64 bytes. Its format is shown below.

Table 11. Loop Frame Format

48-Bit	48-Bit	16-Bit	16-Bit	12-Bit	4-Bit	32-Bit	16-Bit
FFFF FFFF FFFF	SID	8899	2300	000	TTL	0000	CRC

In order to achieve loop detection, each switch device needs a unique SID (the source MAC address). If an EEPROM is not used, a unique SID should be assigned via SMI after reset. The TTL (Time-To-Live) field is used to avoid a storm triggered by the loop frame. The TTL field in the loop frame will decrease by 1 when it passes through an RTL8305NBI-VB whose MAC address is not equal to the SID of the loop frame. The RTL8305NBI-VB will drop a loop frame in which the TTL is the minimum value (0001 is the minimum value. 0000, meaning 16, is the maximum value). The initial value of the TTL field can be configured via SMI or EEPROM.

In Figure 12, device A, B, and C are in a loop. Device D connects to device B. Device D generates a loop frame with an initial TTL value of 3, and then sends to device B. When the loop frame arrives at device C, the TTL value decreases to 2. It turns to 1 when the loop frame is transmitted to device A, and then the loop frame is dropped by the device A. If device D generates loop frames without the TTL mechanism, the loop frames will cause a storm in the loop of devices A, B, and C. The RTL8305NBI-VB provides an option to assign high priority to loop frames to reduce the possibility of erroneous loop frame dropping, and thereby enhance loop detection.

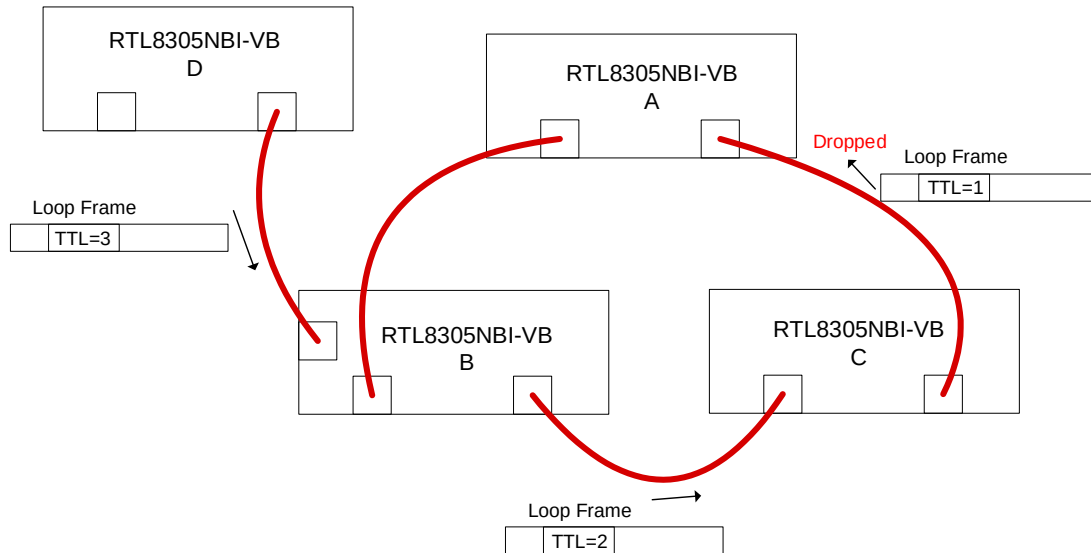


Figure 12. Loop Example 2

7.3.8. Reg.0.14 PHY Digital Loopback Return to Internal

The digital loopback mode of the PHY (return to internal MAC) may be enabled on a per-port basis by setting MII Reg.0.14 to 1. In digital loopback mode, the TXD of the PHY is transferred directly to the RXD of the PHY, with TXEN changed to CRS_DV, and returns to the MAC via an internal MII. The data stream coming from the MAC will not egress to the physical medium, and an incoming data stream from the network medium will be blocked in this mode. The packets will be looped back in 10Mbps full duplex or 100Mbps full duplex mode. This function is especially useful for diagnostic purposes. For example, a NIC can be used to send broadcast frames into Port 0 of the RTL8305NBI-VB and set Port 1 to Reg0.14 Loopback. The frame will be looped back to Port 0, so the received packet count can be checked to verify that the switch device is good. In this example, Port 0 can be 10M or 100M, and full or half duplex.

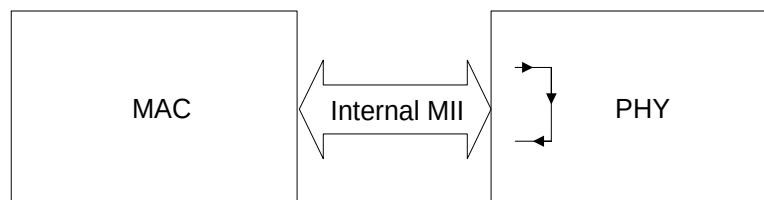


Figure 13. Reg. 0.14 Loopback

As the RTL8305NBI-VB only supports digital loopback in full duplex mode, PHY Reg.0.8 for each port will always be kept on 1 when digital loopback is enabled. The digital loopback only functions on broadcast packets (DA=FF-FF-FF-FF-FF-FF). In loopback mode, the link LED of the loopback port should always be ON, and the Speed and Duplex LED combined to reflect the link status (100full/10full) correctly, regardless of what the previous status of this loopback port was.

7.3.9. LDO for 1.2V Power Generation

The RTL8305NBI-VB can use an internal LDO to generate 1.2V from a 3.3V power supply. This 1.2V is used for the digital core and analog receiver circuits. Do not use the LDO for other chips, even if the rating is enough.

Do not connect an inductor (bead) directly between the V12OUT pin and AVDDLPLL pin. This will adversely affect the stability of the 1.2V power to a significant degree. Refer to the reference design for details.

7.3.10. Crystal/Oscillator

When using a crystal, the RTL8305NBI-VB should connect a loading capacitor from each pin of XI and XO to ground. Whether using an oscillator or driving an external 25MHz clock from another device, the external clock should be fed into the XI pin. The following table shows the requirements of the crystal and oscillator.

Table 12. Crystal and Oscillator Requirements

Nominal Frequency	25.000 MHz
Frequency Tolerance	±50ppm Max.
Temperature Characteristics	±50ppm in Operating Temperature Range
Equivalent Series Resistance of Crystal	30 Ohm Max.
XTALI/OSC Input Clock Jitter Tolerance (in 5KHz to 2.5MHz Range)	250ps Max.
Duty Cycle	40%~60%

8. Advanced Function Descriptions

8.1. VLAN Function

8.1.1. VLAN Description

The RTL8305NBI-VB supports 16 VLAN groups via the 16-entry VLAN table (see Table 13 and Table 14). These can be configured as port-based VLANs and/or IEEE 802.1Q tag-based VLANs. The RTL8305NBI-VB supports four IVLs, with the mapping information in the VLAN table. The contents of the VLAN table can be configured via SMI or EEPROM. Multiple ingress filtering and egress filtering options provide various VLAN admit rules for the RTL8305NBI-VB. The RTL8305NBI-VB also provides a flexible VLAN tag insert/remove function based on port and VID.

Table 13. VLAN Table

Entry Index	VLAN ID	Membership	UNTAG_MSK	FID
VLAN Entry 0	VLAN ID A[11:0]	VLAN ID A membership [4:0]	VLAN ID A UNTAG_MSK [4:0]	FID[1:0]
VLAN Entry 1	VLAN ID B [11:0]	VLAN ID B membership [4:0]	VLAN ID B UNTAG_MSK [4:0]	FID[1:0]
.....				
VLAN Entry 15	VLAN ID P [11:0]	VLAN ID P membership [4:0]	VLAN ID P UNTAG_MSK [4:0]	FID[1:0]

Table 14. VLAN Entry

Field	Description	Bits
VID	The VLAN ID for Search. The VID of the ingress packet will be compared with this field.	12
MBR	VLAN Member Port Set. If the bit in this field is '1', the corresponding port is a member port of the VLAN specified by the VID field.	6
UNTAG SET	VLAN Untag Set. If the bit in this field is '1', egress packets from the corresponding port will be VLAN-untagged.	6
PRIORITY	VID-Based Priority. The priority assigned to all ingress packets of the VLAN specified by the VID field.	2
FID	The FID is Used by Lookup Table for IVL Application.	12

The main VLAN features of the RTL8305NBI-VB are as follows:

- Supports up to 16 VLAN groups
- Flexible IEEE 802.1Q port/tag-based VLAN
- Four IVLs
- Leaky VLAN for ARP broadcast/unicast/multicast packets
- Leaky inter-VLAN mirror function
- VLAN tag Insert/Remove function

8.1.2. Port-Based VLAN

The 16 VLAN membership registers designed into the RTL8305NBI-VB provide full flexibility for users to configure the member ports to associate with different VLAN groups in the VLAN table. Each port can join more than one VLAN group.

Port-based VLAN mapping is the simplest implicit mapping rule. Each ingress packet is assigned to a VLAN group based on the input port. It is not necessary to parse and inspect frames in real-time to determine their VLAN association. All the packets received on a given input port will be forwarded to this port's VLAN members. The RTL8305NBI-VB supports VLAN indexes for each port to individually index this port to one of the 16 VLAN membership registers. A port that is not included in a VLAN's member set cannot transmit packets to this VLAN.

For non-VLAN tagged frames, the RTL8305NBI-VB performs port-based VLAN. The VLAN ID associated with the port-based VLAN index setting is the Port VID (PVID) of this port. The VLAN tag with the ingress port's PVID can be inserted (or replace the VID with a PVID for VLAN-tagged packets) into the packet on egress. The RTL8305NBI-VB also provides an option to admit VLAN tagged packets with a specific PVID only. When IEEE 802.1Q tag-aware VLAN is enabled, the VLAN tag admit control and non-PVID discard are enabled at the same time. Non-tagged packets and packets with an incorrect PVID will be RTL8305NBI-VB.

The RTL8305NBI-VB supports Port VID (PVID) for each port and can insert a PVID in the VLAN tag on egress. The PVID in the inserted (or replaced) VLAN tag on egress can indicate the source port of the packet. Using this function, VID information carried in the VLAN tag will be changed to PVID. The RTL8305NBI-VB also provides an option to admit VLAN tagged packets with a specific PVID only. If this function is enabled, it will drop non-tagged packets and packets with an incorrect PVID.

8.1.3. IEEE 802.1Q Tagged-VID Based VLAN

The RTL8305NBI-VB supports 16 VLAN entries to perform IEEE 802.1Q-tagged VID-based VLAN mapping. The RTL8305NBI-VB uses a 12-bit explicit identifier in the VLAN tag to associate received packets with a VLAN. If the VID of a VLAN-tagged frame does not match any of the 16 VLAN entries, the RTL8305NBI-VB will drop the frame. Otherwise, the RTL8305NBI-VB compares the explicit identifier in the VLAN tag with the 16 VLAN IDs to determine the VLAN association of this packet, and then forwards this packet to the member set of this VLAN.

Two VIDs are reserved for special purposes; one of them is all 1's, which is reserved and currently unused. The other is all 0's, which indicates a priority tag. A priority-tagged frame should be treated as an untagged frame.

When '802.1Q tag aware VLAN' is enabled, the RTL8305NBI-VB performs 802.1Q tag-based VLAN mapping for tagged frames, but still performs port-based VLAN mapping for untagged frames. If '802.1Q tag aware VLAN' is disabled, the RTL8305NBI-VB performs only port-based VLAN mapping both on non-tagged and tagged frames.

8.1.4. Insert/Remove/Replace Tag

The RTL8305NBI-VB supports the VLAN Insertion/Removal/replacing action for each port. The 802.1Q VLAN tags can be inserted, removed, or replaced based on the port's setting.

8.1.5. Ingress and Egress Rules

The RTL8305NBI-VB provides flexible VLAN ingress and egress rules to permit comprehensive traffic control. The RTL8305NBI-VB can filter packets on ingress according to the tag condition of the packet. For a normalized VLAN application and VLAN translation application, each of the RTL8305NBI-VB ports can be independently configured to:

- ‘admit all frames’
- ‘admit only tagged frames’
- ‘admit only untagged frames’

Note: The priority tagged frame (VID=0) will be treated as an untagged frame.

The RTL8305NBI-VB also can optionally discard a frame associated with a VLAN of which the ingress port is not in the member set.

For the egress filter, the RTL8305NBI-VB drops the frame if this frame belongs to a VLAN but its egress port is not one of the VLAN’s member ports. However, there are 5 leaky options to provide exceptions for special applications.

- ‘Unicast leaky VLAN’ enables inter-VLAN unicast packet forwarding. That is, if the layer 2 lookup table search has a hit, then the unicast packet will be forwarded to the egress port, ignoring the egress rule
- ‘Multicast leaky VLAN’ enables inter-VLAN multicast packet forwarding. Packets may be flooded to all the multicast address group member sets, ignoring the VLAN member set domain limitation
- ‘Broadcast leaky VLAN’ enables inter-VLAN broadcast packet forwarding. Packets may be flooded to all the other ports, ignoring the VLAN member set domain limitation
- ‘ARP leaky VLAN’ enables broadcasting of ARP packets to all other ports, ignoring the egress rule
- ‘Inter-VLAN mirror function’ enables the inter-VLAN mirror function, ignoring the VLAN member set domain limitation. The default value is ‘Enable the inter-VLAN mirror’

8.2. IEEE 802.1p Remarking Function

The RTL8305NBI-VB provides IEEE 802.1p Remarking ability. Each port can enable or disable IEEE 802.1p Remarking ability.

In addition, there is a RTL8305NBI-VB global IEEE 802.1p Remarking Table. When one port enables 802.1p Remarking ability, 2-bit priority (not QID) determined by the RTL8305NBI-VB is mapped to 3-bit priority according to the 1p Remarking Table.

If the port's 1p remarking function is enabled, transmitting VLAN tagged packets will have the 1Q VLAN tag's Priority field replaced with the 3-bit 1p remarking Priority.

When the VLAN tags are inserted to non-tagged packets, the inserted tag's priority will accord with the 1p remarking table, even if the port's 1p remarking function is disabled. When the VLAN tag is replaced on tagged packets and the 1p remarking function is disabled, the VLAN tag's VID will be replaced but the priority will not change. For a VLAN-tagged packet, the VID and 3-bit priority can be replaced by the RTL8305NBI-VB independently.

8.3. QoS Function

8.3.1. Bandwidth Control

8.3.1.1 Output (TX) Bandwidth Control

The RTL8305NBI-VB supports MIN-MAX packet scheduling.

Packet scheduling offers three modes:

- Type I leaky bucket, which specifies the average rate of one queue (see Figure 14; only Q2 and Q3 have leaky bucket, Q0 and Q1 do not). The queue rate can be configured from 0kbps to the line rate in steps of 64kbps
- Weighted Round Robin (WRR), which decides which queue is selected in one slot time to guarantee the minimal packet rate of one queue
- Port bandwidth control (type II leaky bucket) to control the bandwidth of the whole port. The port rate can be configured from 0kbps to the line rate in steps of 64kbps

In addition, the RTL8305NBI-VB can select one of the two sets of packet-scheduling configurations according to the packet-scheduling mode. Figure 14 shows the RTL8305NBI-VB packet-scheduling diagram.

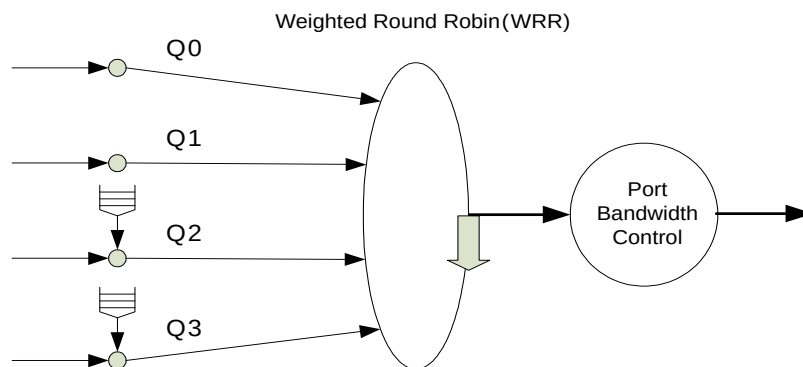


Figure 14. Packet-Scheduling Diagram

Weighted Round Robin (WRR)

WRR adds weighting based on Round Robin; for example, assume Q3:Q2:Q1:Q0: 4:3:2:1, then the transmit order will be:

```
Q0->
Q1->Q1->
Q2->Q2->Q2->
Q3->Q3->Q3->Q3->
```

WRR guarantees a minimal packet rate for one queue only.

If there is strict priority (only in Q2 and Q3) and WRR at the same time, the queue with strict priority has higher priority than WRR. When the scheduler scans queues, queues with strict priority are scanned first, and then the other queues are scanned according to WRR. If there is more than one queue with strict priority, the queue with the bigger QID has higher priority.

8.3.1.2 Input (RX) Bandwidth Control

Input bandwidth control limits the input bandwidth. When input traffic is more than the RX Bandwidth parameter, this port will either send out a ‘pause ON’ frame, or drop the input packet depending on the flow control status. The input bandwidth can also be configured from 0kbps to the line rate in steps of 64kbps.

8.3.2. Priority Assignment

Priority assignment specifies the priority of a received packet according to various rules. The RTL8305NBI-VB can recognize the QoS priority information of incoming packets to give a different egress service priority.

The RTL8305NBI-VB identifies the priority of packets based on several types of QoS priority information:

- Port-based priority
- IEEE 802.1p/Q VLAN Priority Tag
- DSCP Priority field
- IP Address
- Reassigned priority
- RLDP priority

Below is a block diagram of the priority assignment.

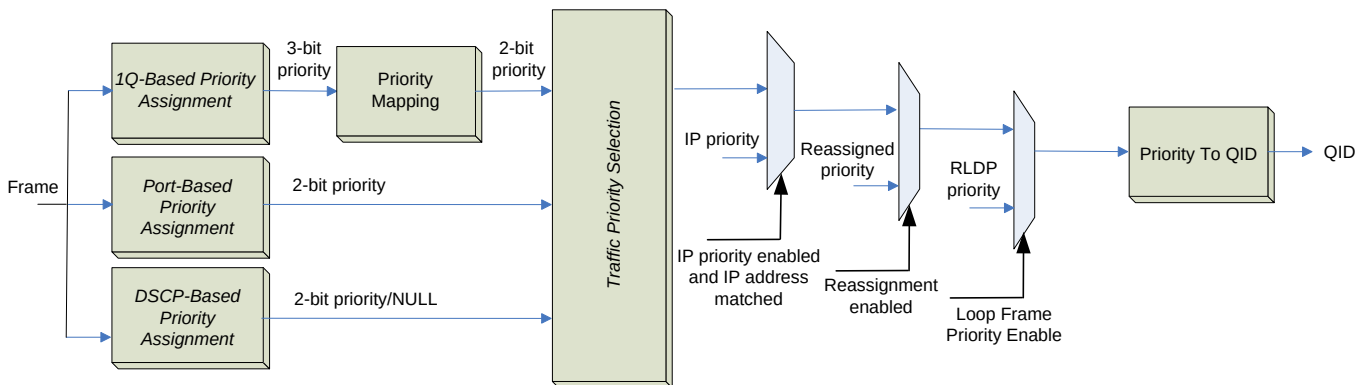


Figure 15. RTL8305NBI-VB Priority Assignment Diagram

8.3.2.1 Queue Number Selection

In the RTL8305NBI-VB, the output queue number can be set. All ports follow a global configuration. The maximum number of output queues per port is 4. After changing the queue number via SMI (Serial Management Interface), the external device must perform a soft reset in order to update the configuration.

8.3.2.2 Port-Based Priority Assignment

Each physical port is assigned a 2-bit priority level. Packets received from a high-priority port are sent to the high-priority queue of the destination port. Port-based priority can be disabled by register setting.

8.3.2.3 IEEE 802.1p/Q-Based Priority Assignment

In IEEE 802.1Q-based priority assignment, when a packet is VLAN-tagged or priority-tagged, the 3-bit priority is specified by tag. When a packet is untagged, the 802.1Q-based priority is assigned to the default 2-bit priority information of a physical port. So, each port must provide a default 2-bit priority (every received packet must be assigned a 2-bit 1Q-based priority). When the priority comes from a packet, the 1Q-based priority is acquired by mapping 3-bit tag priority to 2-bit priority through an RTL8305NBI-VB 1Q-based Priority Mapping Table. The 1Q-based priority can be disabled.

8.3.2.4 DSCP-Based Priority Assignment

DSCP (Differentiated Services Code Point)-based priority assignment maps the DSCP of an IP packet to 2-bit priority information through a DSCP to priority table, as DSCP is only in the IP packet. A non-IP packet (such as a Layer 2 frame, ARP, etc) will get a NULL instead of a 2-bit priority. For an IPv6 IP header, DSCP-based priority assignment acquires the DSCP value according to the class of IPv6 header.

In the RTL8305NBI-VB, DSCP-based priority assignment provides a DSCP to Priority Table of all DSCP values. If the DSCP of a packet is not matched in the table, the DSCP-based priority is 2'b00. The DSCP-based priority can be disabled by register.

8.3.2.5 IP Address-Based Priority

When IP-based priority is enabled, any incoming packets with source or destination IP address equal to the configuration in register IP Priority Address [A] and IP Priority Mask [A], or IP Priority Address [B] and IP Priority Mask [B] will be set to a 2-bit priority.

IP priority [A] and IP priority [B] may be enabled or disabled independently. IP address-based priority can be enabled or disabled by the control register.

8.3.2.6 Reassigned Priority

The RTL8305NBI-VB can reassign the priority mainly according to the packets' DMAC information. This function is used to differentiate the priority of the Layer 2 control packet, broadcast packet, multicast packet, unicast packet, and so on.

8.3.2.7 RLDP-Based Priority

To support the loop detection effectively, the RTL8305NBI-VB provides the RLDP-based priority assignment. When it is enabled, the pre-defined priority will be assigned to all RLDP packets.

8.3.2.8 Packet Priority Selection

As one received packet may simultaneously support several priority assignment mechanisms, e.g., Port-Based Priority, 1Q-Based Priority, DSCP-Based Priority, it may get several different priority values.

- RLDP-based priority has the highest priority
- If RLDP-based priority is disabled, the final priority is equal to the reassigned priority
- If RLDP-based priority and reassigned priority is disabled, the final priority is equal to the IP address priority
- If RLDP-based priority, reassigned priority and IP address priority are disabled, the following rules are used to decide a final priority for the other five types of priority

There is a 2-bit register for each of the three types of priority that represent the weight of the priority. The higher value in the register indicates a higher weight for the priority. If more than one of the three types of priority is the same, the final priority will be given to the type whose priority value is greatest.

Queue Priority Mapping

The 2-bit priority has four numbers; however, every port has at most four output queues, so every port needs a User Priority to Traffic Class Mapping Table to map the priority to QID. A set of Traffic Class Mapping Tables is provided for each port independently. There is a mechanism to prevent a problem caused by mapping the traffic to an unused queue. For example, when a port's queue number is 2, queue 2 and queue 3 are not used and mapping the traffic to queue 2 or queue 3 will cause the system to crash. In the mechanism, traffic mapped to the unused queue will be forced to the highest used queue (queue 2 in a 3-queue case, queue 1 in a 2-queue case, queue 0 in a 1-queue case). In the example, the traffic mapped to a port's queue 2 or queue 3 will be forwarded to queue 1.

8.4. Lookup Table Function

8.4.1. Function Description

- 2048-entry lookup table (LUT)
- 4-way entry for each entry index
- Supports LRU (Least Recently Used) function for lookup table learning

8.4.2. Address Search, Learning, and Aging

Received packets are forwarded according to the information learned or written into the LUT. When a packet is received, the RTL8305NBI-VB tries to retrieve learned information and assign a forwarding destination port to the packet.

The 48-bit destination MAC address (DA) of the received packet and the 2-bit FID are used to calculate a 9-bit index value. The hash algorithm uses all 48 bits of the MAC address and 2 bits of the FID. The hash algorithm is shown below.

$$\text{Index0} = \text{MAC4} \wedge \text{MAC11} \wedge \text{MAC18} \wedge \text{MAC25} \wedge \text{MAC32}$$

$$\text{Index1} = \text{MAC3} \wedge \text{MAC10} \wedge \text{MAC17} \wedge \text{MAC24} \wedge \text{MAC47}$$

$$\text{Index2} = \text{MAC2} \wedge \text{MAC9} \wedge \text{MAC16} \wedge \text{MAC39} \wedge \text{MAC46}$$

$$\text{Index3} = \text{MAC1} \wedge \text{MAC8} \wedge \text{MAC31} \wedge \text{MAC38} \wedge \text{MAC45}$$

$$\text{Index4} = \text{FID1} \wedge \text{MAC0} \wedge \text{MAC23} \wedge \text{MAC30} \wedge \text{MAC37} \wedge \text{MAC44}$$

$$\text{Index5} = \text{FID0} \wedge \text{MAC15} \wedge \text{MAC22} \wedge \text{MAC29} \wedge \text{MAC36} \wedge \text{MAC43}$$

$$\text{Index6} = \text{MAC7} \wedge \text{MAC14} \wedge \text{MAC21} \wedge \text{MAC28} \wedge \text{MAC35} \wedge \text{MAC42}$$

$$\text{Index7} = \text{MAC6} \wedge \text{MAC13} \wedge \text{MAC20} \wedge \text{MAC27} \wedge \text{MAC34} \wedge \text{MAC41}$$

$$\text{Index8} = \text{MAC5} \wedge \text{MAC12} \wedge \text{MAC19} \wedge \text{MAC26} \wedge \text{MAC33} \wedge \text{MAC40}$$

As the 9-bit MAC addresses, MAC[13:15] and MAC[0:5] are not stored in the LUT entries, these MAC address bits should be calculated from the index information via the following method when the hash algorithm is selected.

$$\text{MAC0} = \text{Index4} \wedge \text{FID1} \wedge \text{MAC23} \wedge \text{MAC30} \wedge \text{MAC37} \wedge \text{MAC44}$$

$$\text{MAC1} = \text{Index3} \wedge \text{MAC8} \wedge \text{MAC31} \wedge \text{MAC38} \wedge \text{MAC45}$$

$$\text{MAC2} = \text{Index2} \wedge \text{MAC9} \wedge \text{MAC16} \wedge \text{MAC39} \wedge \text{MAC46}$$

$$\text{MAC3} = \text{Index1} \wedge \text{MAC10} \wedge \text{MAC17} \wedge \text{MAC24} \wedge \text{MAC47}$$

$$\text{MAC4} = \text{Index0} \wedge \text{MAC11} \wedge \text{MAC18} \wedge \text{MAC25} \wedge \text{MAC32}$$

$$\text{MAC5} = \text{Index8} \wedge \text{MAC12} \wedge \text{MAC19} \wedge \text{MAC26} \wedge \text{MAC33} \wedge \text{MAC40}$$

$$\text{MAC13} = \text{Index7} \wedge \text{MAC6} \wedge \text{MAC20} \wedge \text{MAC27} \wedge \text{MAC34} \wedge \text{MAC41}$$

$$\text{MAC14} = \text{Index6} \wedge \text{MAC7} \wedge \text{MAC21} \wedge \text{MAC28} \wedge \text{MAC35} \wedge \text{MAC42}$$

$$\text{MAC15} = \text{Index5} \wedge \text{FID0} \wedge \text{MAC22} \wedge \text{MAC29} \wedge \text{MAC36} \wedge \text{MAC43}$$

The hashed index key is used to locate a matching LUT entry. There are 4 entries sharing one index key (Table 15). This is called a 4-way hash. It is helpful to minimize address collisions in the address learning process. The address search engine compares the DA packet with the data in 4 entries, from entry 3 to entry 0. The final forwarding destination is abstracted from the first matching entry. If the address search fails to return a matching LUT entry, the packet will be flooded to appropriate ports.

Table 15. L2 Table 4-Way Hash Index Method

Index	Entry 0	Entry 1	Entry 2	Entry 3
0x00	MAC Addr 0	MAC Addr 1	MAC Addr 2	MAC Addr 3
0x01	MAC Addr 4	MAC Addr 5	MAC Addr 6	MAC Addr 7
0x02	MAC Addr 8	MAC Addr 9	MAC Addr 10	MAC Addr 11
...	...	...	...	...
0x1FE	MAC Addr 2040	MAC Addr 2041	MAC Addr 2042	MAC Addr 2043
0x1FF	MAC Addr 2044	MAC Addr 2045	MAC Addr 2046	MAC Addr 2047

Address learning is the gathering process and storing of information from received packets for the future purpose of forwarding frames addressed to the receiving port. The information includes the source MAC address (SA) and the receiving port. As with the hash algorithm, an address search is used in address learning. The SA of the received packet is used to calculate the entry index. The receiving port information and the aging timer of the first matching entry will be updated when an address is learned. If there is no matching entry, the packet's information will be 'learned' into the first empty entry. The SA will not be learned when all of the 4 entries are occupied. The address learning process can be disabled on a per-port basis via register setting.

For unicast packet learning & search, and multicast packet search, the RTL8305NBI-VB applies the same 4-way hash algorithm.

Address aging is used to keep the contents of the learned address table updated in a dynamic network topology. The look-up engine will update the aging timer of an entry whenever the corresponding SA appears. An entry will be invalid (aged out) if its aging timer is not refreshed by the address learning process during the aging time period. The aging time of the RTL8305NBI-VB is between 200 and 400 seconds. The RTL8305NBI-VB also supports a fast aging function that is used to age all dynamic entries within 1ms.

8.4.3. Lookup Table Definition

In traditional switch learning, if a MAC address hash collision occurs then the later MAC address in the collision will not be learned into the lookup table. The LRU function attempts to resolve this problem.

When Enable LRU = 0b1, then the LRU function is enabled. If the Source MAC address of the incoming packet encounters a hash collision during the learning process, and when the 4-way entries are all occupied, then the switch will learn the address into one of the 4-way entries using the LRU aging timer. The criteria for selecting the entry to over-write is compared via the aging timer and by choosing the oldest entry. If the aging timer of the 4 entries are the same, then the entry with the highest Entry_Address[1:0] value is selected to be over-written.

8.5. Storm Filter Function

The RTL8305NBI-VB can effectively control four-types of broadcast storms; those caused by broadcast packets, multicast packets, unknown multicast packets, and unknown DA unicast packets.

Note: Broadcast packets discussed here are packets whose DA is ff-ff-ff-ff-ff-ff.

Multicast packets include all multicast packets and only unknown multicast packets, which are those whose DA is a multicast address, but excluding 01-80-C2-00-00-xx.

An unknown DA unicast packet is a packet whose DA is a unicast address and is not found in the lookup table of the switch.

The RTL8305NBI-VB can configure a storm filter rate for these four packet types, and the rate unit can be configured as packet-based or byte-based via registers. The storm filter rate limits the packet forwarding rate to less than the rate threshold.

8.6. Input and Output Drop Function

If some destination ports are blocking, or the buffer is full, the frames to these ports will be dropped.

There are two types of drop:

- Input Drop: Drop the frame directly. Do not forward to any port
- Output Drop: Forward only to non-blocking ports

For the RTL8305NBI-VB, the dropping of broadcast, multicast, and unknown DA frames can be controlled independently.

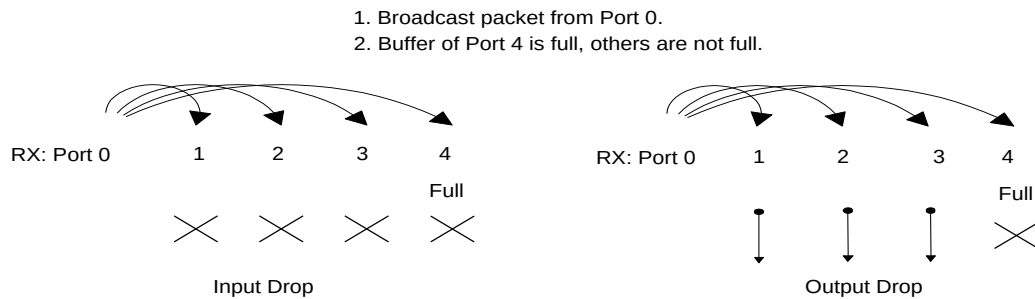


Figure 16. Broadcast Input Drop vs. Output Drop

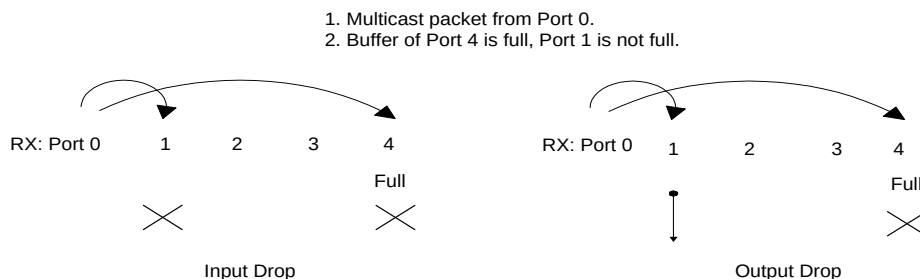


Figure 17. Multicast Input Drop vs. Output Drop

8.7. LED Function

The RTL8305NBI-VB provides flexible LED functions for diagnostics. The LEDs can be configured to indicate the link information (link, activity, speed, duplex), and collision & loop detection information.

The parallel LED for each port indicates the port's link information when loop-detection is disabled or no loop condition occurs. If the loop is detected on a port, the parallel LED will blink.

All LED statuses are represented as active-low or high depending on input strapping.

LED_BLINK_TIME determines the LED blinking period for activity and collision via register (0: 32ms and 1: 128ms).

Some LED pins are dual function pins: input operation for configuration upon reset, and output operation for LED after reset. If the pin input is floating upon reset, the pin output is active high after reset. Otherwise, if the pin input is pulled high upon reset, the pin output is active low after reset.

Figure 18 shows example circuits for LEDs. Typical values for pull-down resistors are 10KΩ.

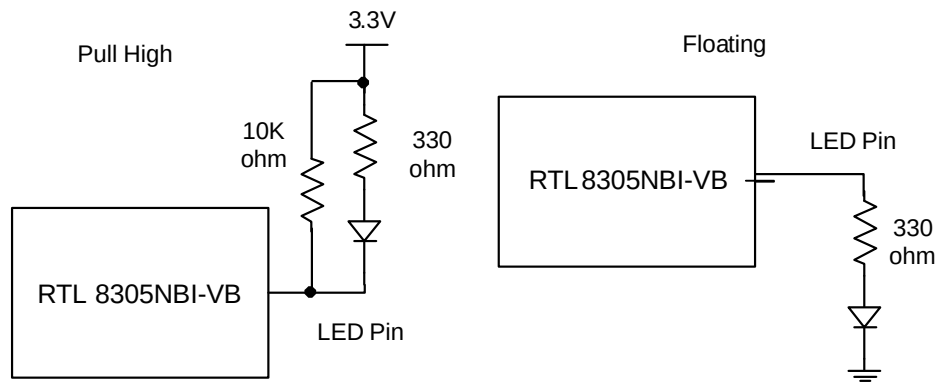


Figure 18. Floating and Pull-High of LED Pins for LED

8.8. *Energy-Efficient Ethernet (EEE)*

The RTL8305NBI-VB supports Energy-Efficient Ethernet (EEE) function as defined in IEEE 802.3az. The EEE function implements the Low Power Idle (LPI) mode at 100Mbps operation to save power during periods of low link utilization. In Low Power Idle mode, devices on both sides of the link disable portions of the functionality to lower the power consumption.

At the transmitter side, ports 0~4 of the RTL8305NBI-VB can automatically enter or quit LPI mode based on their transmission loading. When a port's EEE function is enabled, the transmission loading is monitored in real time. If the transmission loading is lower than a preset threshold, this port's transmission circuit will enter LPI mode during the idle period. When there are packets to be transmitted, this port wakes up and quits LPI mode.

There are two types of wake-up:

- Packets in a high priority queue or a control packet (e.g., a PAUSE frame). These can wake up the port immediately
- Packet in a low priority queue that reach a preset number. A port in LPI mode can be woken up by low priority packets when the number of the cumulated low priority packets exceeds the preset threshold or a delay timer expires

At the receiver side, each embedded PHY of the RTL8305NBI-VB will automatically respond to the request from the link partner to enter or quit the LPI mode.

The EEE ability for 100Base-TX on each side of a link should be exchanged via auto-negotiation. Auto-negotiation is mandatory when EEE is enabled. The MDIO Manageable Device (MMD), defined in IEEE 802.3, Clause 45, should also be supported, as the EEE register is located in the MMD of each PHY.

The RTL8305NBI-VB also supports EEE at 10Mbps operation by reducing the transmit amplitude (10Base-Te). 10Base-Te is fully interoperable with 10Base-T PHYs over 100m of Category 5 or better cable.

The EEE function for each port is enabled by default and can be disabled independently via strapping pin, registers, or EEPROM configurations.

8.9. *Cable Diagnosis*

The RTL8305NBI-VB physical layer transceivers use DSP technology to implement the Realtek Cable Tester (RTCT) feature for cable diagnosis. The RTCT feature can detect short, open, or normal in both differential pair signal runs.

9. Characteristics

9.1. Electrical Characteristics/Maximum Ratings

WARNING: Maximum ratings are limits beyond which permanent damage may be caused to the device or which may affect device reliability. All voltages are specified reference to GND unless otherwise specified.

Table 16. Electrical Characteristics/Maximum Ratings

Parameter	Min	Max	Units
DVDDH, AVDDH, AVDDHPLL Supply Referenced to GND	GND-0.3	+3.63	V
DVDDL, AVDDL, AVDDLPLL Supply Referenced to GND	GND-0.3	+1.32	V

9.2. Operating Range

Table 17. Operating Range

Parameter	Min	Max	Units
Storage Temperature	-55	+150	°C
Ambient Operating Temperature (Ta)	-40	+85	°C
3.3V Vcc Supply Voltage Range (DVDDH, AVDDH, AVDDHPLL)	3.13	3.47	V
1.2V Vcc Supply Voltage Range (DVDDL, AVDDL, AVDDLPLL)	1.14	1.26	V

9.3. DC Characteristics

Table 18. DC Characteristics

Parameter	SYM	Condition	Min	Typ.	Max	Units
TTL Input High Voltage	V _{ih}	-	2.0	-	-	V
TTL Input Low Voltage	V _{il}	-	-	-	0.8	V
TTL Input Current	I _{in}	-	-10	-	10	μA
TTL Input Capacitance	C _{in}	-	-	3	-	pF
Output High Voltage	V _{oh}	-	2.25	-	-	V
Output Low Voltage	V _{ol}	-	-	-	0.4	V
Output Three State Leakage Current	I _{oz}	-	-	-	10	μA
Power Supply Current for 1.2V	I _{cc}	10Base-T, idle	-	32	-	mA
		10Base-T, Peak continuous 100% utilization	-	35	-	
		100Base-TX, idle	-	87	-	
		100Base-TX, Peak continuous 100% utilization	-	88	-	
		Link down	-	33	-	
Power Supply Current for 3.3V	I _{cc}	10Base-T, idle	-	17	-	mA
		10Base-T, Peak continuous 100% utilization	-	111	-	
		100Base-TX, idle	-	93	-	
		100Base-TX, Peak continuous 100% utilization	-	93	-	
		Link down	-	17	-	

Parameter	SYM	Condition	Min	Typ.	Max	Units
Total Power Consumption for All Ports	PS	10Base-T, idle	-	94.5	-	mW
		10Base-T, Peak continuous 100% utilization	-	408.3	-	
		100Base-TX, idle	-	411.3	-	
		100Base-TX, Peak continuous 100% utilization	-	412.5	-	
		Link down	-	95.7	-	

Note: All power supply currents are measured under the following conditions:

1. DVDDL=AVDDL=AVDDHPLL=1.2V; DVDDH=AVDDH=AVDDHPLL=3.3V.
2. Room temperature.
3. The EEE and Green features are disabled.
4. All LEDs are in low-active mode.
5. LDO power is not included.

9.4. Thermal Characteristics

9.4.1. Simulation Conditions

Table 19. PCB Descriptions

PCB	PCB Dimension (L x W)	79.7 x 50.8mm
	PCB Thickness	1.6mm
	PCB Top GND Plane Size	75%
	Number of Cu Layer-PCB	1-Layer

Table 20. Condition Descriptions

Input Power	0.6 W
Test Board (PCB)	1 Layer
Control Condition	Air Flow= 0, 1, 2, 3ms

9.4.2. Thermal Characteristics Results

Table 21. Thermal Characteristics Results

Air Flow (ms)	0	1	2	3
θ_{JA} (°C/W)	51.6	45.6	43.4	41.7
ψ_{JT} (°C/W)	0.8	-	-	-
ψ_{JB} (°C/W)	24.6	-	-	-
Max. Junction Temperature	125°C			

9.5. Digital Timing Characteristics

9.5.1. LED Timing

Table 22. LED Timing

Parameter	SYM	Conditions	Min	Typ.	Max	Units
LED On Time	tLEDOn	LED Blinking to Indicate Link Information	32	-	128	ms
LED Off Time	tLEDOff	LED Blinking to Indicate Link Information	32	-	128	ms

9.5.2. Reception/Transmission Data Timing of SMI Interface

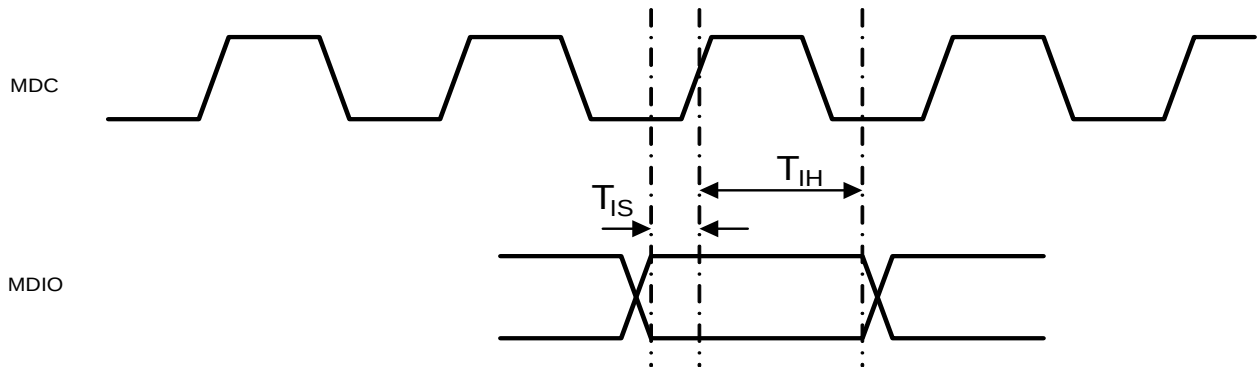


Figure 19. Reception Data Timing of SMI Interface

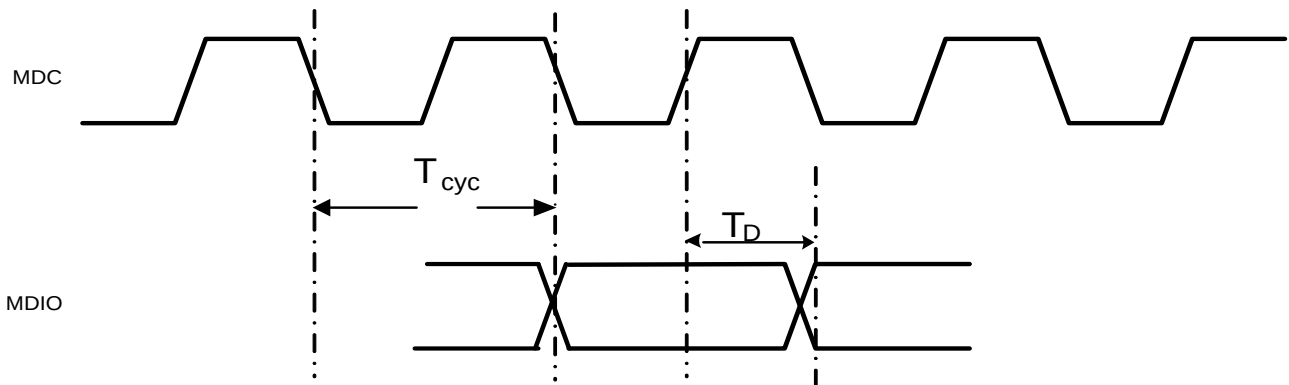


Figure 20. Transmission Data Timing of SMI Interface

Table 23. SMI Timing

Parameter	SYM	Description	I/O	Min	Typ.	Max	Units
MDC	T_{cyc}	MDC Clock Cycle.	I	400	-	-	ns
MDIO Input Setup Time	T_{IS}	MDIO to MDC Rising Edge Setup Time.	I	50	-	-	ns
MDIO Input Hold Time	T_{IH}	MDIO to MDC Rising Edge Hold Time.	I	10	-	-	ns
MDIO Output Delay Time	T_D	MDIO to MDC Rising Edge Output Delay.	O	2	-	10	ns

9.5.3. EEPROM Auto-Load Timing

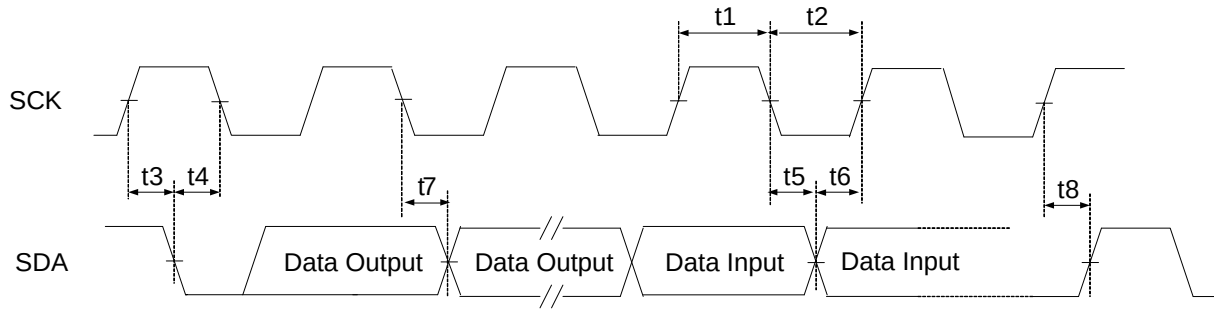
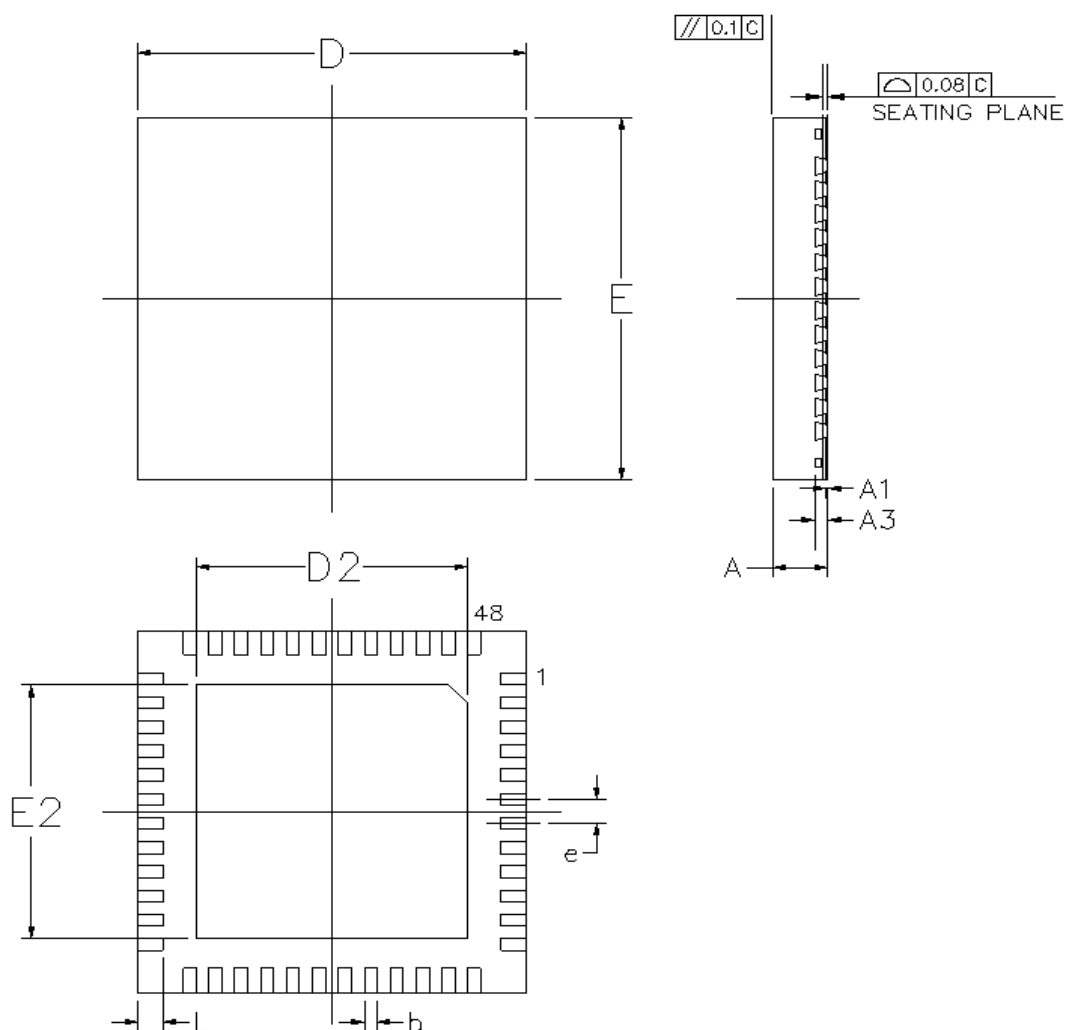


Figure 21. EEPROM Auto-Load Timing

Table 24. EEPROM Auto-Load Timing Characteristics

Symbol	Description	Min	Typ.	Max	Units
t_1	SCL High Time.	-	2.52	-	μs
t_2	SCL Low Time.	-	2.52	-	μs
t_3	START Condition Setup Time.	-	2.52	-	μs
t_4	START Condition Hold Time.	-	2.52	-	μs
t_5	Data In Hold Time.	0	-	-	ns
t_6	Data In Setup Time.	100	-	-	ns
t_7	Data Output Hold Time.	-	1.28	-	μs
t_8	STOP Condition Setup Time.	-	2.52	-	μs

10. Mechanical Dimensions



10.1. Mechanical Dimensions Notes

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.75	0.85	1.00	0.030	0.034	0.039
A ₁	0.00	0.02	0.05	0.000	0.001	0.002
A ₃	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	6.00BSC			0.236BSC		
D2/E2	4.15	4.4	4.65	0.163	0.173	0.183
e	0.40BSC			0.016BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Note 1: CONTROLLING DIMENSION: MILLIMETER (mm).

Note 2: REFERENCE DOCUMENT: JEDEC MO-220.

11. Ordering Information

Table 25. Ordering Information

Part Number	Package	Status
RTL8305NBI-VB-CG	48-Pin QFN in 'Green' Package (RoHS Compliant) (Industrial version).	MP

Note: See page 5 for package identification.

Realtek Semiconductor Corp.

Headquarters

No. 2, Innovation Road II
Hsinchu Science Park, Hsinchu 300, Taiwan
Tel.: +886-3-578-0211. Fax: +886-3-577-6047
www.realtek.com