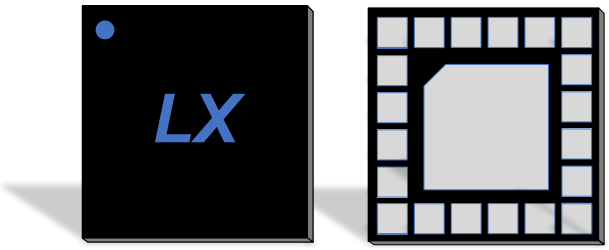


Product Features

- Excellent insertion loss
  - 0.50 dB Insertion Loss at 2.7GHz
- P0.1dB @ 29dBm
- Multi-Band operation 700MHz to 3800MHz
- RFFE serial control interface
- Compact 2mm x 2mm in QFN-14 package，MSL1
- No DC blocking capacitors required (unless external DC is applied to the RF ports)

Product Applications

- 2G/3G/4G antenna diversity
- Cellular modems and USB Devices

Product Description

The LX8686 is a low loss, high isolation SP8T switch for antenna diversity receiving.

The LX8686 is compatible with MIPI control, which is a key requirement for many cellular transceivers. This part is packaged in a compact 2mm x 2mm, 14-pin, QFN package which allows for a small solution size with no need for external DC blocking capacitors (when no external DC is applied to the device ports).

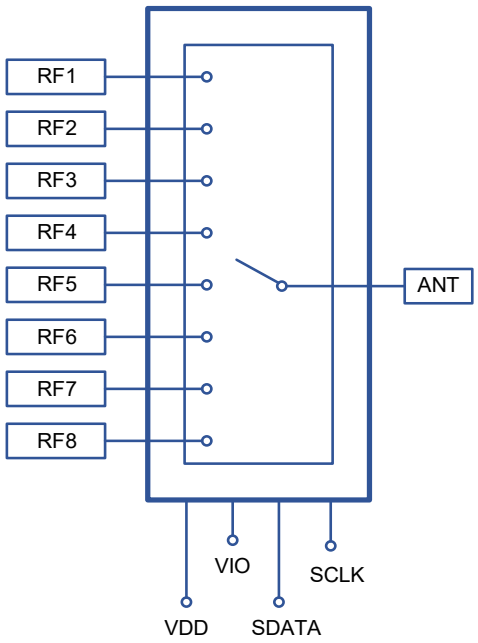


Figure 1 Functional Block Diagram

Pin Configuration (Top View)

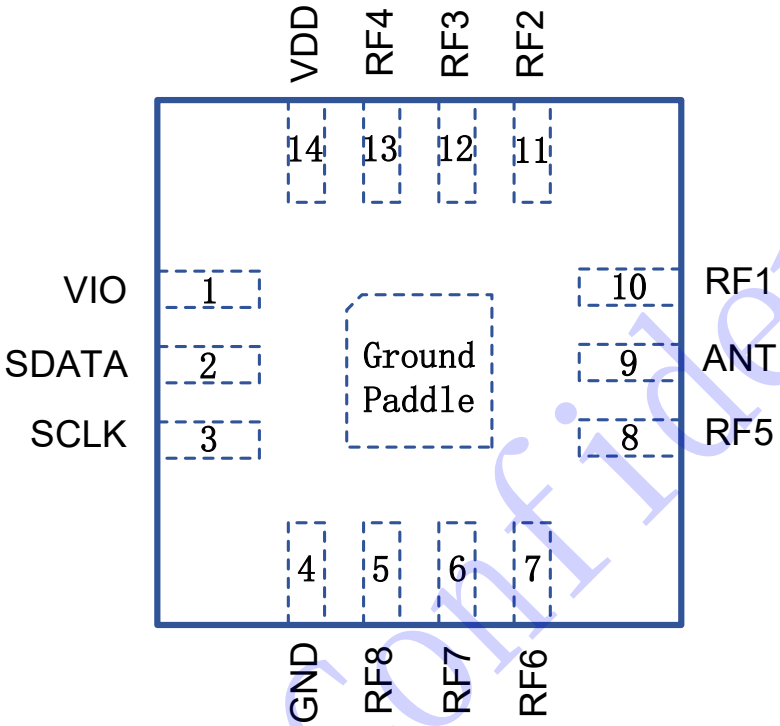


Figure 2 Pin Configuration (Top View)

Pin Descriptions

Table 1:

NO.	Name	Description	NO.	Name	Units
1	VIO	RFFE Reference Voltage	8	RF5	RF Port5
2	SDATA	RFFE Data Bus	9	ANT	Antenna Port
3	SCLK	RFFE Clock Bus	10	RF1	RF Port1
4	GND	Ground	11	RF2	RF Port2
5	RF8	RF Port8	12	RF3	RF Port3
6	RF7	RF Port7	13	RF4	RF Port4
7	RF6	RF Port6	14	VDD	Power Supply Voltage
Ground Paddle	GND	Ground			

Function Characteristics

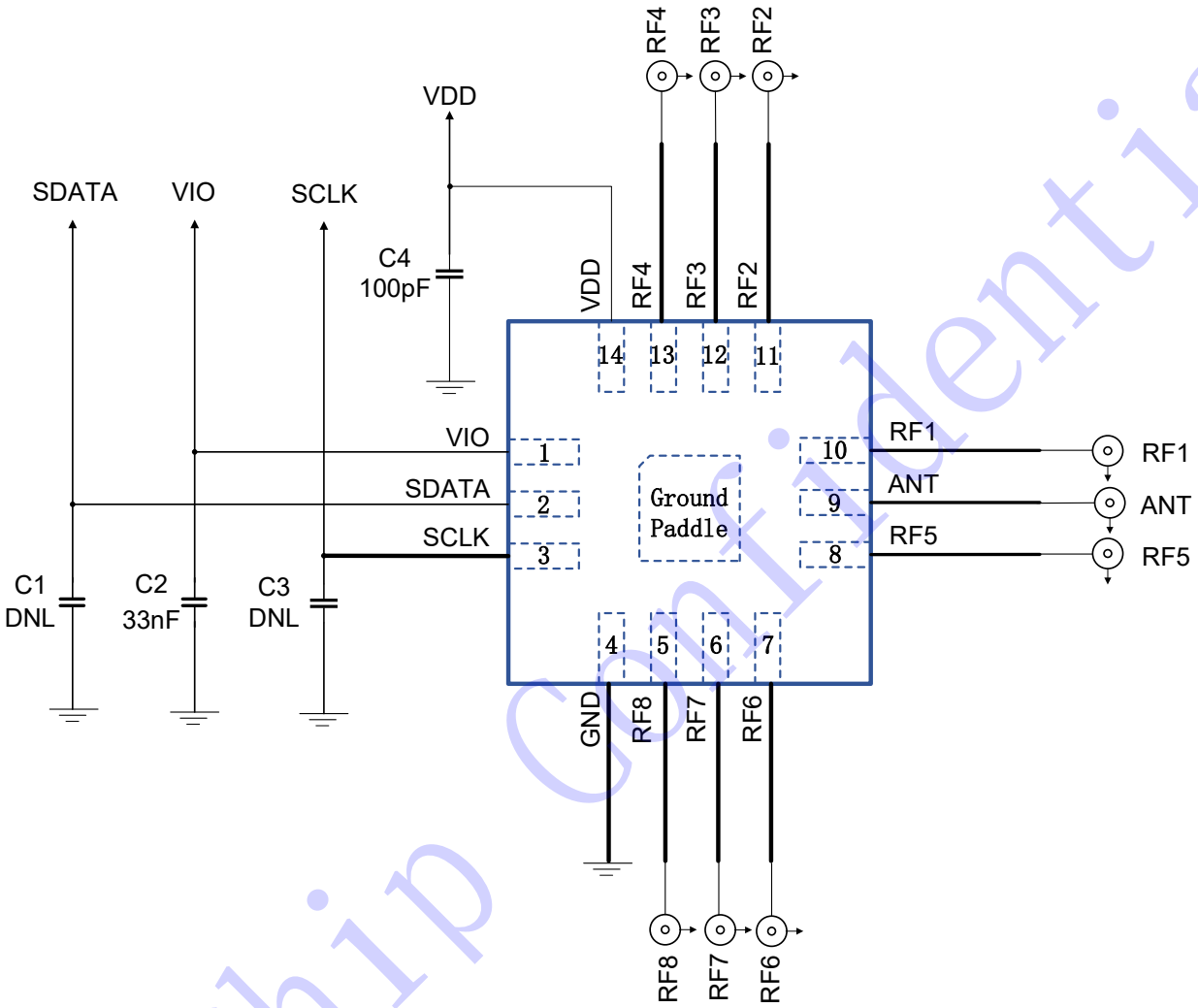


Figure 3 Evaluation Board Schematic

Truth Table

Table 2:

Control	Switched RF Outputs							
Register_0	RF1	RF2	RF3	RF4	RF5	RF6	RF7	RF8
0x0A	Insertion Loss	Isolation	Isolation	Isolation	Isolation	Isolation	Isolation	Isolation
0x08	Isolation	Insertion Loss	Isolation	Isolation	Isolation	Isolation	Isolation	Isolation
0x0B	Isolation	Isolation	Insertion Loss	Isolation	Isolation	Isolation	Isolation	Isolation
0x09	Isolation	Isolation	Isolation	Insertion Loss	Isolation	Isolation	Isolation	Isolation
0x01	Isolation	Isolation	Isolation	Isolation	Insertion Loss	Isolation	Isolation	Isolation
0x04	Isolation	Isolation	Isolation	Isolation	Isolation	Insertion Loss	Isolation	Isolation
0x0C	Isolation	Isolation	Isolation	Isolation	Isolation	Isolation	Insertion Loss	Isolation
0x05	Isolation	Isolation	Isolation	Isolation	Isolation	Isolation	Isolation	Insertion Loss

Recommended Operating Conditions

Table 3:

Parameters	Symbol	Min	Typ	Max	Units
Operating Frequency	F_1	0.7		3.8	GHz
Supply Voltage	V_{DD}	2.5	2.8	4.2	V
Power supply for MIPI	V_{IO}	1.65	1.8	1.95	V
MIPI Control Voltage High	V_H	0.8*VIO	1.8	1.95	V
MIPI Control Voltage Low	V_L	0	0	0.2*VIO	V

Absolute Maximum Conditions

Table 4:

Parameters	Symbol	Min	Max	Units
Power Supply	V_{DD}	+2.5	+4.2	V
Supply voltage for MIPI	V_{IO}	+1.0	+2.0	V
MIPI Control voltage (SDATA, SCLK)	V_{CTL}	0	+2.0	V
RF input power (RF1 to RF8)	P_{IN}		+29	dBm
Device Operating Temperature	T_{OP}	-35	+90	℃
Device Storage Temperature	T_{STG}	-40	+125	
Electrostatic Discharge Human body model (HBM), Class 1C Machine Model (MM), Class A Charged device model (CDM), Class III	 ESD_HBM ESD_MM ESD_CDM		 1000 100 500	V

Notices: *Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.*

Power ON and OFF sequence

Here is the recommendation about power-on/off sequence in order to avoid damaging the device.

Power ON

1) Apply voltage supply - VDD
2) Apply logic supply - VIO
3) Wait 10μs or greater and then apply MIPI bus signals – SCLK and SDATA
4) Wait 5μs or greater after MIPI bus goes idle and then apply the RF Signal

Power OFF

1) Remove the RF Signal
2) Remove MIPI bus – SCLK and SDATA
3) Remove logic supply - VIO
4) Remove voltage supply – VDD

DC Performances

Table 5:

Parameters	Symbol	Test Condition	Min.	Typ.	Max.	Units
Supply Voltage	V_{DD}		2.5	2.8	3.6	V
Supply Current	I_{DD}			50	80	uA
VIO supply voltage	V_{IO}		1.65	1.8	1.95	V
VIO Supply current	I_{IO}			4	10	uA
SDATA, SCLK control voltage: High Low	V_{CTL_H} V_{CTL_L}		0.8*V_{IO} 0	V_{IO} 0	1.95 0.3	V V
Switching Speed, one RF to another		10% to 90% RF		1	2	uS

RF Performances

Table 6:

Parameters	Symbol	Test Condition	Min.	Typ.	Max.	Units
Insertion loss (ANT pin to RF1/2/3/4/5/6/7/8 pins)	IL	0.1 to 1.0GHz 1.0 to 2.0GHz 2.0 to 2.7GHz 3.0 to 3.8GHz		0.4 0.6 0.8 1.0	0.5 0.7 0.8 1.1	dB
Isolation (ANT pin to RF1/2/3/4/5/6/7/8 pins)	ISO	0.1 to 1.0GHz 1.0 to 2.0GHz 2.0 to 2.7GHz 3.0 to 3.8GHz	35 25 20 17	40 30 24 20		
Input 0.1dB Compression point (ANT pin to RF1/2/3/4/5/6/7/8 pins)	$P_{0.1dB}$	F_0=950MHz,20%DC		+29		dBm

Register Definition

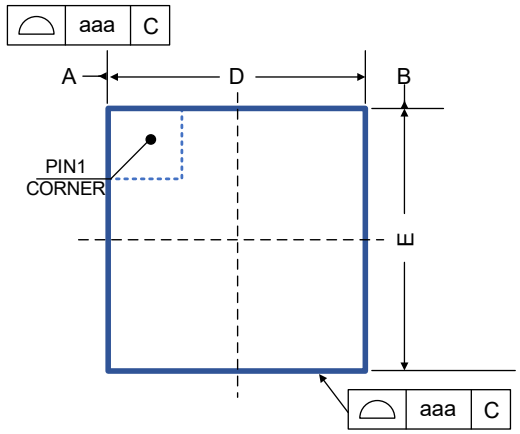
Table 7:

Register Address	Register Name	Data Bits	R/W	Function	Description	Default	BROADCAST_ID support	Trigger support
0x00	REGISTER_0	7:0	R/W	RF Control	Register_0 turth Table: Table 2	0x00	no	Yes
0x001A	RFFE_STATUS	7	R/W	SOFTWARE RESET	0: Normal operation 1: Software reset Note: On software reset, this register and all configurable registers are reset except for	0	No	No

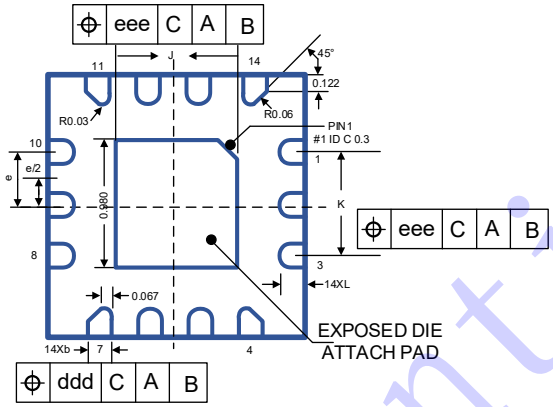
					USID, GSID, and PM_TRIG.			
		6	R/W	COMMAND_FRAME_PARITY_ERR	Command Frame with parity error	0	No	No
		5	R/W	COMMAND_LENGTH_ERR	Command Sequence with incorrect length	0	No	No
		4	R/W	ADDRESS_FRAME_PARITY_ERR	Address Frame with parity error	0	No	No
		3	R/W	DATA_FRAME_PARITY_ERR	Data Frame with parity error	0	No	No
		2	R/W	READ_UNUSED_REG	Read Command Sequence to an invalid address	0	No	No
		1	R/W	WRITE_UNUSED_REG	Write Command Sequence to an invalid address	0	No	No
		0	R/W	BID_GID_ERR	Read Command Sequence with a BSID or GSID Note: Reading this register resets this register.	0	No	No
0X001B	GROUP_SID	7:4	R	RESERVED		0x0	No	No
		3:0	R/W	GSID	Group Slave ID	0x0	No	No
0x001C		7:6	R/W	PWR_MODE	00: Normal Operation (ACTIVE) 01: Reset all registers to default settings (STARTUP) 10: Low power (LOW POWER) 11: Reserved Note: Write PWR_MODE=2'h1 will reset	0b10	Yes	No

					all register, and puts the device into STARTUP state.			
		5	R/W	Trigger_ Mask_2	If this bit is set, trigger 2 is disabled	0	No	No
		4	R/W	Trigger_ Mask_1	If this bit is set, trigger 1 is disabled	0	No	No
	MANUFACTURER_ID	3	R/W	Trigger_ Mask_0	If this bit is set, trigger 0 is disabled Note: When all triggers are disabled, writing to a register that is associated with trigger 0, 1, or 2, causes the data to go directly to the destination register.	0	No	No
		2	W	Trigger_2	A write of a one to this bit loads trigger 2's registers	0	Yes	No
		1	W	Trigger_1	A write of a one to this bit loads trigger 1's registers	0	Yes	No
		0	W	Trigger_0	A write of a one to this bit loads trigger 0's registers Note: Trigger processed immediately then cleared. Trigger 0, 1, and 2 will always read as 0.	0	Yes	No
0x001D	PRODUCT_ID	7:0	R	PRODUCT_ID	Product Number	0x5D	No	No
0x001E	MANUFACTURER_ID	7:0	R	MANUFACTURER_ID[7:0]	Lower eight bits of MIPI registered Manufacturer ID	0x78	No	No
0x001F	MAN_US ID	7:4	R	MANUFACTURER_ID [9:8]	Upper two bits of MIPI registered Manufacturer ID	0x04	No	No
		3:0	R/W	USID	USID of the device.	0xB	No	No

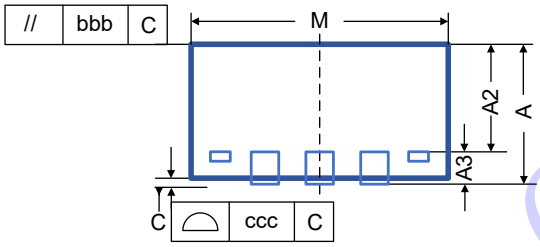
Package Outline Dimension



TOP VIEW



BOTTOM VIEW



SIDE VIEW

DESCRIPTION		SYMBOL	MILLIMETER		
			MIN.	NOM.	MAX.
TOTAL THICKNESS		A	0.50	0.55	0.60
STAND OFF		A1	0	-	0.05
MOLD THICKNESS		A2	0.35	0.40	0.45
L/F THICKNESS		A3	0.152 REF		
LEAD WIDTH		b	0.13	0.18	0.23
BODY SIZE	X	D	1.95	2.00	2.05
	Y	E	1.95	2.00	2.05
LEAD PITCH		e	0.40 BSC		
EP SIZE	X	J	0.93	0.98	1.03
	Y	K	0.93	0.98	1.03
LEAD LENGTH		L	0.16	0.21	0.26
PACKAGE EDGE TOLERANCE		aaa	0.100		
MOLD FLATNESS		bbb	0.100		
COPLANARITY		ccc	0.080		
LEAD OFFSET		ddd	0.100		
EXPOSED PAD OFFSET		eee	0.100		

Figure 4 Package Outline Dimension

Marking Specifications

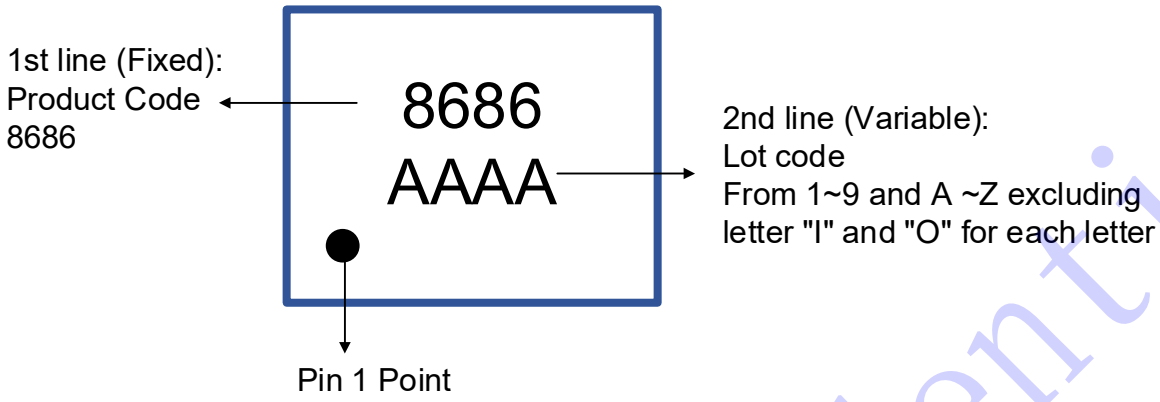


Figure 5 Marking Specification (Top View)

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electric charge. Proper ESD protection techniques should be applied when devices are operated.

RoHS Compliant

This product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) , and are considered RoHS compliant.

