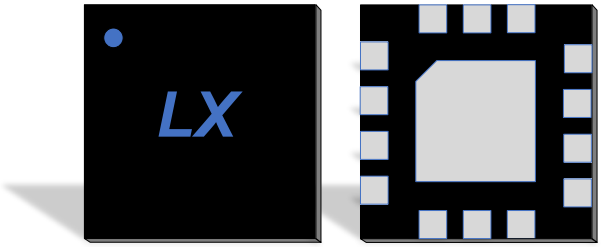


Product Features

- Multi-Band operation 0.1 to 2.7GHz
- Input P0.1dB compression Point: 36dBm
- MIPI RFFE V2.1 Compatible
- Small package: QFN-14 2.0mm x 2.0mm x 0.55mm
- No DC blocking capacitors required
- 1kV HBM ESD Protection on all pins

Product Applications

- 2G/3G/4G antenna diversity
- Cellular modems and USB Devices

Product Description

The LX8666 is a Silicon On Insulator (SOI) Single Pole, Six Throw (SP6T) antenna switch with a Mobile Industry Processor Interface (MIPI) which require very low insertion loss, high isolation and high linearity performance.

The LX8666 is manufactured in a compact 2.0mm x 2.0mm x 0.55mm, 14-pin surface mount Quad Flat No-Lead (QFN) package.

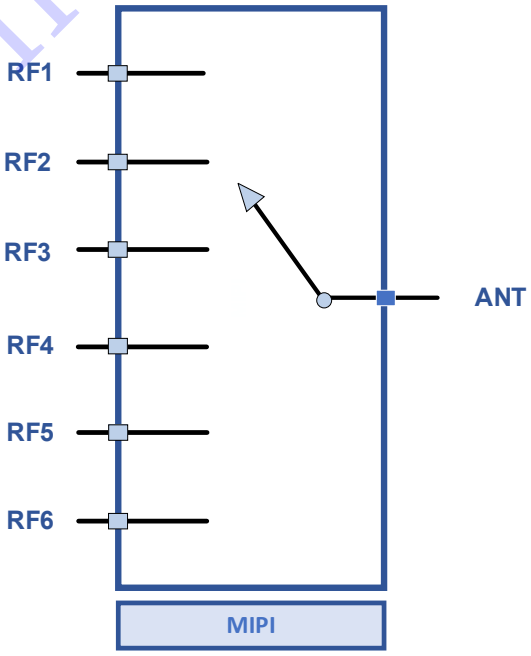


Figure 1 Functional Block Diagram

Pin Configuration (Top View)

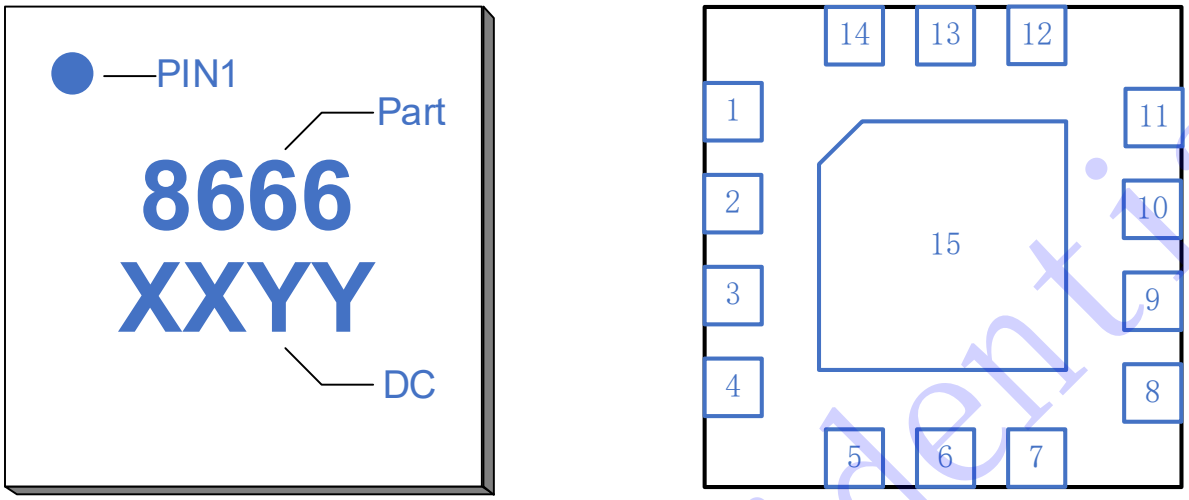


Figure 2 Pin Configuration (Top View)

Pin Descriptions

Table 1:

NO.	Name	Description	NO.	Name	Units
1	RF5	RF Port5	9	RF2	RF Port2
2	RF3	RF Port3	10	RF4	RF Port4
3	RF1	RF Port1	11	RF6	RF Port6
4	VDD	Power Supply Voltage	12	GND	Ground
5	VIO	RFFE Reference Voltage	13	ANT	Antenna Port
6	SDATA	RFFE Data Bus	14	GND	Ground
7	SCLK	RFFE Clock Bus	15	GND	Ground
8	GND	Ground			

Function Characteristics

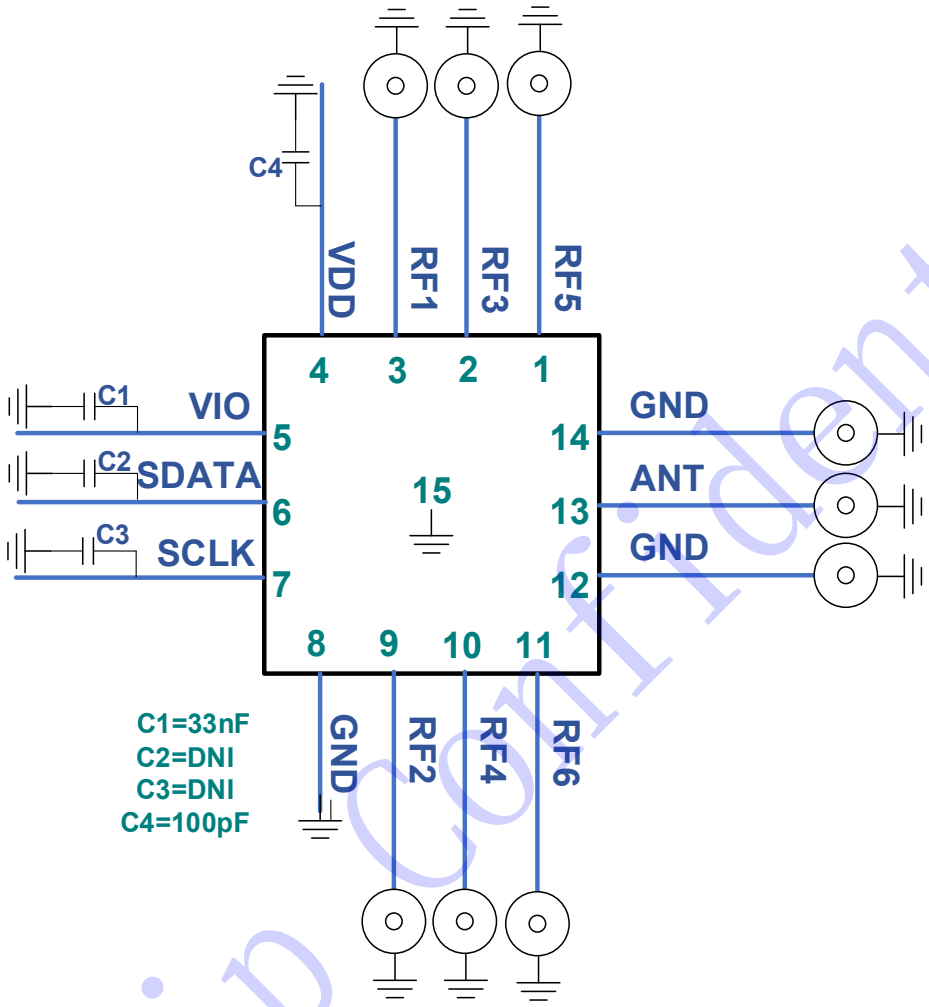


Figure 3 Evaluation Board Schematic

0x00[7:0] (Register_0) for RF Operating Mode

Table 2:

state	Mode	Register_0							
		D7	D6	D5	D4	D3	D2	D1	D0
1	RF5	0	0	0	0	0	0	0	1
2	RF3	0	0	0	0	1	1	1	0
3	RF1	0	0	0	0	0	0	1	0
4	RF6	0	0	0	0	1	0	0	1
5	RF4	0	0	0	0	0	1	0	0
6	RF2	0	0	0	0	1	0	0	0

Absolute Maximum Conditions

Table 3:

Parameters	Symbol	Min	Max	Units	Conditions
DC Power Supply	V_{DD}	2.4	4.8	V	T_A=25°
Digital control signal	V_{IO}	1.3	2	V	T_A=25°
Max RF Input Power (ANT to RF1~8)	P_{INMAX}		36	dBm	F_0=950MHz,20% DC, VSWR=1.:1,T_A=25°
Device Operating Temperature	T_{OP}	-40	+90	℃	
Device Storage Temperature	T_{STG}	-55	+150		
Electrostatic Discharge (All Pins)	$V_{ESD(HBM)}$	1000		V	Human Body Model
	$V_{ESD(CDM)}$	500			Charged Device Model

Notices: *Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.*

Recommended Operating Conditions

Table 4:

Parameters	Symbol	Min	Typ	Max	Units
Operating Frequency	F_0	0.4		2.7	GHz
DC Supply Voltage	V_{DD}	2.5	2.8	4.2	V
RFFE Reference Supply	V_{IO}	1.65	1.8	1.95	V
RFFE Bus Voltage (SDATA, SCLK) High	V_{IH}	0.8*VIO	VIO	VIO	V
RFFE Bus Voltage (SDATA, SCLK) Low	V_{IL}	0	0	0.2*VIO	V

DC Performances

Table 5:

Parameters	Symbol	Test Condition	Min.	Typ.	Max.	Units
DC Supply Current	I_{DD}			50	90	uA
Current on VIO	I_{IO}			4	10	uA

(T_A=25℃, V_{DD}=2.8V, V_{IO}=1.8V, V_{IH}=0V, P_{IN}=0dBm, Z_0=50Ω, unless otherwise noted.)

Timing Performances

Table 6:

Parameters	Symbol	Test Condition	Min.	Typ.	Max.	Units
Switching Time	T_{SW}	50% of SCLK to 10%/90% of final RF		1	2	us
Wake Up Time	T_{WK}	Cold Start, 50% VIO to 90% RF		10	20	
Turn On Time	T_{ON}	Exiting Lower Power State (50%SCLK) to 90% RF Input		10	20	

(T_A=25℃, V_{DD}=2.8V, V_{IO}=1.8V, V_{IH}=0V, P_{IN}=0dBm, Z_0=50Ω, unless otherwise noted.)

RF Performances

Table 7:

Parameters	Symbol	Test Condition	Min.	Typ.	Max.	Units
Insertion loss (ANT to RFX)	IL	F_0=0.4 to 1.0GHz F_0=1.0 to 2.0GHz F_0=2.0 to 2.7GHz		0.38 0.45 0.60	0.42 0.55 0.85	dB
Isolation (ANT to RFX)	ISO	F_0=0.4 to 1.0GHz F_0=1.0 to 2.0GHz F_0=2.0 to 2.7GHz	32 25 23	42 30 28		dB
Return Loss		F_0=0.4 to 1.0GHz F_0=1.0 to 2.0GHz F_0=2.0 to 2.7GHz	24 17 14	30 22 17		dB
Input 0.1dB Compression point (ANT to RFx)	$P_{0.1dB}$	F_0=900MHz, 20%DC		36		dBm
2nd Order Harmonic	$2F_0$	Pin = +26 dBm,900MHz Pin = +35 dBm,900MHz		-94 -82		dBm
3rd Order Harmonic	$3F_0$	Pin = +26 dBm,900MHz Pin = +35 dBm,900MHz		-92 -82		

(T_A=25℃, V_{DD}=2.8V, V_{IO}=1.8V, V_{IH}=0V, P_{IN}=0dBm, Z_0=50Ω, unless otherwise noted.)

MIPI RFFE Commands

MIPI RFFE V2.1 interface supports the following Command Sequences:

• Register Write

• Register Read

• Register_0 Write

Figure 4 and Figure 5 illustrate the timing diagrams for register write command sequence and read command sequence, respectively. Figure 6 describes the Register_0 write command sequence. In the below timing figures, SA[3:0] is the slave address. A[4:0] is the register address. D[7:0] is the data. “P” is a parity bit.

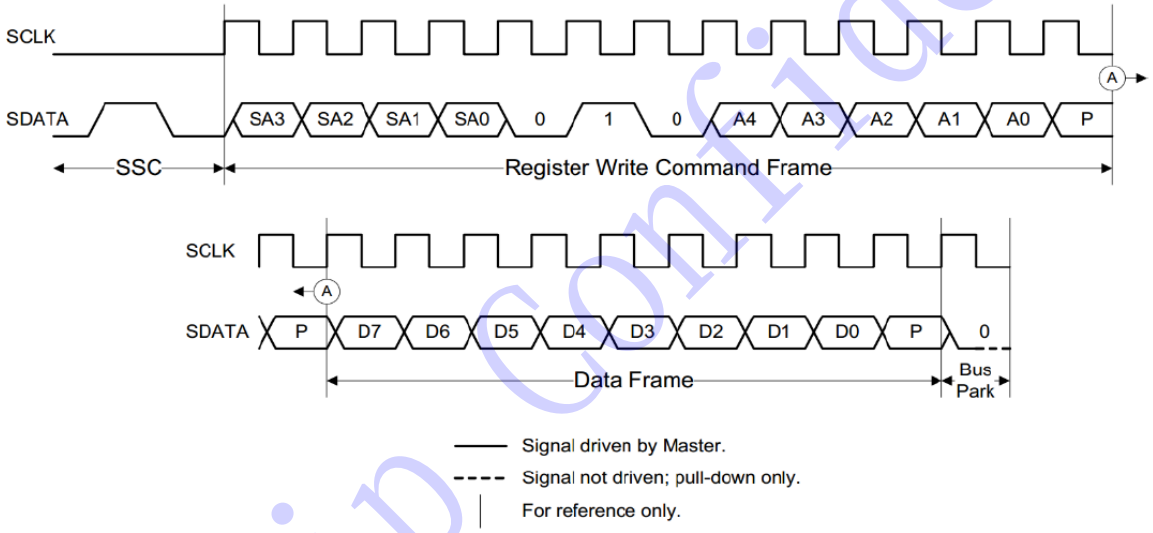


Figure 4 Register Write Command Sequence

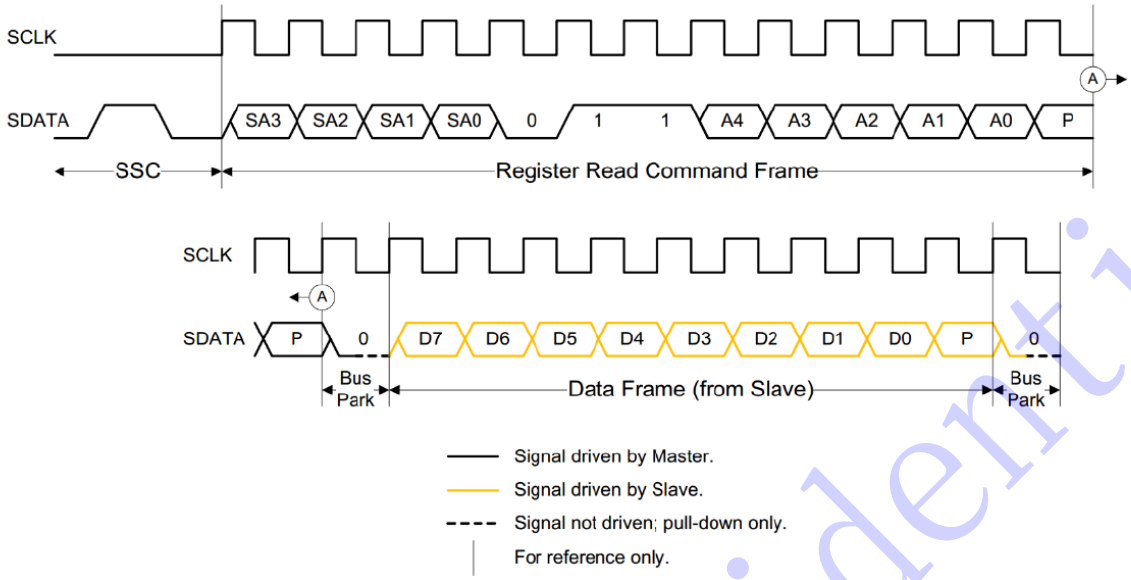


Figure 5 Register Read Command Sequence

Figure 6 shows the Register_0 Write Command Sequence. The Command Sequence starts with an SSC, followed by the Register 0 Write Command Frame containing the Slave address, a logic '1' (to denote the command type and address), and an only seven-bit word to be written into Register 0. The Command Sequence ends with a Bus Park Cycle.

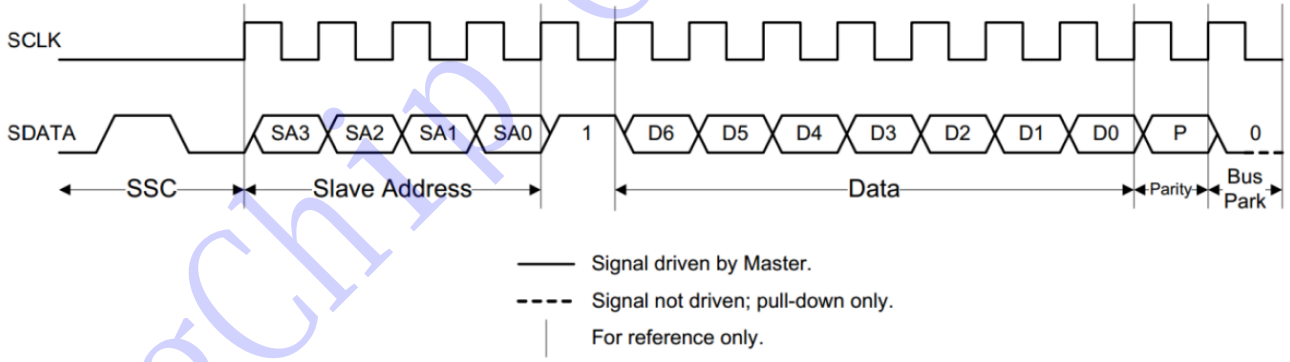


Figure 6 Register_0 Write Command Sequence

Other information such as MIPI USID programming sequences, MIPI bus specifications, etc. can be referred to the MIPI Alliance Specification for RF Front-End Control Interface (RFFE), V2.1 (18-DEC-2017).

Register Definition

Table 8:

Register 0, Address: 0x00 (MODE_CTRL)				
Register 0	**Description**	**Default**	**Notes**	**Trig**
[7:0]	MODE_CTRL	0x0	Switch control. See Truth Table	0
Register 1B, Address: 0x1B				
Register 1B	**Description**	**Default**	**Notes**	**Trig**
[7:4]	Reserved	0x0	Reserved	No
[3:0]	GSID	0x0	Group slave ID	No
Register 1C Address: 0x1C (PM_TRIG)				
Register 1C	**Description**	**Default**	**Notes**	**Trig**
[7:6]	PWR_MODE	0x1	00 = Normal Operation (ACTIVE) 01 = Default Settings (STARTUP) 10 = Low Power (LOW POWER) 11 = Reserved	No
[5]	Trigger Mask 2	0x0	Trigger Enable: 0 Trigger Disable: 1	No
[4]	Trigger Mask 1	0x0	Trigger Enable: 0 Trigger Disable: 1	No
[3]	Trigger Mask 0	0x0	Trigger Enable: 0 Trigger Disable: 1	No
[2]	Trigger Register 2	0x0	1 = Latch Register 2 contents	No
[1]	Trigger Register 1	0x0	1 = Latch Register 1 contents	No
[0]	Trigger Register 0	0x0	1 = Latch Register 0 contents	No
Register1D, Address: 0x01D (PM_ID)				
Register1D	**Description**	**Default**	**Notes**	**Trig**
[7:0]	Product ID	0X45	Product ID = 0X45	No
Register 1E, Address: 0x01E (MAN_ID)				
Register 1E	**Description**	**Default**	**Notes**	**Trig**
[7:0]	Manufacturer ID	0x78	Manufacturer ID[7:0] = 0x78	No
Register 1F Address: 0x01F (USID)				
Register 1F	**Description**	**Default**	**Notes**	**Trig**
[7:4]	Manufacturer ID	0x04	Manufacturer ID [11:8]	No
[3:0]	User ID	0xA	The default value at reset is selected via pin USID.	No

Evaluation Board

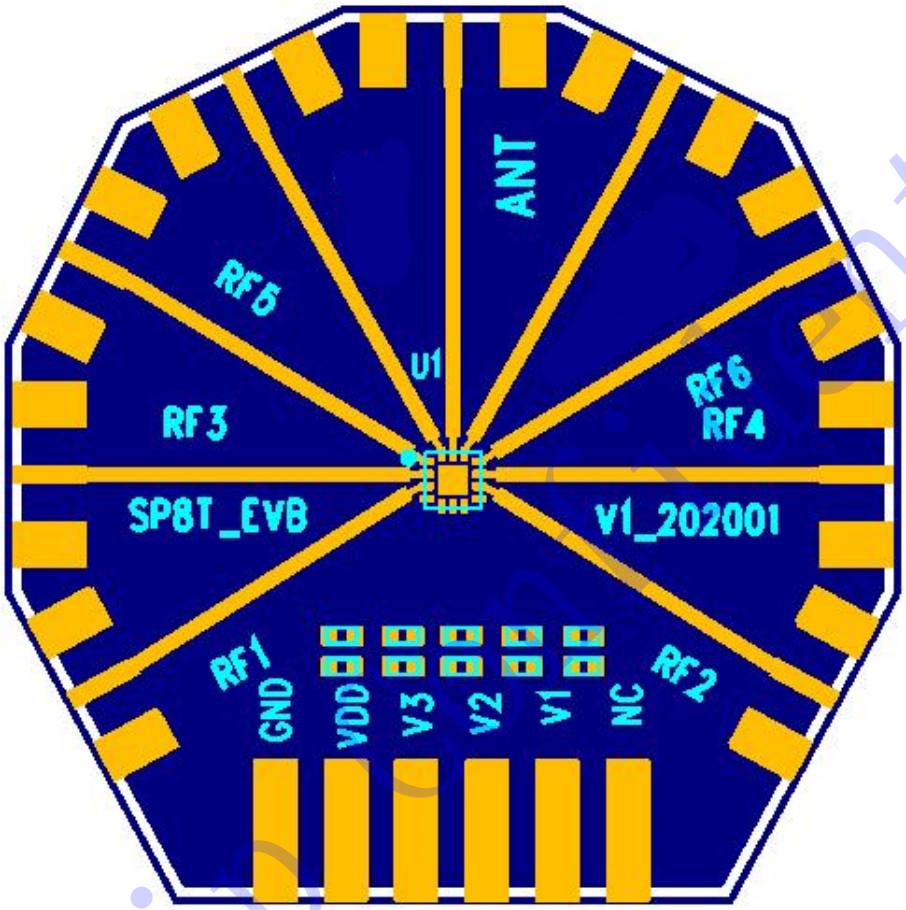
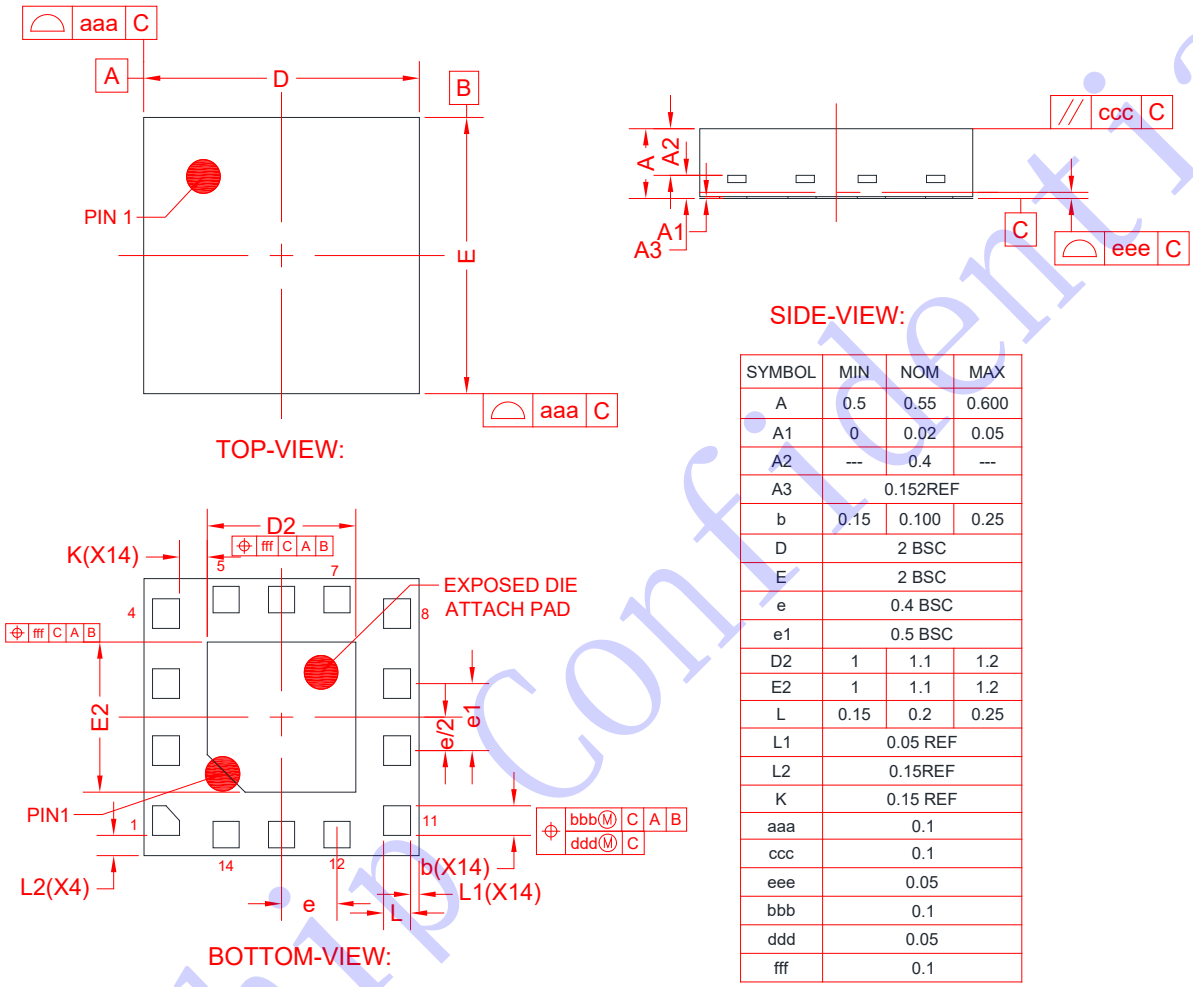


Figure 7 Evaluation Board Assembly Diagram

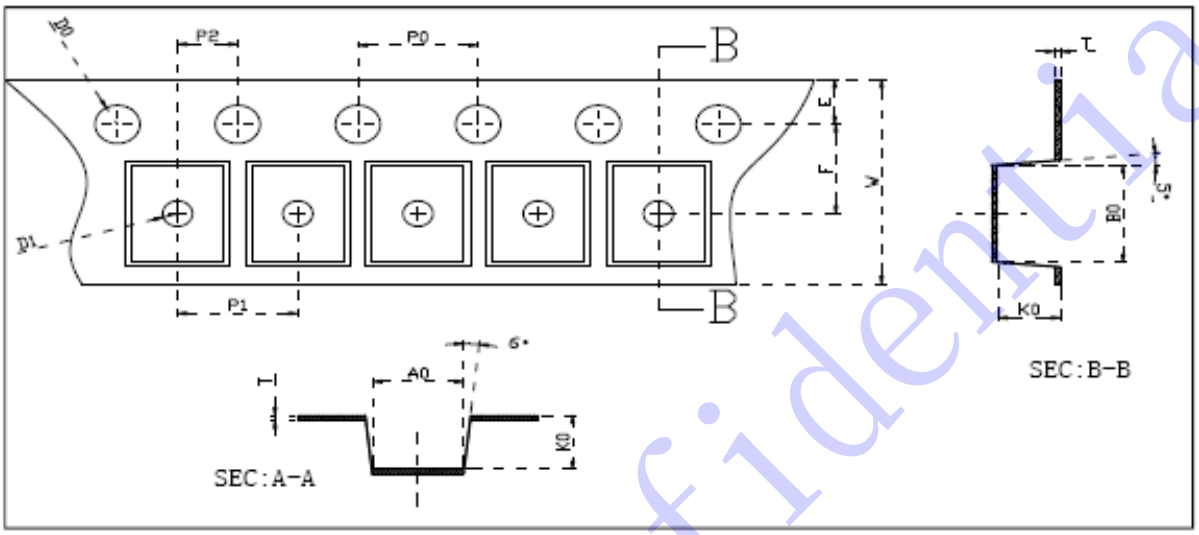
Package Outline Dimension



SYMBOL	MIN	NOM	MAX
A	0.5	0.55	0.600
A1	0	0.02	0.05
A2	---	0.4	---
A3		0.152REF	
b	0.15	0.100	0.25
D		2 BSC	
E		2 BSC	
e		0.4 BSC	
e1		0.5 BSC	
D2	1	1.1	1.2
E2	1	1.1	1.2
L	0.15	0.2	0.25
L1		0.05 REF	
L2		0.15REF	
K		0.15 REF	
aaa		0.1	
ccc		0.1	
eee		0.05	
bbb		0.1	
ddd		0.05	
fff		0.1	

Figure 8 Package Outline Dimension

Package Dimensions (5000pcs)



W	8.00±0.10	T	0.20±0.05	D1	1.00±0.10	单位	MM
E	1.75±0.10	F	3.50±0.10	D0	1.50±0.10	材质	PC+PS
P0	4.00±0.10	P1	4.00±0.10	P2	2.00±0.10		
A0	2.18±0.10	B0	2.20±0.10	K0	0.75±0.10		

Figure 9 Tape and Reel Dimensions

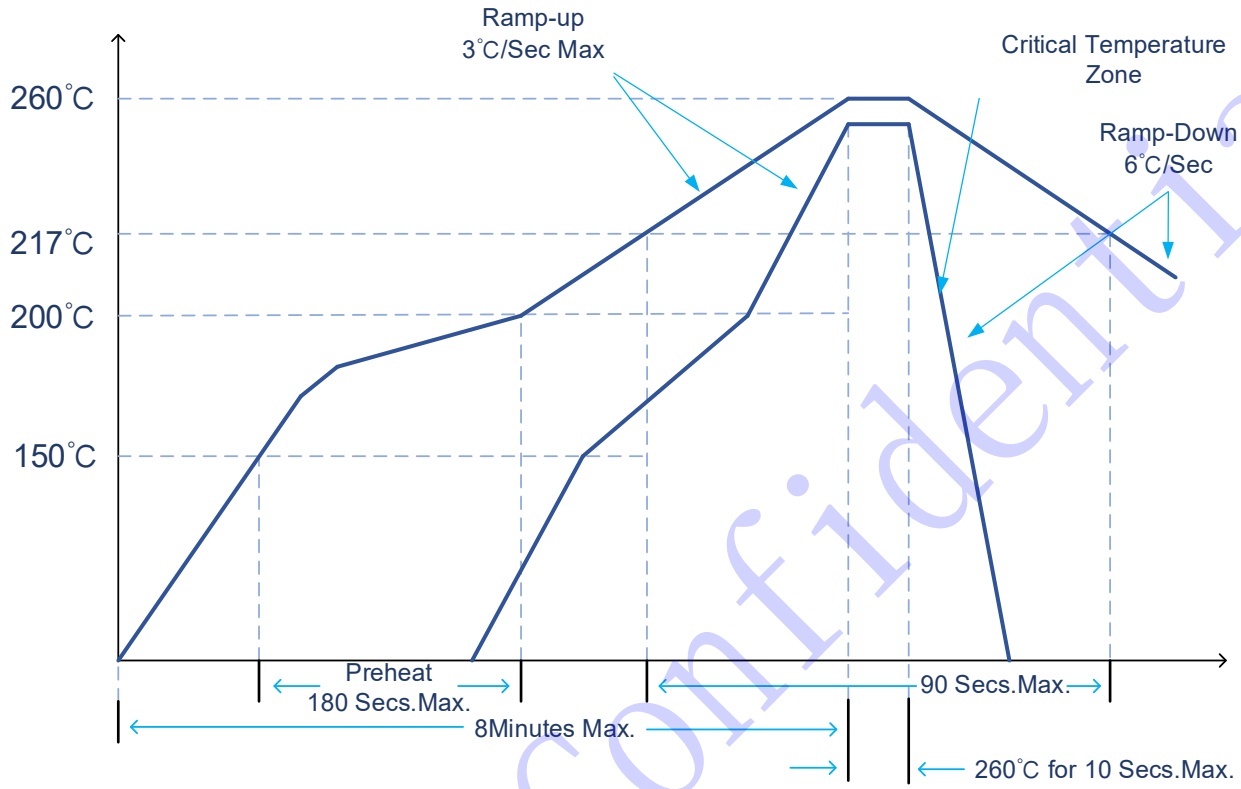
Declaration of No Harmful Substances

This part is compliant with 2005/20/EC packaging directive, 1907/2006/EC REACH directive and the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead free
- Halogen Free (Chlorine, Bromine)
- SVHC Free

Reflow Chart



NOTE: Reflow Profile with 240℃ peak also acceptable.

