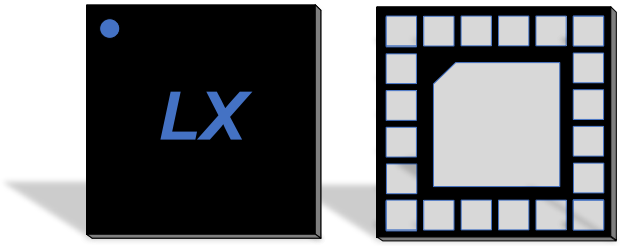


Product Features

- Excellent Insertion Loss and Isolation performance
- High Linearity
- RFFE 2.1 Control Interface
- Broadband frequency range: 0.1 to 3 GHz
- Small package: QFN-20 2.5mm x 2.5mm x 0.45mm
- No DC blocking capacitors required
- 1kV HBM ESD Protection on all pins

Product Applications

- 4G multimode cellular tablets and Multi-Mode GSM, EDGE, WCDMA, LTE
- Diversity antenna switching

Product Description

The LX86C0 is a Silicon On Insulator (SOI) Single Pole, Twelve Throw (SP12T) antenna switch with a Mobile Industry Processor Interface (MIPI) which require very low insertion loss, high isolation and high linearity performance.
The LX86C0 is manufactured in a compact 2.5mm x 2.5mm x 0.45mm, 20-pin surface mount Quad Flat No-Lead (QFN) package.

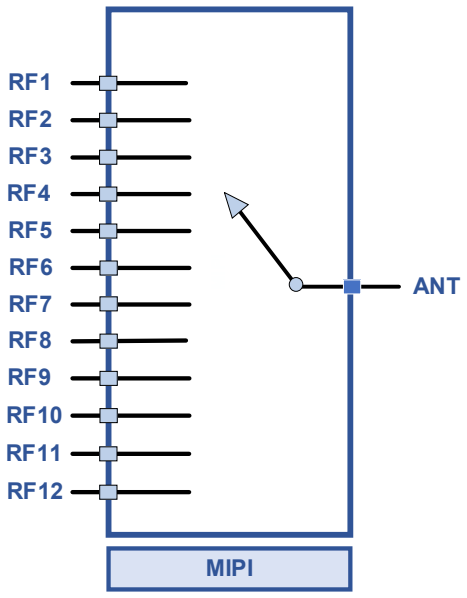


Figure 1 Functional Block Diagram

Absolute Maximum Conditions

Parameters	Symbol	Minimum	Maximum	Units
Supply voltage	V_{DD}	2.5	3.6	V
Digital control signal	V_{IO}		2	V
RF input power	Pin		+37	dBm
Storage temperature	T_{STG}	-55	+150	℃
Operating temperature	T_{OP}	-40	+90	℃
Human Body Model, Class 1C	ESD	1000		V

1: Test condition 50% duty cycle, VSWR=1:1, +25 ° C

Note: *Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.*

General Electrical Specifications

Parameters	Symbol	Test Condition	Min.	Typ.	Max.	Units
Supply voltage	V_{DD}		2.5	2.8	3.6	V
Supply current, active mode	I_{DD}		100		150	μA
Interface supply	VIO		1.65	1.8	2	V
Interface signal: High Low			 0.8 x VIO 0	 VIO 0	 2 0	V
Control current: High Low	I_{CTL}		5		15	μA
Turn-on time (PIN = +27 dBm)	T_{ON}	Measured from 50% of final VDD supply voltage to 90% of RF power		20		μs
Switching time (PIN = +27 dBm)	T_{SW}	Measured from 50% of final VDD supply voltage to 90% of RF power		2	5	μs

(VDD = 2.8 V, VIO = 1.8 V, TOP = +25 ℃, Characteristic Impedance [ZO] = 50 Ω, Unless Otherwise Noted)

RF Specifications

Parameters	Symbol	Test Condition	Min.	Typ.	Max.	Units
Operating frequency	f		0.1		3	GHz
Insertion loss	IL	Up to 1.0 GHz Up to 2.0 GHz Up to 2.7 GHz		0.51 0.61 0.66		dB
Isolation (ANT port to any receive port)	Iso	Up to 1.0 GHz Up to 2.0 GHz Up to 2.7 GHz	35 23 20	38 25 23		dB
Return loss	RL	All ports, up to 1.0 GHz All ports, up to 2.0 GHz All ports, up to 2.7 GHz	23 20 15	26 23 18		dB
2nd Order harmonics	2fo	Pin = +26 dBm,900MHz	-80	-86		dBm
3rd Order harmonics	3fo	Pin = +26 dBm,900MHz	-70	-74		dBm
2nd Order harmonics	2fo	Pin = +30 dBm,900MHz	-72	-78		dBm
3rd Order harmonics	3fo	Pin = +30 dBm,900MHz	-58	-62		dBm
0.1 dB Compression Point 50% duty cycle, VSWR=1:1	P0.1dB	900M, 50Ω		+37		dBm

Truth Table

Reg_1C	Reg_00								ANT-RFX
	D7	D6	D5	D4	D3	D2	D1	D0	
38	x	0	0	0	0	0	0	0	ISO
38	x	0	0	0	1	1	1	1	ISO
38	x	0	0	0	0	1	0	0	ANT-RF1 on
38	x	0	0	0	0	1	1	1	ANT-RF2 on
38	x	0	0	0	1	0	0	1	ANT-RF3 on
38	x	0	0	0	1	0	1	1	ANT-RF4 on
38	x	0	0	0	1	1	0	0	ANT-RF5 on
38	x	0	0	0	0	0	0	1	ANT-RF6 on
38	x	0	0	0	0	0	1	0	ANT-RF7 on
38	x	0	0	0	0	0	1	1	ANT-RF8 on
38	x	0	0	0	1	0	1	0	ANT-RF9 on
38	x	0	0	0	1	0	0	0	ANT-RF10 on
38	x	0	0	0	0	1	0	1	ANT-RF11 on
38	x	0	0	0	0	1	1	0	ANT-RF12 on

MIPI RFFE Commands

MIPI RFFE V2.1 interface supports the following Command Sequences:

- Register Write
- Register Read
- Register_0 Write

Figure 2 and Figure 3 illustrate the timing diagrams for register write command sequence and read command sequence, respectively. Figure 4 describes the Register_0 write command sequence. In the below timing figures, SA[3:0] is the slave address. A[4:0] is the register address. D[7:0] is the data. “P” is a parity bit.

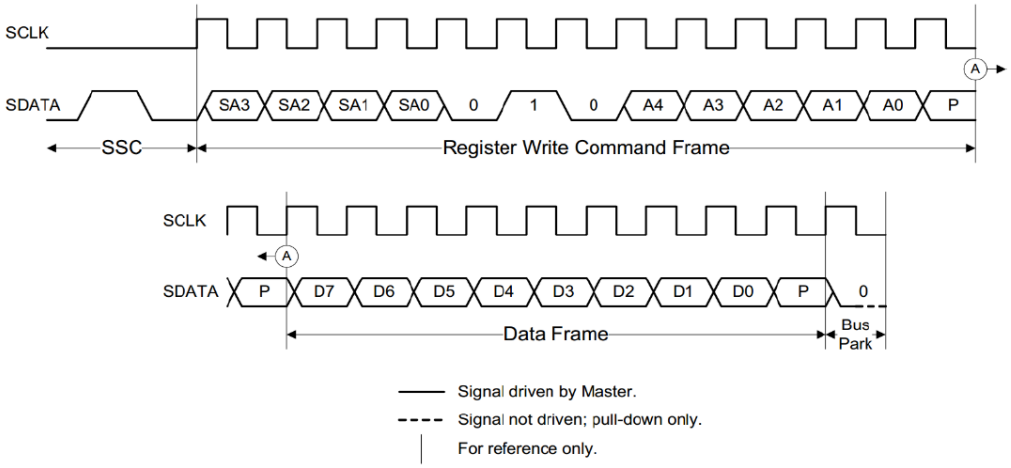


Figure 2 Register Write Command Sequence

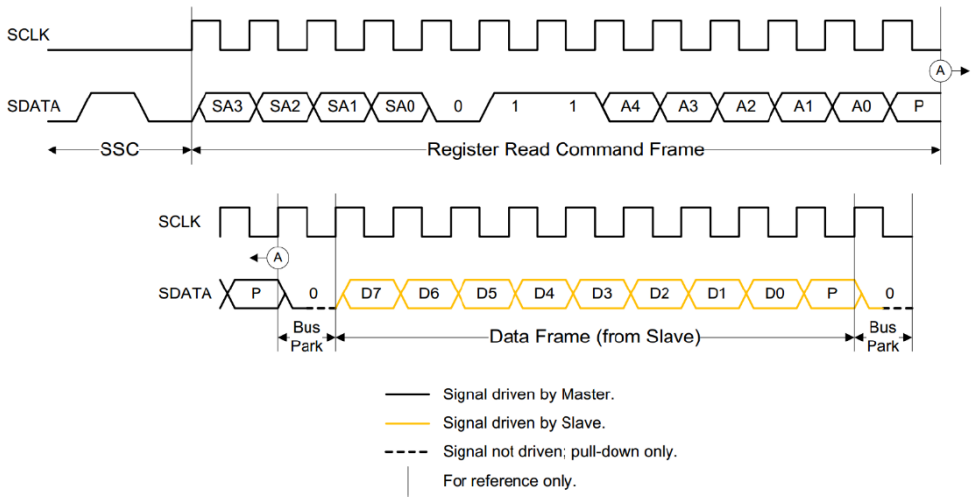


Figure 3 Register Read Command Sequence

Figure 4 shows the Register_0 Write Command Sequence. The Command Sequence starts with an SSC, followed by the Register 0 Write Command Frame containing the Slave address, a logic '1' (to denote the command type and address), and an only seven-bit word to be written into Register 0. The Command Sequence ends with a Bus Park Cycle.

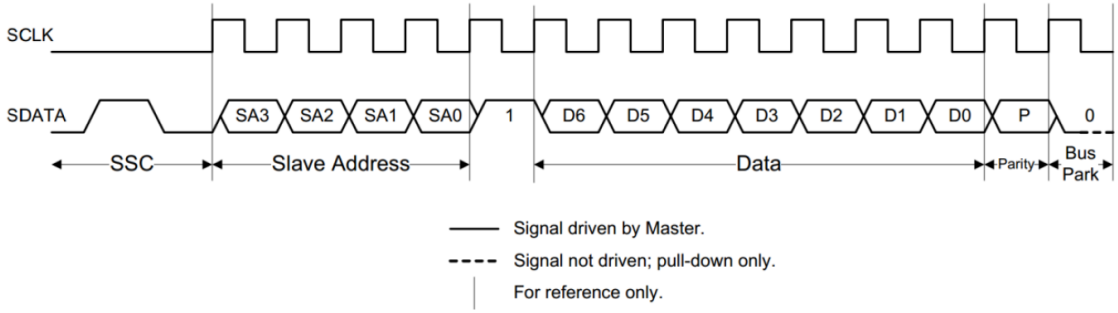


Figure 4 Register_0 Write Command Sequence

Other information such as MIPI USID programming sequences, MIPI bus specifications, etc. can be referred to the MIPI Alliance Specification for RF Front-End Control Interface (RFFE), V2.1 (18-DEC-2017).

Register definition

Register 0, Address: 0x00 (MODE_CTRL)				
Register 0	**Description**	**Default**	**Notes**	**Trig**
[7:0]	MODE_CTRL	0x0	Switch control. See Truth Table	0
Register 1B, Address: 0x1B				
Register 1B	**Description**	**Default**	**Notes**	**Trig**
[7:4]	Reserved	0x00	Reserved	No
[3:0]	GSID	0x00	Group slave ID	No
Register 1C Address: 0x1C (PM_TRIG)				
Register 1C	**Description**	**Default**	**Notes**	**Trig**
[7:6]	PWR_MODE	10	00 = Normal Operation (ACTIVE) 01 = Default Settings (STARTUP) 10 = Low Power (LOW POWER) 11 = Reserved	No
[5]	Trigger Mask 2	0	Trigger Enable: 0 Trigger Disable: 1	No
[4]	Trigger Mask 1	0	Trigger Enable: 0 Trigger Disable: 1	No
[3]	Trigger Mask 0	0	Trigger Enable: 0 Trigger Disable: 1	No
[2]	Trigger Register 2	0	1 = Latch Register 2 contents	No
[1]	Trigger Register 1	0	1 = Latch Register 1 contents	No
[0]	Trigger Register 0	0	1 = Latch Register 0 contents	No
Register1D, Address: 0x01D (PM_ID)				
Register1D	**Description**	**Default**	**Notes**	**Trig**
[7:0]	Product ID	0X5F	Product ID = 0X5F	No
Register 1E, Address: 0x01E (MAN_ID)				
Register 1E	**Description**	**Default**	**Notes**	**Trig**
[7:0]	Manufacturer ID	0x78	Manufacturer ID[7:0] = 0x78	No
Register 1F Address: 0x01F (USID)				
Register 1F	**Description**	**Default**	**Notes**	**Trig**
[7:4]	Manufacturer ID	0x04	Manufacturer ID [11:8]	No
[3:0]	User ID	0xA	The default value at reset is selected via pin USID.	No

Power ON and OFF Sequence

Here is the recommendation about power-on/off sequence in order to avoid damaging the device.

Power ON

- Apply voltage supply - VDD
- Apply logic supply - VIO
- Wait 20μs or longer and then apply MIPI bus signals – SCLK and SDATA
- Wait 2μs or longer after MIPI bus goes idle and then apply the RF Signal

Power OFF

- Remove the RF Signal
- Remove MIPI bus – SCLK and SDATA
- Remove logic supply - VIO
- Remove voltage supply - VDD

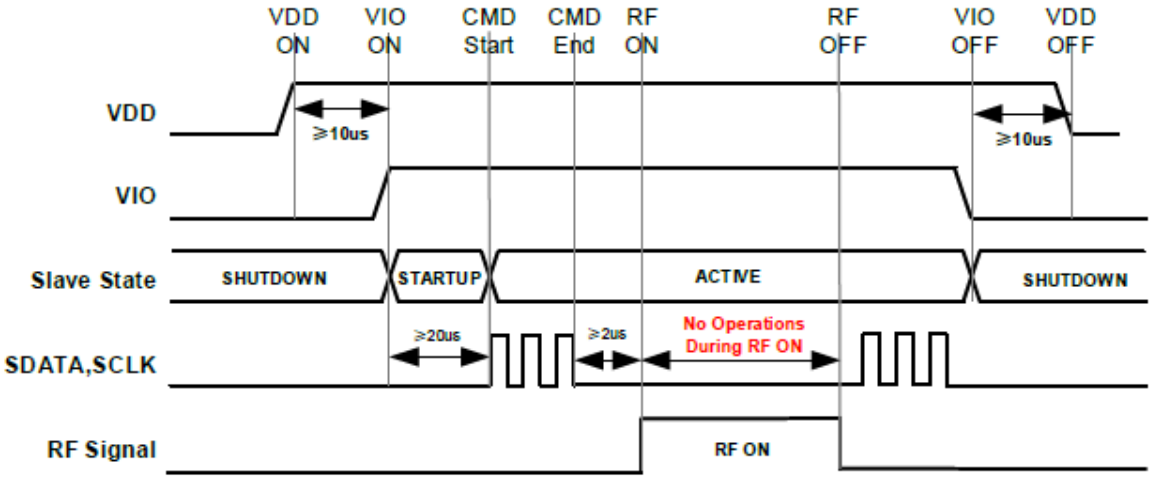


Figure 5 Power On/Off Sequence

Notice

VIO can be applied to the device before VDD or removed after VDD.

It is important to wait 20μs after VIO & VDD are applied before sending SDATA to ensure correction data transmission.

It is strongly recommended that no SDATA/SCLK operations are implemented during RF power on period so as to prevent the device being damaged.

Pin-out Information

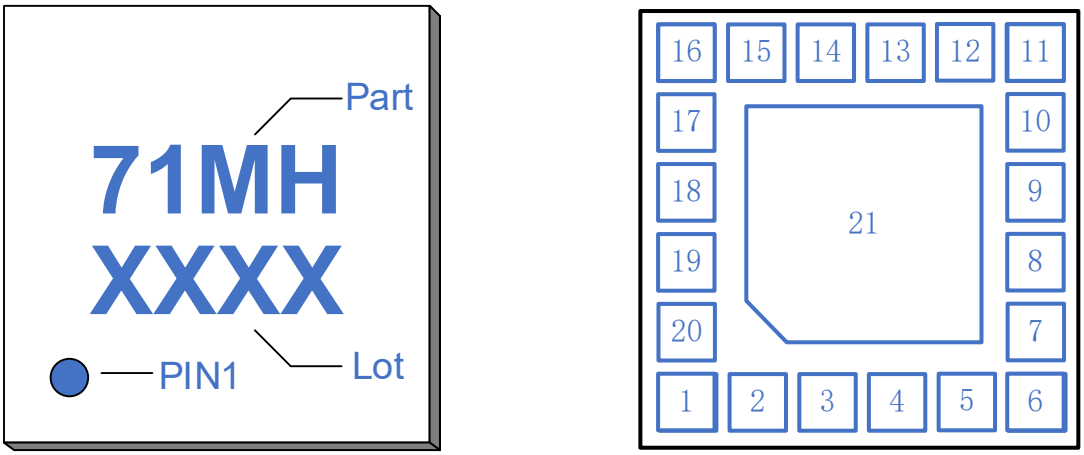


Figure 6 Pin-out Information

Table 1. Pin Description

Pin #	Name	Description	Pin #	Name	Description
1	ANT	Antenna in	12	RF1	RF Port 1
2	RF4	RF Port 4	13	RF8	RF Port 8
3	RF3	RF Port 3	14	RF7	RF Port 7
4	RF2	RF Port 2	15	RF6	RF Port 6
5	RF12	RF Port 12	16	RF5	RF Port 5
6	NC	Not Connect	17	GND	Ground
7	VDD	Supply voltage	18	RF10	RF Port 10
8	VIO	Digital control signal	19	RF9	RF Port 9
9	SDATA	MIPI data input/output	20	GND	Ground
10	SCLK	MIPI clock	21	GND	Ground
11	RF11	RF Port 11			

Application circuit

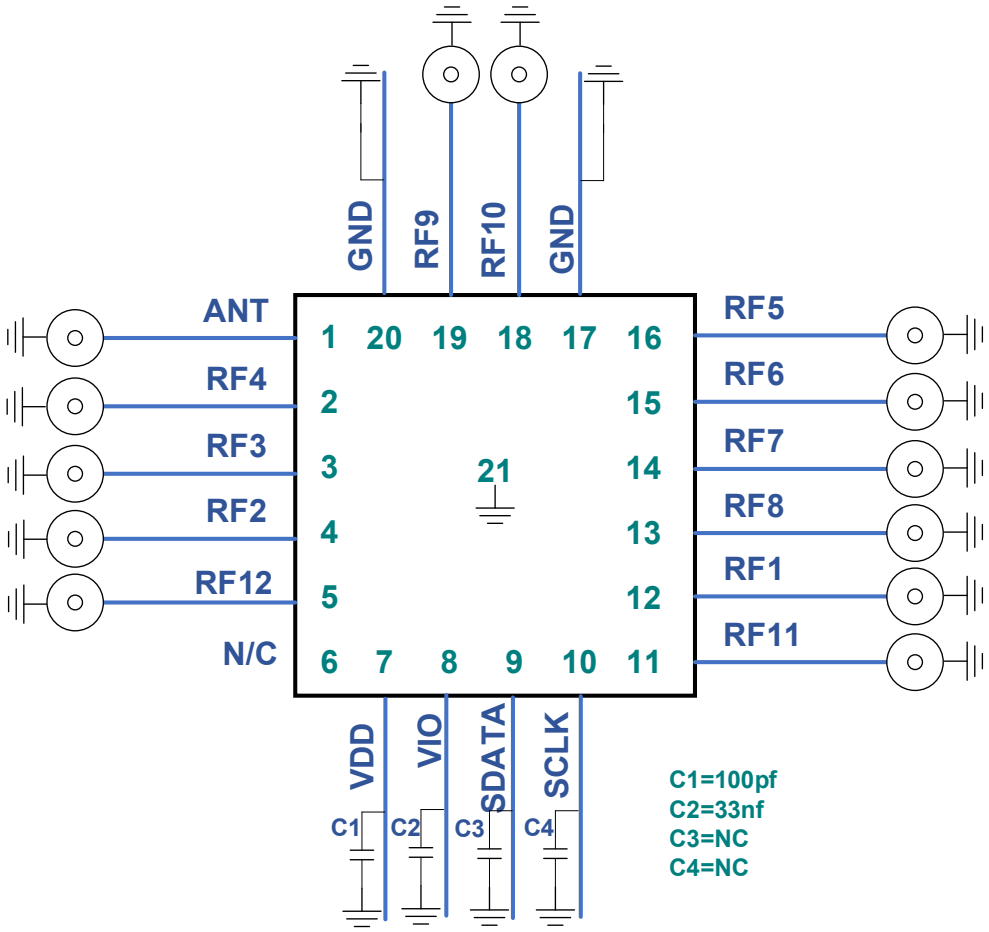


Figure 7 Application circuit

Evaluation Board

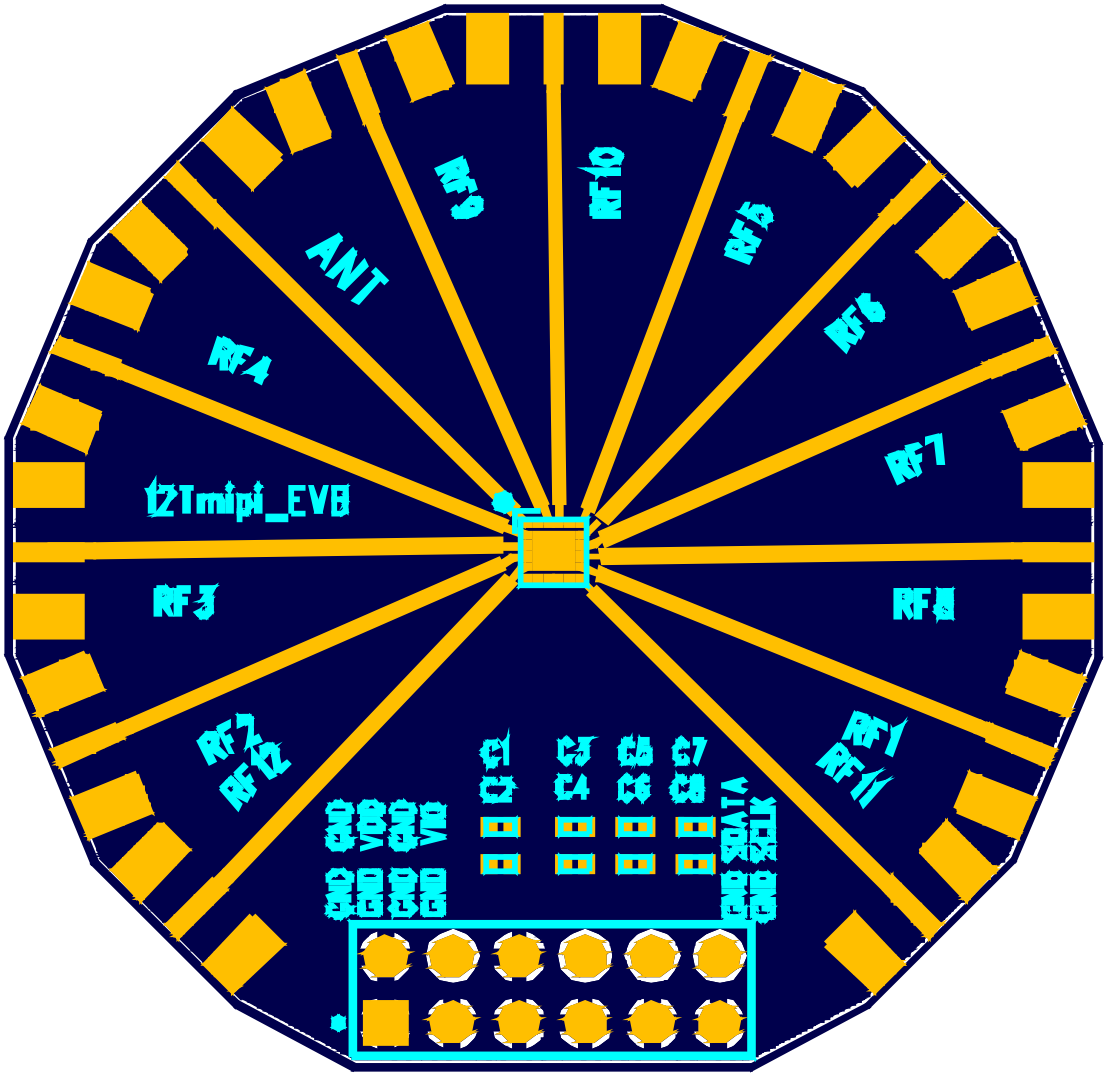
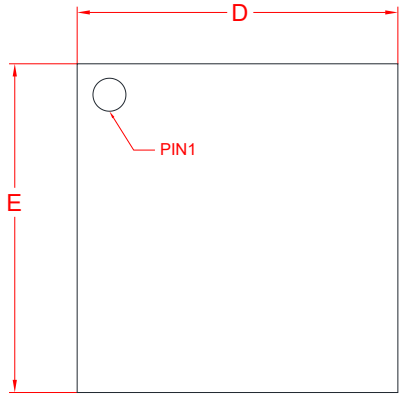
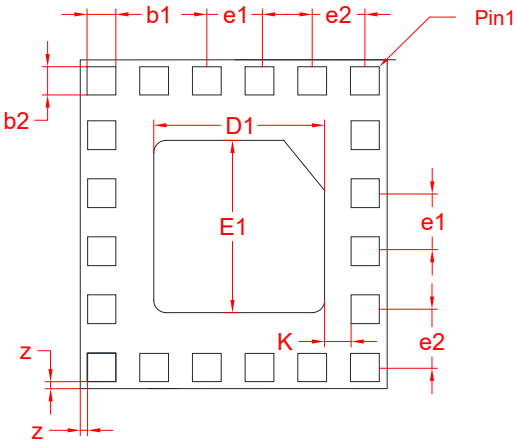


Figure 8 Evaluation Board Assembly Diagram

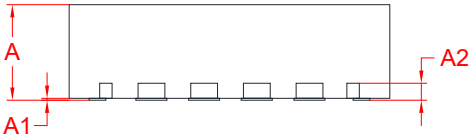
Package Outline Dimension



TOP-VIEW:



BOTTOM-VIEW:



FRONT-VIEW:

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.40	0.45	0.50
A1	0.00	0.02	0.05
A2	0.119	0.127	0.135
b1	0.15	0.20	0.25
b2	0.15	0.20	0.25
D	2.45	2.50	2.55
E	2.45	2.50	2.55
D1	1.29	1.34	1.39
E1	1.29	1.34	1.39
z	0.10REF		
e1	0.35	0.40	0.45
e2*	0.40	0.45	0.50
K	0.23	0.28	0.33

Figure 9 Package Outline Dimension

Package Dimensions (3000pcs)

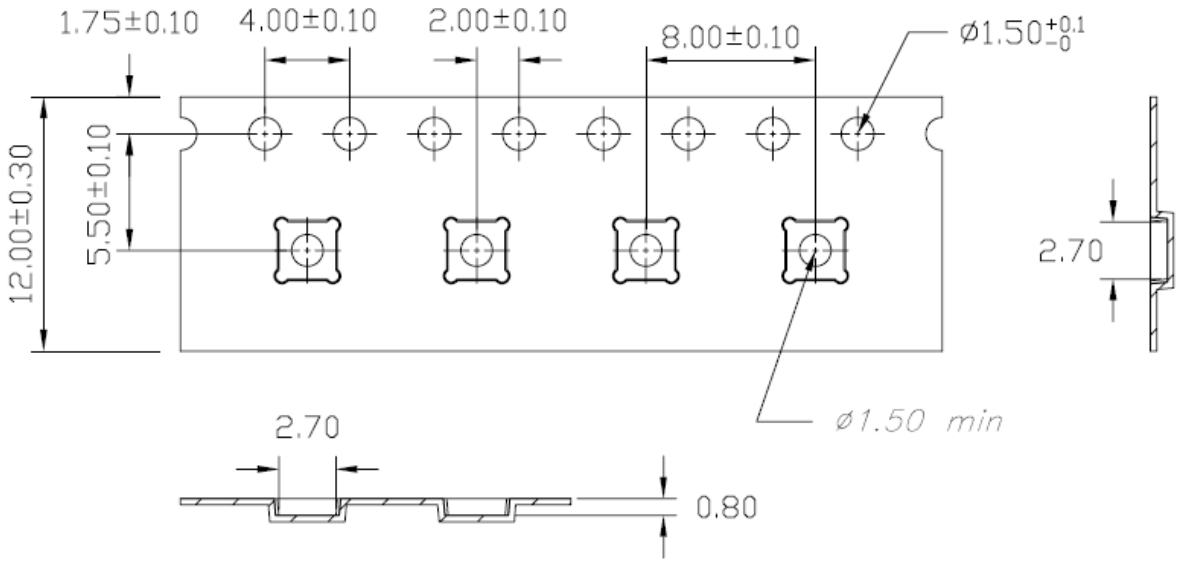


Figure 10 Tape and Reel Dimensions

Declaration of No Harmful Substances

This part is compliant with 2005/20/EC packaging directive, 1907/2006/EC REACH directive and the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

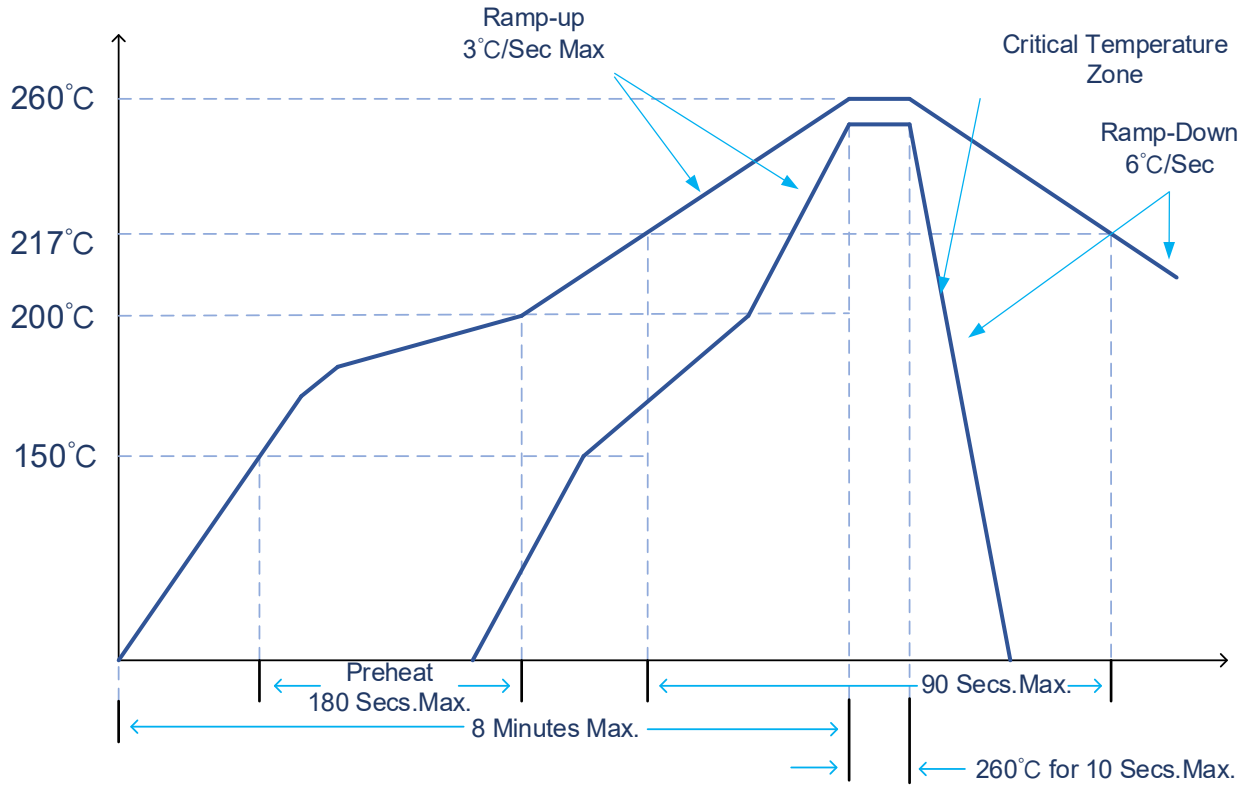
This product also has the following attributes:

• Lead free

• Halogen Free (Chlorine, Bromine)

• SVHC Free

Reflow Chart



NOTE: Reflow Profile with 240˚C peak also acceptable.

