

Product Features

- Excellent Insertion Loss and Isolation performance
- High Linearity
- RFFE 2.1 Control Interface
- Broadband frequency range: 0.1 to 3.8 GHz
- Small package: QFN-20 2.4mm x 2.4mm x 0.45mm
- No DC blocking capacitors required
- 1kV HBM ESD Protection on all pins

Product Applications

- 3G/4G multimode cellular tablets and Multi-Mode GSM, EDGE, WCDMA, LTE
- Diversity antenna switching

Product Description

The LX1660 is a Silicon On Insulator (SOI) Single Pole, Ten-Throw (SP10T) antenna switch with a Mobile Industry Processor Interface (MIPI) which require very low insertion loss, high isolation and high linearity performance.

The high linearity performance and low insertion loss for UMTS, CDMA2000, and LTE applications.

The LX1660 is manufactured in a compact 2.4mm x 2.4mm x 0.45mm, 20-pin surface mount Quad Flat No-Lead (QFN) package.

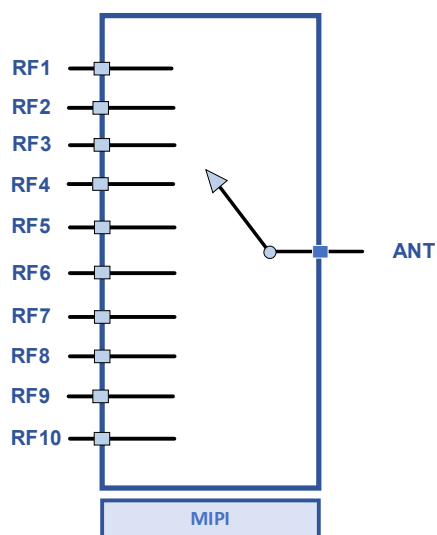


Figure 1 Functional Block Diagram

Absolute Maximum Conditions

Parameters	Symbol	Minimum	Maximum	Units
Supply voltage	V _{DD}	2.4	4.8	V
Digital control signal	V _{IO}	1.3	2	V
RF input power	P _{in}		+36	dBm
Storage temperature	T _{STG}	-55	+150	°C
Operating temperature	T _{OP}	-40	+90	°C
Human Body Model, Class 1C	ESD	1000		V

1: Test condition 50% duty cycle, VSWR=1:1, +25 °C

Note: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

General Electrical Specifications

Parameters	Symbol	Test Condition	Min.	Typ.	Max.	Units
Supply voltage	V _{DD}		2.5	2.8	4.2	V
Supply current, active mode	I _{DD}			80	120	μA
Interface supply	P _{in}		1.65	1.8	1.95	V
Interface signal:						
High			0.8 x V _{IO}	V _{IO}	1.95	V
Low			0	0	0.3	
Control current:						
High	I _{CTL}			5	15	μA
Low						
Switching time (PIN = +27 dBm)	T _{SW}	Measured from 50% of final V _{DD} supply voltage to 90% of RF power		2	3	μs

(V_{DD} = 2.85 V, V_{IO} = 1.8 V, T_{OP} = +25 °C, Characteristic Impedance [Z_O] = 50 Ω, Unless Otherwise Noted)

RF Specifications

Parameters	Symbol	Test Condition	Min.	Typ.	Max.	Units
Operating frequency	f		0.1		3.8	GHz
Insertion loss	IL	Up to 1.0 GHz		0.40	0.45	dB
		Up to 2.0 GHz		0.64	0.65	
		Up to 2.7 GHz		0.88	1.00	
		Up to 3.8 GHz		1.00	1.20	
Isolation (ANT port to any receive port)	Iso	Up to 1.0 GHz	30	34	dB	
		Up to 2.0 GHz	23	28		
		Up to 2.7 GHz	20	25		
		Up to 3.8 GHz	20	24		
2nd Order harmonics	2fo	Pin = +26 dBm,900MHz		-68	-67	dBm
		Pin = +35 dBm,900MHz		-50	-46	
3rd Order harmonics	3fo	Pin = +26 dBm,900MHz		-66	-40	dBm
		Pin = +35 dBm,900MHz		-45		
0.1 dB Compression Point 50% duty cycle, VSWR=1:1	P0.1dB	900M, 50Ω		+36		dBm

Truth Table

Reg_1C	Reg_00								ANT-RFX
	D7	D6	D5	D4	D3	D2	D1	D0	
38	0	0	0	0	0	0	0	0	ISO
38	0	0	0	0	0	0	1	0	ANT-RF1 on
38	0	0	0	0	1	0	1	0	ANT-RF2 on
38	0	0	0	0	1	1	1	0	ANT-RF3 on
38	0	0	0	0	1	0	1	1	ANT-RF4 on
38	0	0	0	0	0	0	0	1	ANT-RF5 on
38	0	0	0	0	1	0	0	1	ANT-RF6 on
38	0	0	0	0	0	1	1	0	ANT-RF7 on
38	0	0	0	0	0	1	0	0	ANT-RF8 on
38	0	0	0	0	1	1	0	0	ANT-RF9 on
38	0	0	0	0	1	0	0	0	ANT-RF10 on

Register definition

Register 0, Address: 0x00 (MODE_CTRL)				
Register 0	Description	Default	Notes	Trig
[7:0]	MODE_CTRL	0x0	Switch control. See Truth Table	Yes
Register 1B, Address: 0x1B				
Register 1B	Description	Default	Notes	Trig
[7:4]	Reserved	0000	Reserved	No
[3:0]	GSID	0000	Group slave ID	No
Register 1C Address: 0x1C (PM_TRIG)				
Register 1C	Description	Default	Notes	Trig
[7:6]	PWR_MODE	0b10	00 = Normal Operation (ACTIVE) 01 = Default Settings (STARTUP) 10 = Low Power (LOW POWER) 11 = Reserved	No
[5]	Trigger Mask 2	0	Trigger Enable: 0 Trigger Disable: 1	No
[4]	Trigger Mask 1	0	Trigger Enable: 0 Trigger Disable: 1	No
[3]	Trigger Mask 0	0	Trigger Enable: 0 Trigger Disable: 1	No
[2]	Trigger Register 2	0	1 = Latch Register 2 contents	No
[1]	Trigger Register 1	0	1 = Latch Register 1 contents	No
[0]	Trigger Register 0	0	1 = Latch Register 0 contents	No
Register 1D, Address: 0x01D (PM_ID)				
Register 1D	Description	Default	Notes	Trig
[7:0]	Product ID	0X45	Product ID = 0X45	No
Register 1E, Address: 0x01E (MAN_ID)				
Register 1E	Description	Default	Notes	Trig
[7:0]	Manufacturer ID	0x78	Manufacturer ID [7:0] = 0x78	No
Register 1F Address: 0x01F (USID)				
Register 1F	Description	Default	Notes	Trig
[7:4]	Manufacturer ID	0x04	Manufacturer ID [9:8] = 0x04	No
[3:0]	User ID	0xA	The default value at reset is selected via pin USID.	No

Pin-out Information

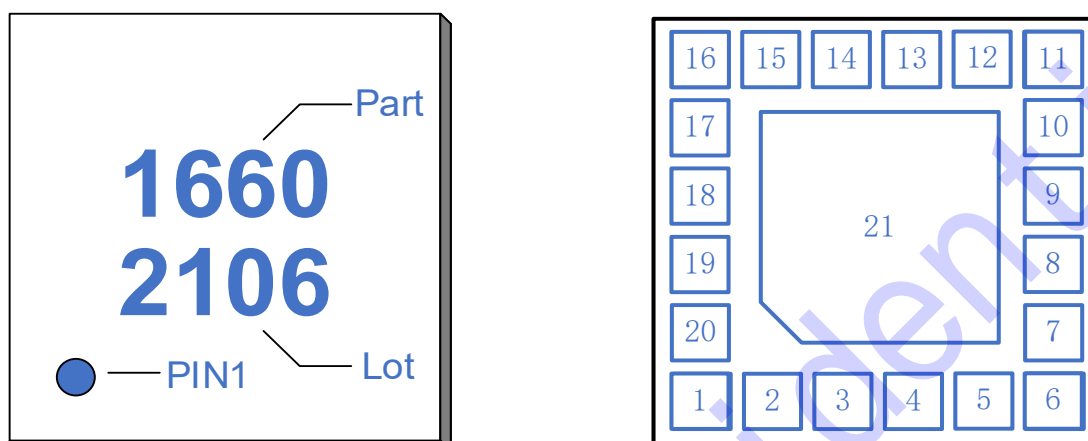


Figure 2 Pin-out Information

Table 1. Pin Description

Pin #	Name	Description	Pin #	Name	Description
1	NC	Not Connect	12	RF4	RF Port 4
2	RF10	RF Port 10	13	RF3	RF Port 3
3	RF9	RF Port 9	14	RF2	RF Port 2
4	RF8	RF Port 8	15	RF1	RF Port 1
5	RF7	RF Port 7	16	GND	Ground
6	RF6	RF Port 6	17	VDD	Power supply
7	GND	Ground	18	VIO	Supply voltage
8	GND	Ground	19	SDATA	Data input/output
9	ANT	Antenna port	20	SCLK	Clock
10	GND	Ground	21	GND	Ground
11	RF5	RF Port 5			

Application circuit

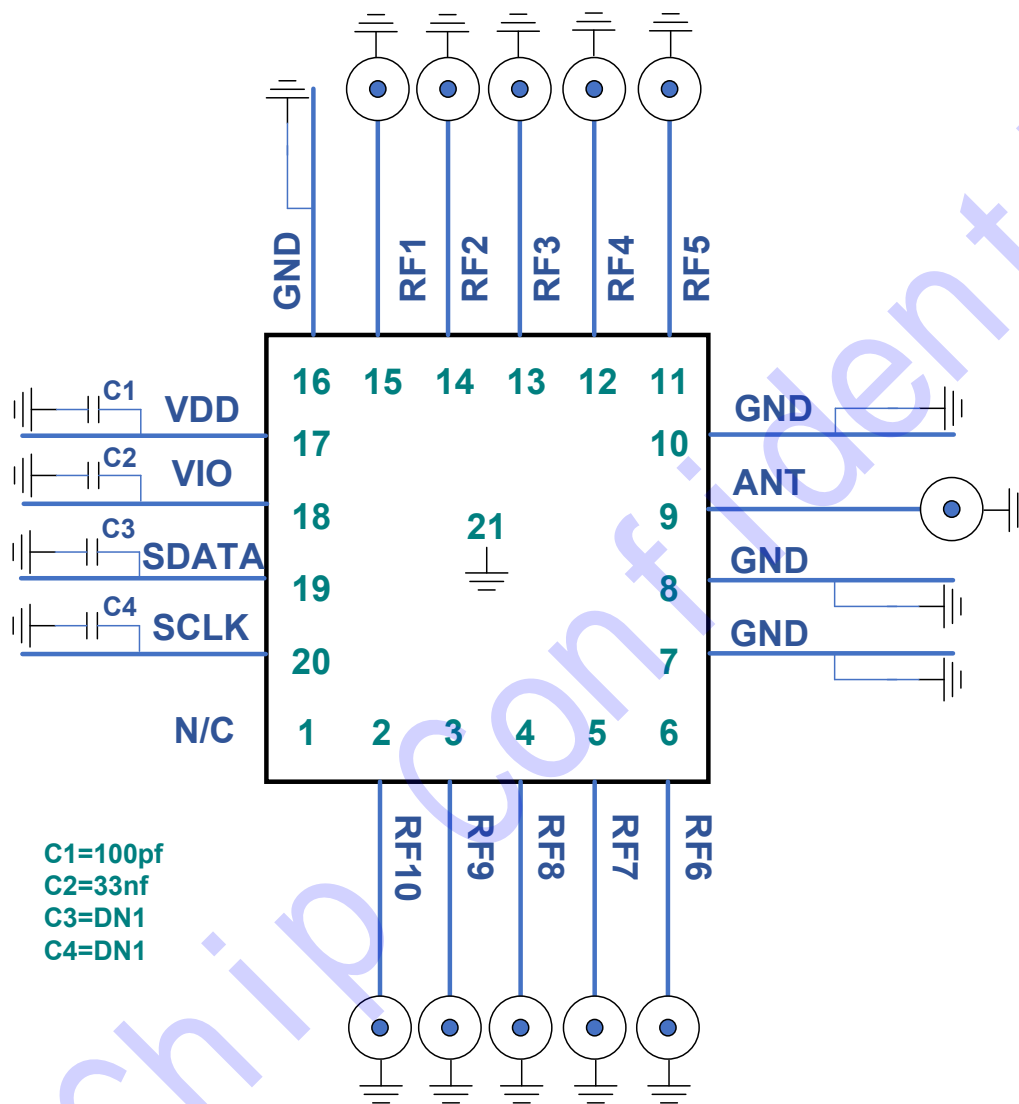


Figure 3 Application circuit

Evaluation Board

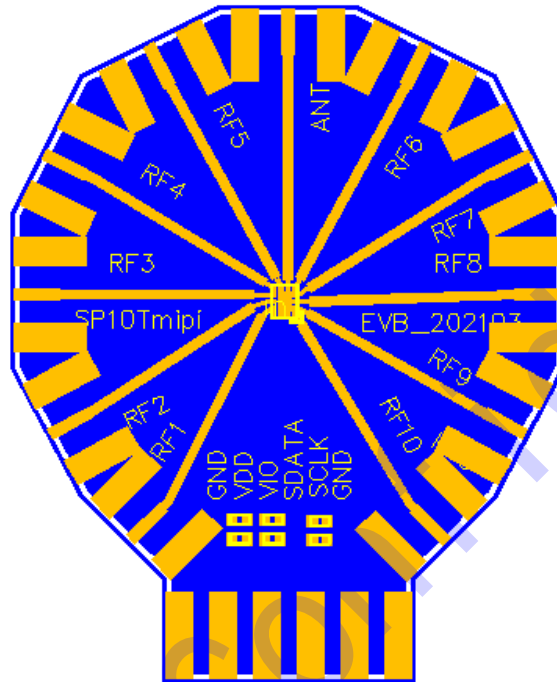
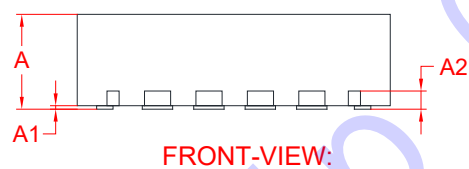
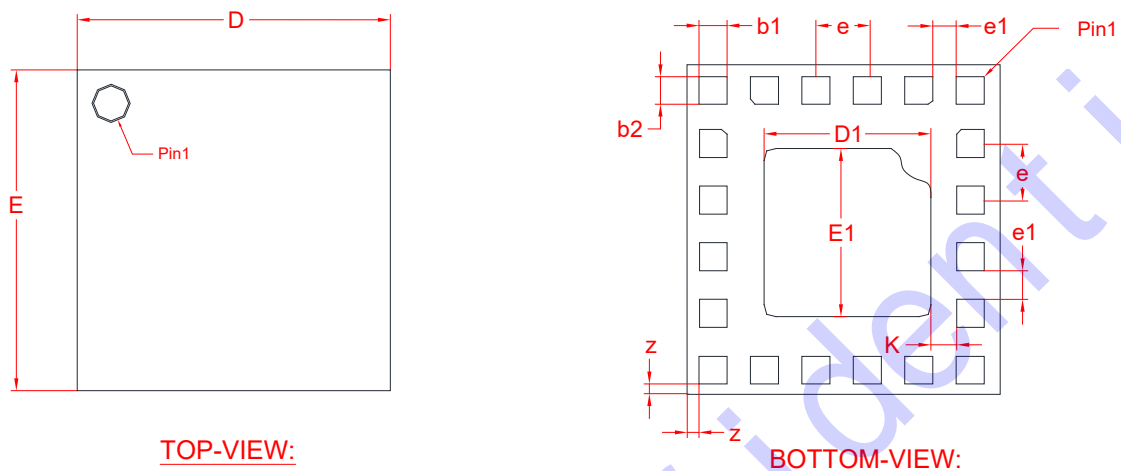


Figure 4 Evaluation Board Assembly Diagram

Package Outline Dimension



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.40	0.45	0.50
A1	0.00	0.02	0.05
A2	0.119	0.127	0.135
b1	0.15	0.20	0.25
b2	0.15	0.20	0.25
D	2.35	2.40	2.45
E	2.35	2.40	2.45
D1	1.25	1.30	1.35
E1	1.25	1.30	1.35
e	0.35	0.40	0.45
e1	0.15	0.20	0.25
z	0.10REF		
K	0.20	0.25	0.30

Figure 5 Package Outline Dimension

Package Dimensions (3000pcs)

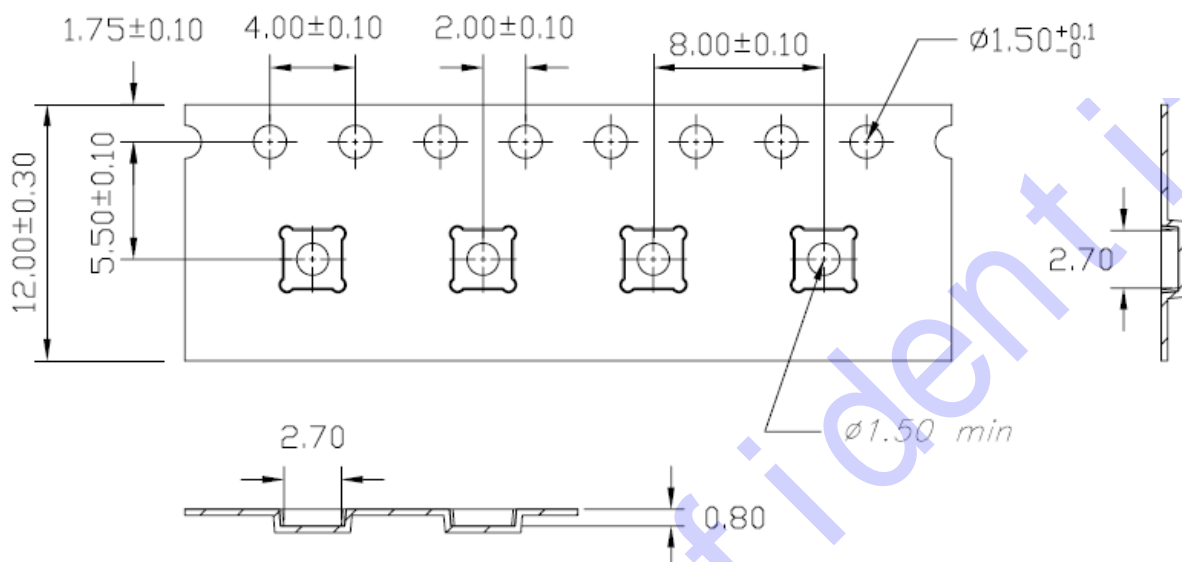


Figure 6 Tape and Reel Dimensions

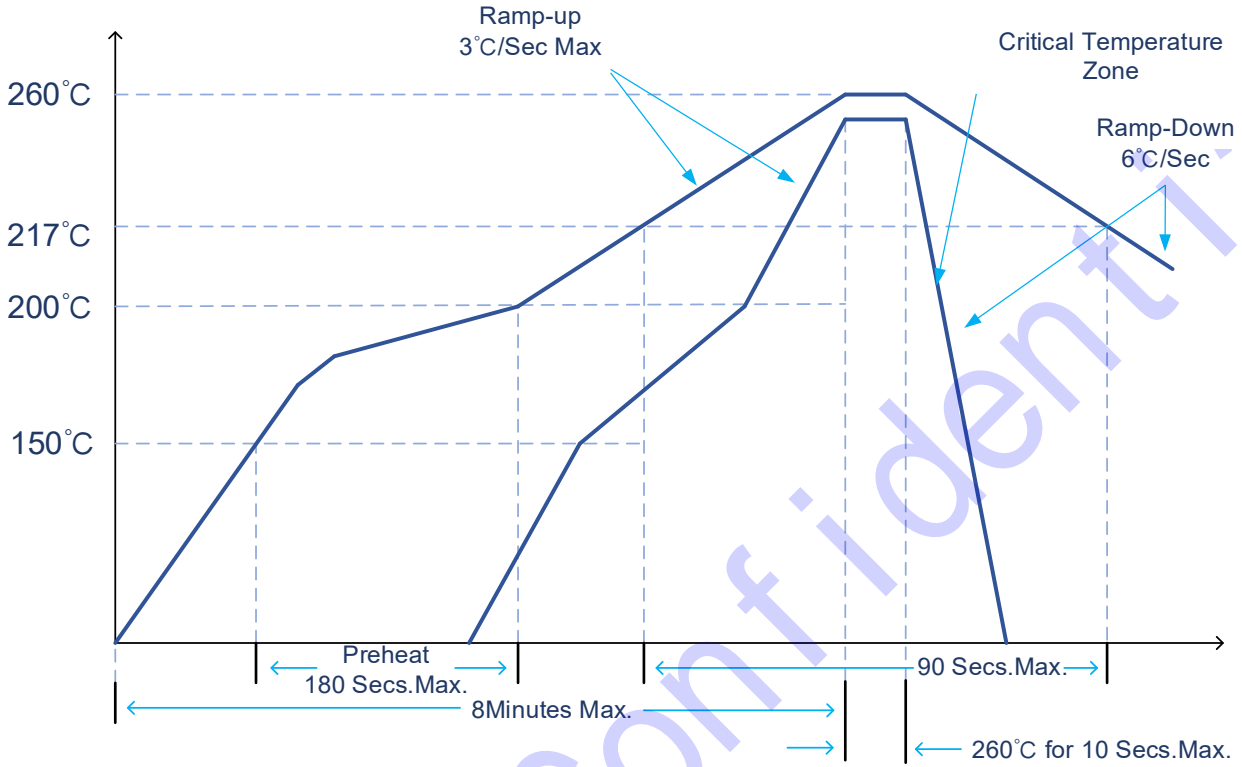
Declaration of No Harmful Substances

This part is compliant with 2005/20/EC packaging directive, 1907/2006/EC REACH directive and the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead free
- Halogen Free (Chlorine, Bromine)
- SVHC Free

Reflow Chart



NOTE: Reflow Profile with 240°C peak also acceptable.

LingChip