

## Product Features

- Multi-Band operation 400 to 2700MHz
- Excellent insertion loss: 0.75 dB@2.7GHz
- Input P0.1dB compression Point: 36dBm
- MIPI RFFE V2.1 serial control interface compatible
- Compact 2mm x 2mm in QFN-14 package, MSL1

## Product Applications

- 2G/3G/4G antenna diversity

## Product Description

The LX8586 is a low loss, high isolation SP8T switch with performance for antenna TRX application.

The LX8586 is compatible with MIPI RFFE interface, which is a key requirement for many cellular transceivers. This part is packaged in a compact 2mm x 2mm, 14-pin, QFN package which allows for a small solution size with no need for external DC blocking capacitors (when no external DC is applied to the device ports).

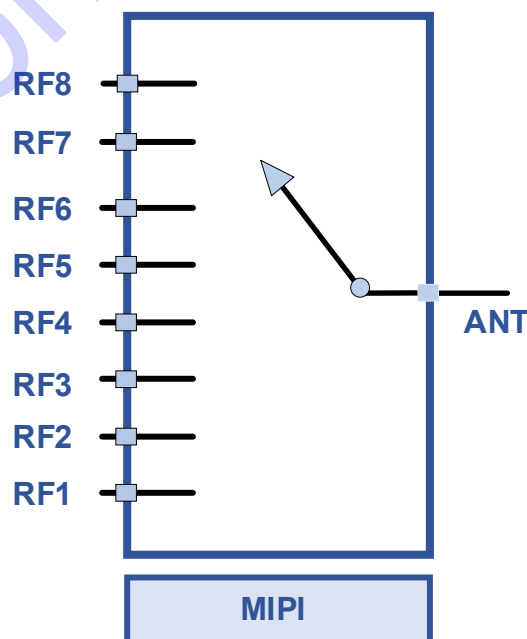


Figure 1 Functional Block Diagram

### Pin Configuration (Top View)

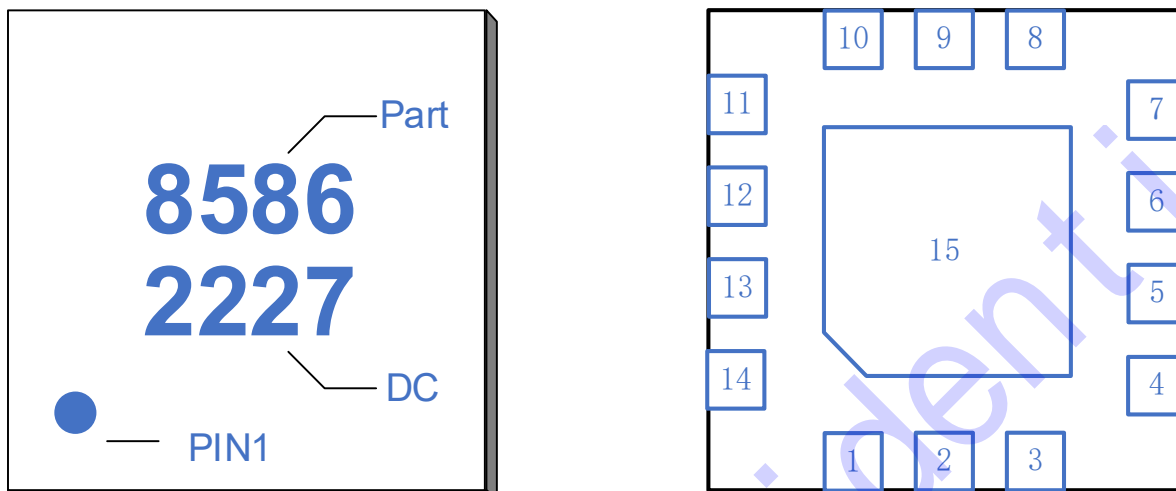


Figure 2 Pin Configuration (Top View)

### Pin Descriptions

Table 1:

NO.	Name	Description	NO.	Name	Units
1	VIO	RFFE Reference Voltage	9	ANT	Antenna Port
2	SDATA	RFFE Data Bus	10	RF1	RF Port1
3	SCLK	RFFE Clock Bus	11	RF2	RF Port2
4	GND	Ground	12	RF3	RF Port3
5	RF8	RF Port8	13	RF4	RF Port4
6	RF7	RF Port7	14	VDD	Power Supply Voltage
7	RF6	RF Port6	15	GND	Ground
8	RF5	RF Port5			

Function Characteristics

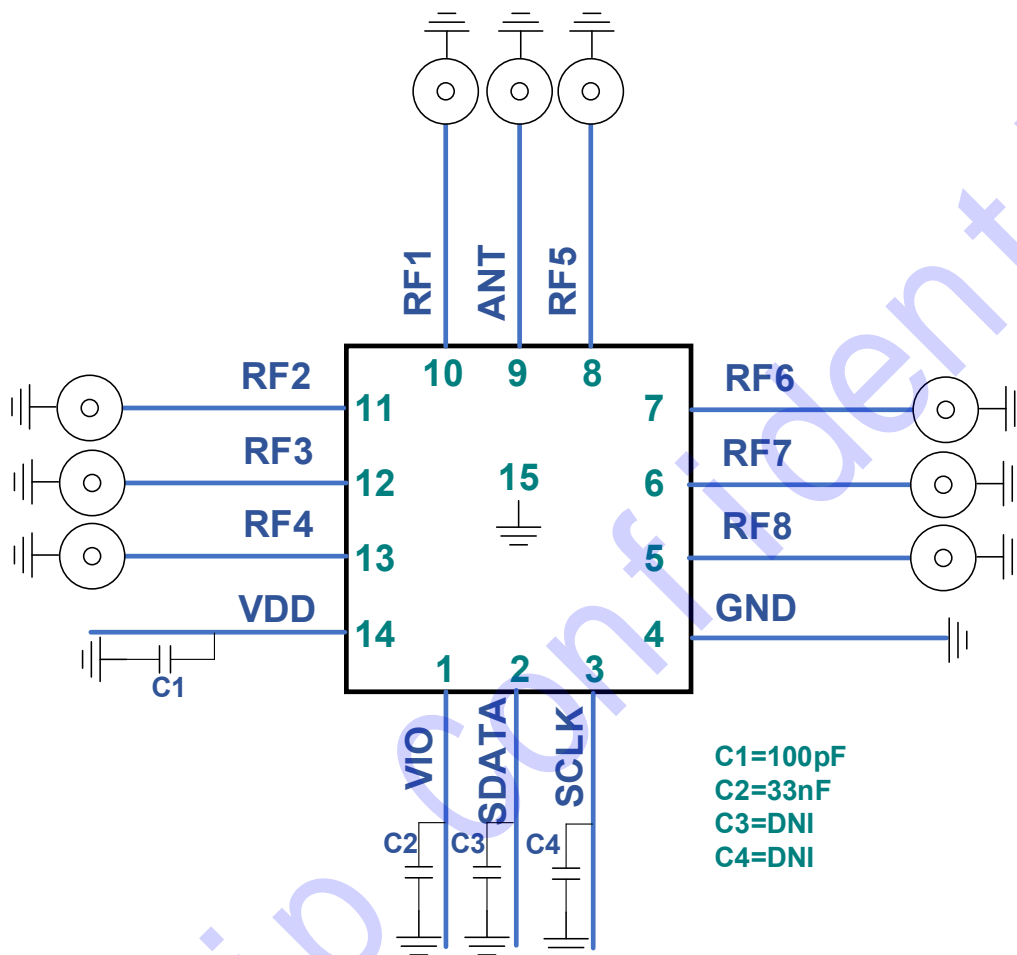


Figure 3 Evaluation Board Schematic

## Truth Table for RF Operating Mode

Table 2:

RF Path Operating Mode								
Register_0	RF1	RF2	RF3	RF4	RF5	RF6	RF7	RF8
0x01	Insertion Loss	Isolation	Isolation	Isolation	Isolation	Isolation	Isolation	Isolation
0x0B	Isolation	Insertion Loss	Isolation	Isolation	Isolation	Isolation	Isolation	Isolation
0x0E	Isolation	Isolation	Insertion Loss	Isolation	Isolation	Isolation	Isolation	Isolation
0x0A	Isolation	Isolation	Isolation	Insertion Loss	Isolation	Isolation	Isolation	Isolation
0x09	Isolation	Isolation	Isolation	Isolation	Insertion Loss	Isolation	Isolation	Isolation
0x06	Isolation	Isolation	Isolation	Isolation	Isolation	Insertion Loss	Isolation	Isolation
0x04	Isolation	Isolation	Isolation	Isolation	Isolation	Isolation	Insertion Loss	Isolation
0x0C	Isolation	Isolation	Isolation	Isolation	Isolation	Isolation	Isolation	Insertion Loss

## Absolute Maximum Conditions

Table 3:

Parameters	Symbol	Min	Max	Units	Condition
DC Power Supply	$V_{DD}$	2.4	4.8	V	$T_A=25^{\circ}\text{C}$
RFFE Reference Supply	$V_{IO}$	1.3	2	V	$T_A=25^{\circ}\text{C}$
RFFE Bus Voltage (SDATA, SCLK)	$V_I$	-0.3	2.5	V	$T_A=25^{\circ}\text{C}$
Max RF Input Power (ANT to RF1~8)	$P_{INMAX}$		37	dBm	$F_0=950\text{MHz}, 20\%\text{DC}, V_{DD}=2.8\text{V}, V_{IO}=1.8\text{V}, Z_0=50\Omega, T_A=25^{\circ}\text{C}$
Device Operating Temperature	$T_{OP}$	-40	+90	°C	
Device Storage Temperature	$T_{STG}$	-55	+150		
Electrostatic Discharge (All Pins)	$V_{ESD(HBM)}$	1000		V	Human Body Model
	$V_{ESD(CDM)}$	500			Charged Device Model

**Notices:** Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

## Recommended Operating Conditions

**Table 4:**

Parameters	Symbol	Min	Typ	Max	Units
Operating Frequency	$F_0$	0.4		2.7	GHz
DC Supply Voltage	$V_{DD}$	2.5	2.8	4.2	V
RFFE Reference Supply	$V_{IO}$	1.65	1.8	1.95	
RFFE Bus Voltage (SDATA, SCLK) High	$V_{IH}$	$0.8 \cdot V_{IO}$	$V_{IO}$	$V_{IO}$	
RFFE Bus Voltage (SDATA, SCLK) Low	$V_{IL}$	0	0	0.3	

## DC Performances

**Table 5:** ( $T_A=25^\circ\text{C}$ ,  $V_{DD}=2.8\text{V}$ ,  $V_{IO}=1.8\text{V}$ ,  $V_{IH}=0\text{V}$ ,  $P_{IN}=0\text{dBm}$ ,  $Z_0=50\Omega$ , unless otherwise noted.)

Parameters	Symbol	Test Condition	Min.	Typ.	Max.	Units
DC Supply Current	$I_{DD}$	Active State		50	90	uA
		Low Power State		6	10	
Current on VIO	$I_{IO}$			4	10	

## Timing Performances

**Table 6:** ( $T_A=25^\circ\text{C}$ ,  $V_{DD}=2.8\text{V}$ ,  $V_{IO}=1.8\text{V}$ ,  $V_{IH}=0\text{V}$ ,  $P_{IN}=0\text{dBm}$ ,  $Z_0=50\Omega$ , unless otherwise noted.)

Parameters	Symbol	Test Condition	Min.	Typ.	Max.	Units
Switching Time	$T_{SW}$	Implementing Switching CMD (50% SCLK) to 90%10% RF		1	2	us
Wake Up Time	$T_{WK}$	Exiting Lower power State CMD Implemented(50%SCLK) to 90%RF		10	20	
Turn On Time	$T_{ON}$	Cold Start, 50% of the latter power-up Supply to 90%RF		10	20	
Powered Reset Time	$T_{RST}$	VIO Off to it starts to re-power up	10			

## RF Performances

**Table 7:** ( $T_A=25^{\circ}\text{C}$ ,  $V_{DD}=2.8\text{V}$ ,  $V_{IO}=1.8\text{V}$ ,  $V_{IH}=0\text{V}$ ,  $P_{IN}=0\text{dBm}$ ,  $Z_0=50\Omega$ , unless otherwise noted.)

Parameters	Symbol	Test Condition	Min.	Typ.	Max.	Units
Insertion loss (ANT to RFX)	IL	$F_0=0.4$ to $1.0\text{GHz}$		0.40	0.45	dB
		$F_0=1.1$ to $2.0\text{GHz}$		0.64	0.70	
		$F_0=2.1$ to $2.7\text{GHz}$		0.88	0.95	
Isolation (ANT to RFX)	ISO	$F_0=0.4$ to $1.0\text{GHz}$	30	34		dB
		$F_0=1.1$ to $2.0\text{GHz}$	20	28		
		$F_0=2.1$ to $2.7\text{GHz}$	21	25		
Input 0.1dB Compression point (ANT to RFX)	$P_{0.1dB}$	$F_0=950\text{MHz}, 20\%DC$		37		dBm
2 <sup>nd</sup> Order Harmonic	$2F_0$	Pin = +26 dBm, 900MHz		-94		dBc
		Pin = +35 dBm, 900MHz		-82		
3 <sup>rd</sup> Order Harmonic	$3F_0$	Pin = +26 dBm, 900MHz		-92		dBc
		Pin = +35 dBm, 900MHz		-82		

## MIPI RFFE Commands

MIPI RFFE V2.1 interface supports the following Command Sequences:

- Register Write
- Register Read
- Register\_0 Write

Figure 4 and Figure 5 illustrate the timing diagrams for register write command sequence and read command sequence, respectively. Figure 6 describes the Register\_0 write command sequence. In the below timing figures, SA[3:0] is the slave address. A[4:0] is the register address. D[7:0] is the data. "P" is a parity bit.

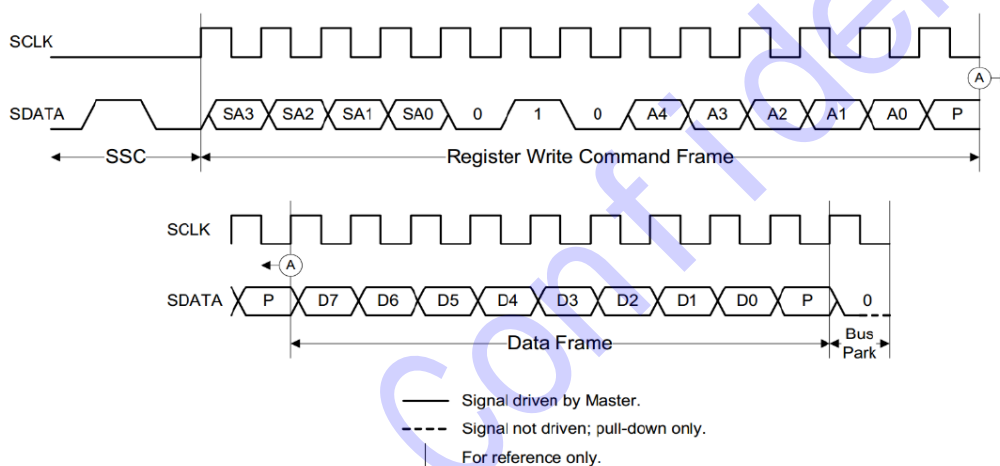


Figure 4 Register Write Command Sequence

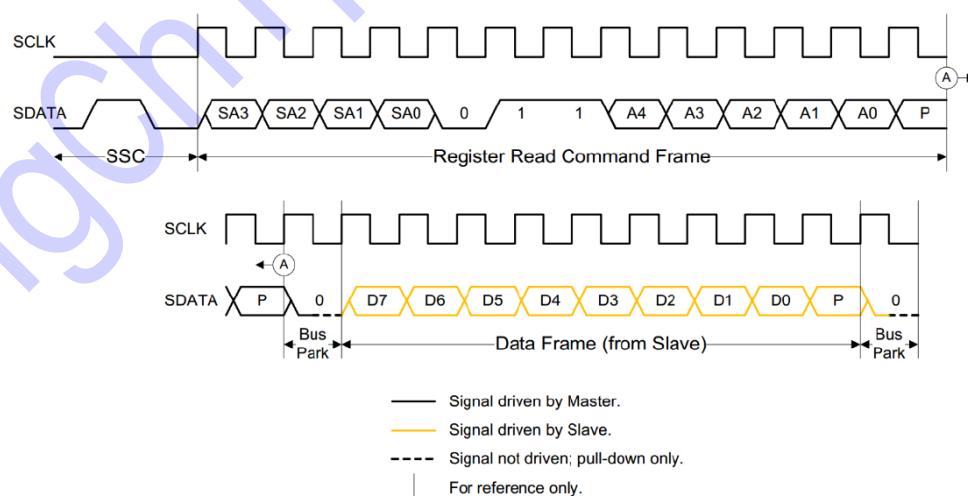


Figure 5 Register Read Command Sequence

Figure 6 shows the Register\_0 Write Command Sequence. The Command Sequence starts with an SSC, followed by the Register 0 Write Command Frame containing the Slave address, a logic '1' (to denote the command type and address), and an only seven-bit word to be written into Register 0. The Command Sequence ends with a Bus Park Cycle.

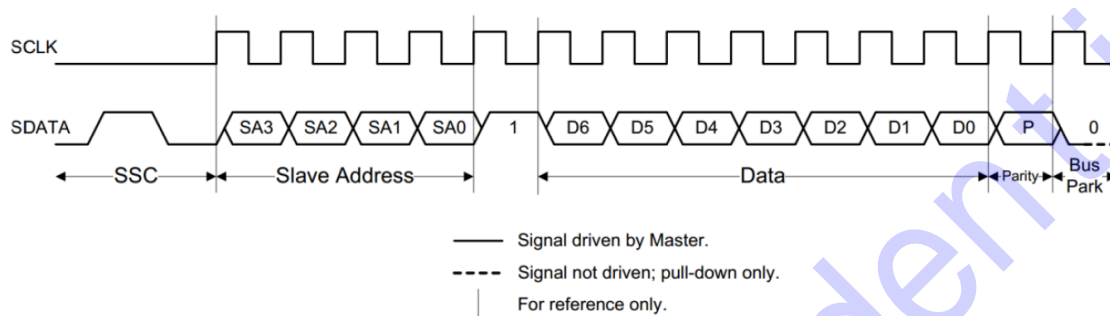


Figure 6 Register\_0 Write Command Sequence

Other information such as MIPI USID programming sequences, MIPI bus specifications, etc. can be referred to the MIPI Alliance Specification for RF Front-End Control Interface (RFFE), V2.1 (18-DEC-2017).



## Register Definition

Table 8:

Register 0, Address: 0x00 (MODE_CTRL)				
Register 0	Description	Default	Notes	Trig
[7:0]	MODE_CTRL	0x0	Switch control. See Truth Table	0
Register 1B, Address: 0x1B				
Register 1B	Description	Default	Notes	Trig
[7:4]	Reserved	0000	Reserved	No
[3:0]	GSID	0000	Group slave ID	No
Register 1C Address: 0x1C (PM_TRIG)				
Register 1C	Description	Default	Notes	Trig
[7:6]	PWR_MODE	10	00 = Normal Operation (ACTIVE) 01 = Default Settings (STARTUP) 10 = Low Power (LOW POWER) 11 = Reserved	No
[5]	Trigger Mask 2	0	Trigger Enable: 0 Trigger Disable: 1	No
[4]	Trigger Mask 1	0	Trigger Enable: 0 Trigger Disable: 1	No
[3]	Trigger Mask 0	0	Trigger Enable: 0 Trigger Disable: 1	No
[2]	Trigger Register 2	0	1 = Latch Register 2 contents	No
[1]	Trigger Register 1	0	1 = Latch Register 1 contents	No
[0]	Trigger Register 0	0	1 = Latch Register 0 contents	No
Register 1D, Address: 0x01D (PM_ID)				
Register 1D	Description	Default	Notes	Trig
[7:0]	Product ID	0X45	Product ID = 0X45	No
Register 1E, Address: 0x01E (MAN_ID)				
Register 1E	Description	Default	Notes	Trig
[7:0]	Manufacturer ID	0x78	Manufacturer ID[7:0] = 0x78	No
Register 1F Address: 0x01F (USID)				
Register 1F	Description	Default	Notes	Trig
[7:4]	Manufacturer ID	0x04	Manufacturer ID [11:8]	No
[3:0]	User ID	0xA	The default value at reset is selected via pin USID.	No

**Package Outline Dimension**

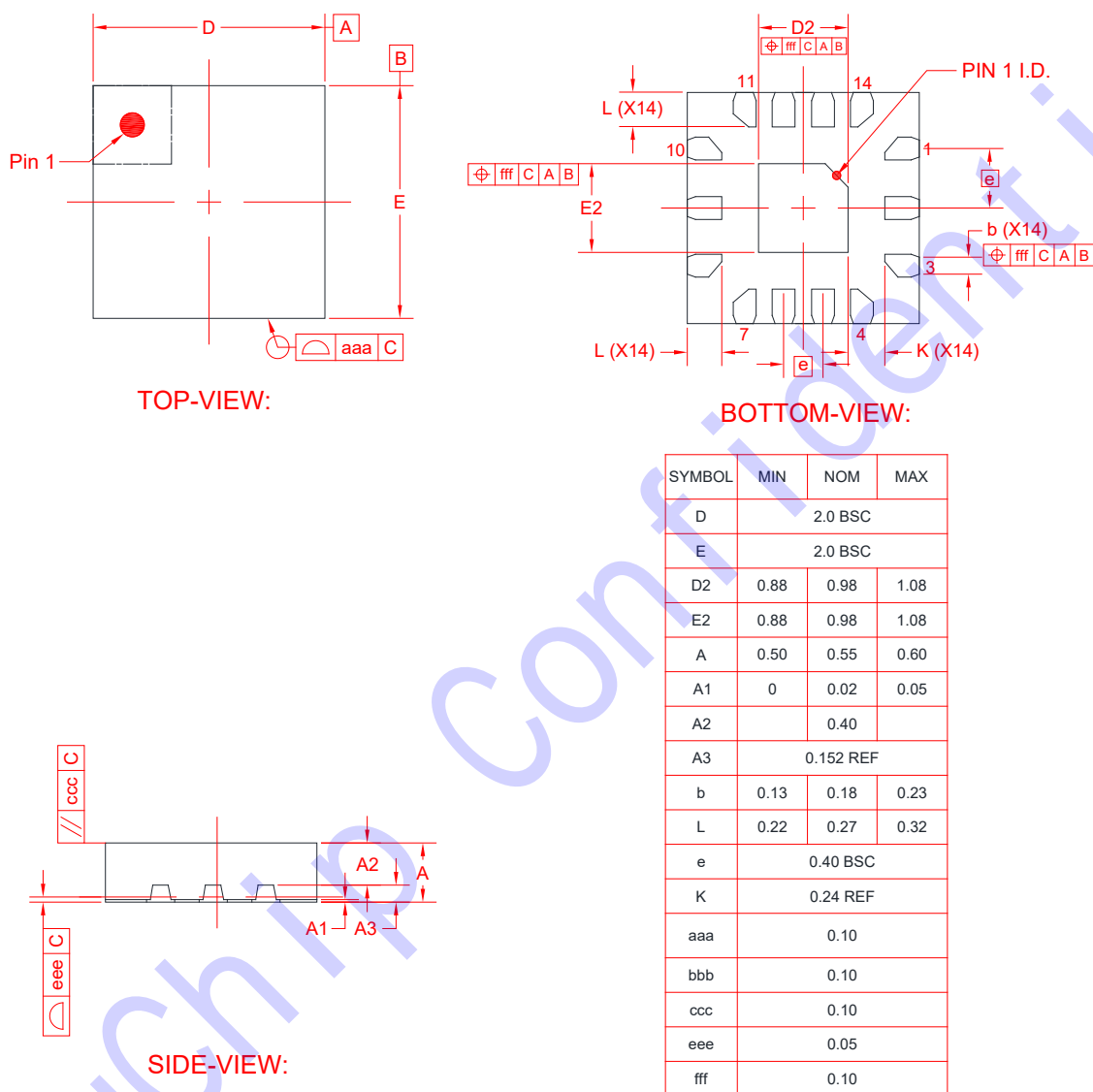
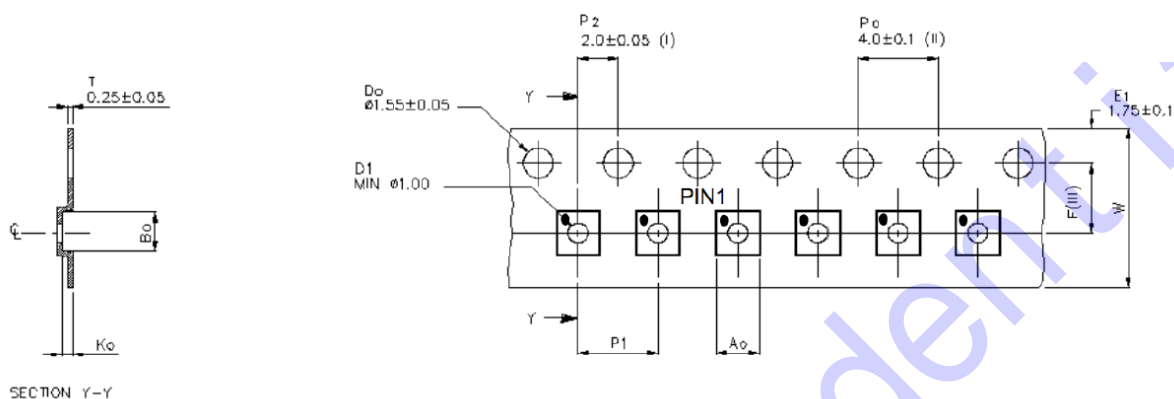


Figure 7 Package Outline Dimension

## Tape and Reel Dimensions (5000pcs)



A <sub>0</sub>	2.20 +/−0.05
B <sub>0</sub>	2.20 +/−0.05
K <sub>0</sub>	0.55 +/−0.05
F	3.50 +/−0.05
P1	4.00 +/−0.10
W	8.00 +0.3/−0.1

- (I) Measured from centreline of sprocket hole to centreline of pocket.  
 (II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .  
 (III) Measured from centreline of sprocket hole to centreline of pocket.  
 (IV) Other material available.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED

Figure 8 Tape and Reel Dimensions

## Declaration of No Harmful Substances

This part is compliant with 2005/20/EC packaging directive, 1907/2006/EC REACH directive and the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead free
- Halogen Free (Chlorine, Bromine)
- SVHC Free

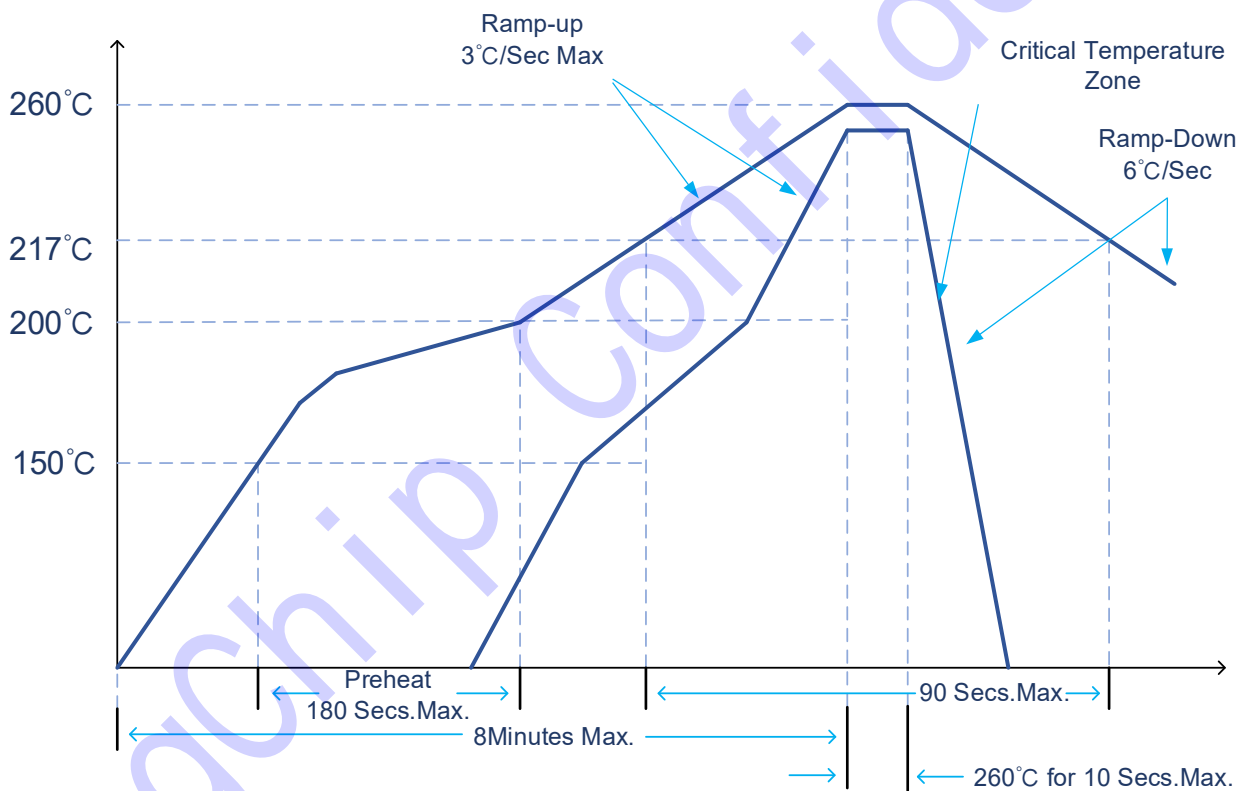
### ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electric charge. Proper ESD protection techniques should be applied when devices are operated.

### RoHS Compliant

This product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) , and are considered RoHS compliant.

### Reflow Chart



NOTE: Reflow Profile with 240°C peak also acceptable.