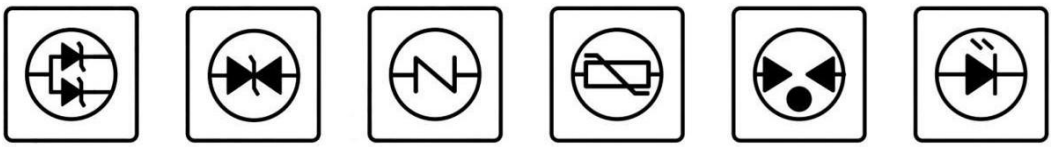
MSKSEMI 美森科
SEMICONDUCTOR



ESD9B5.0ST5G

Product specification

ESD9B5.0ST5G

Features

- 80W peak pulse power per line (t_P = 8/20μs)
- SOD-923 package
- Replacement for MLV(0402)
- Bidirectional configurations
- Response time is typically < 1ns
- Low clamping voltage
- RoHS compliant
- Transient protection for data lines to
  IEC61000-4-2(ESD) ±8 KV(air), ±15KV(contact);
  IEC61000-4-4 (EFT) 40A (5/50ns)

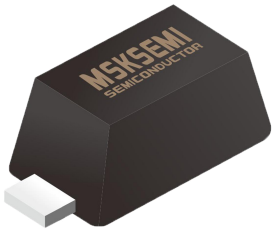
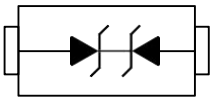
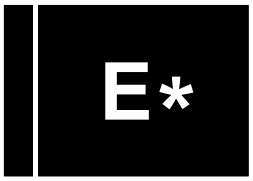
Mechanical Characteristics

- Lead finish:100% matte Sn(Tin)
- Mounting position: Any
- Qualified max reflow temperature:260℃
- Device meets MSL 1 requirements
- Pure tin plating: 7 ~ 17 um
- Pin flatness:≤3mil

Applications

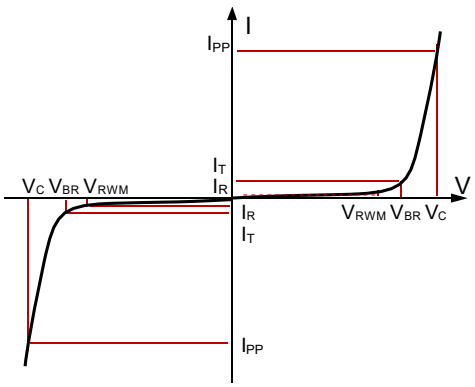
- Cellular phones
- Portable devices
- Digital cameras
- Power supplies

Reference News

SOD-923	PIN Configuration	Marking
		

Electronics Parameter

Symbol	Parameter
V_{RWM}	Peak Reverse Working Voltage
I_R	Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
P_{PP}	Peak Pulse Power
C_J	Junction Capacitance
I_F	Forward Current
V_F	Forward Voltage @ I_F



Electrical characteristics per line@25℃ (unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Peak Reverse Working Voltage	V_{RWM}				5	V
Breakdown Voltage	V_{BR}	I_t = 1mA	5.6	6.7	7.8	V
Reverse Leakage Current	I_R	V_{RWM} = 5V T=25℃			1.0	μA
Maximum Reverse Peak Pulse Current	I_{PP}			5		A
Clamping Voltage	V_C	I_{PP}=1A			8	V
Clamping Voltage	V_C	I_{PP}=3A			13	V
Clamping Voltage	V_C	I_{PP}=5A			15	V
Junction Capacitance	C_j	V_R=0V f = 1MHz		12	15	pF

Absolute maximum rating@25℃

Rating	Symbol	Value	Units
Peak Pulse Power (t_p=8/20μs)	P_{pp}	80	W
Operating Temperature	T_J	-55 to +150	℃
Storage Temperature	T_{STG}	-55 to +150	℃

Typical Characteristics

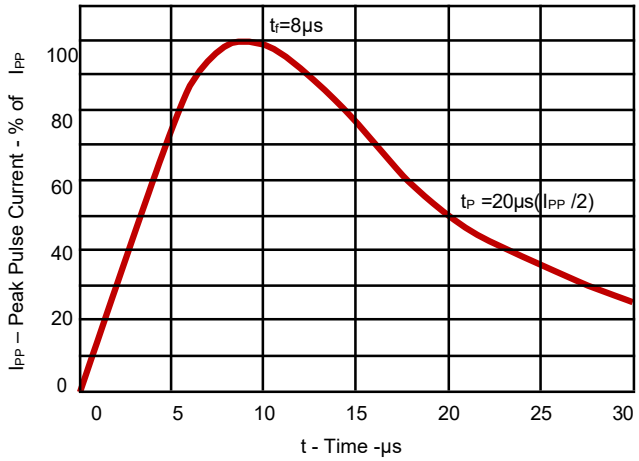


Fig 1.Pulse Waveform

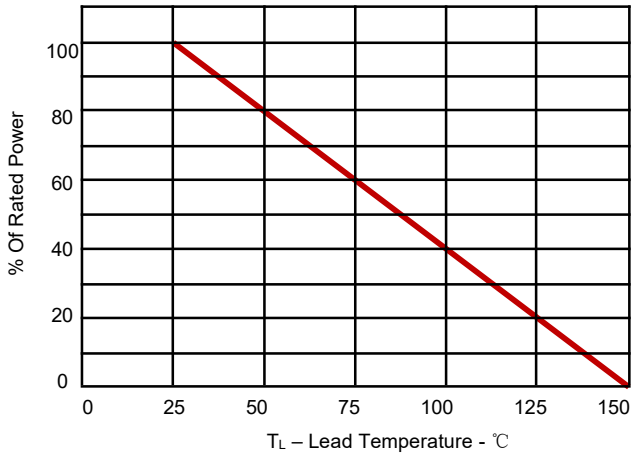


Fig 2.Power Derating Curve

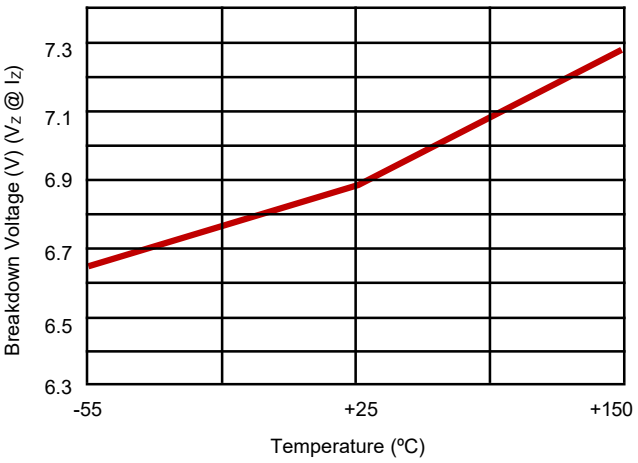


Fig 3.Typical Breakdown Voltage vs. Temperature

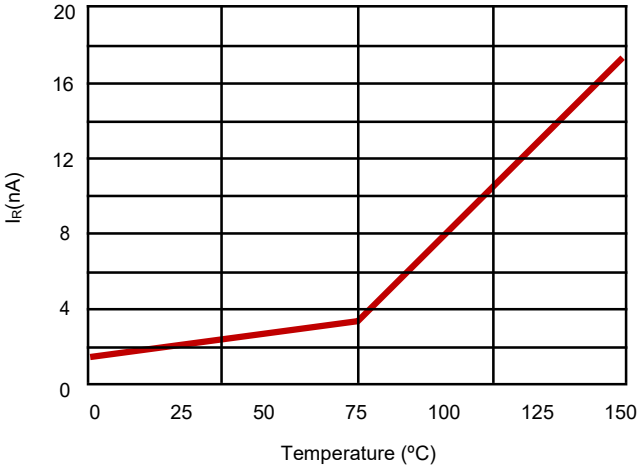


Fig 4.Typical Leakage Current vs. Temperature

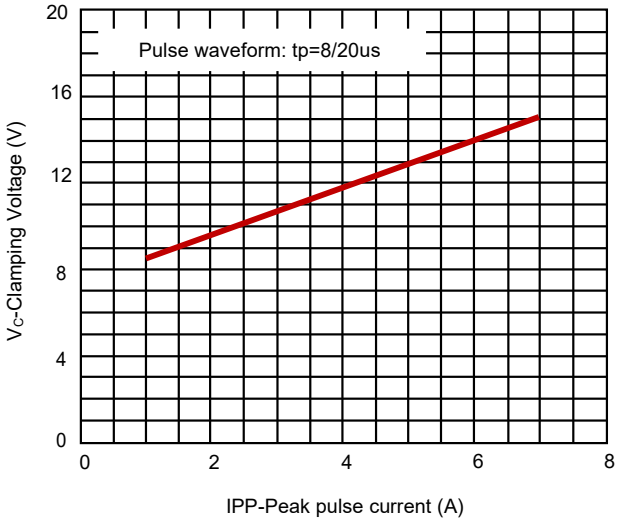


Fig 5. Clamping voltage vs. Peak pulse current

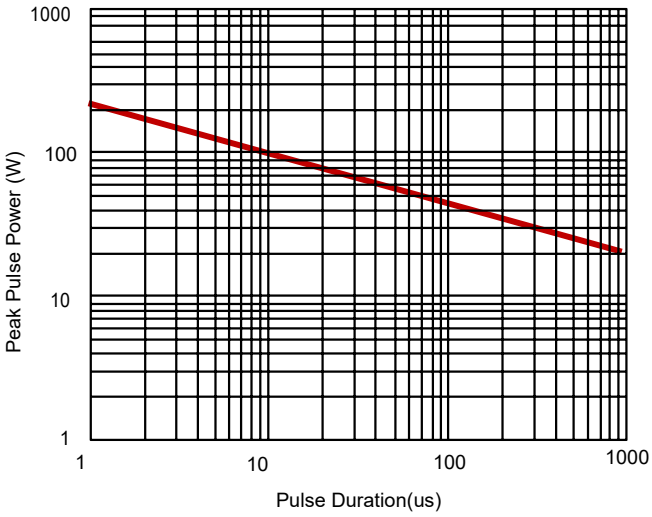


Fig 6. Non-Repetitive Peak Pulse Power vs. Pulse time

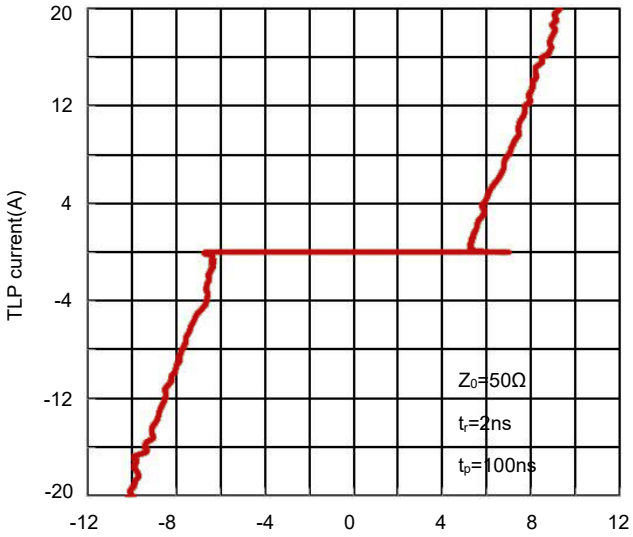
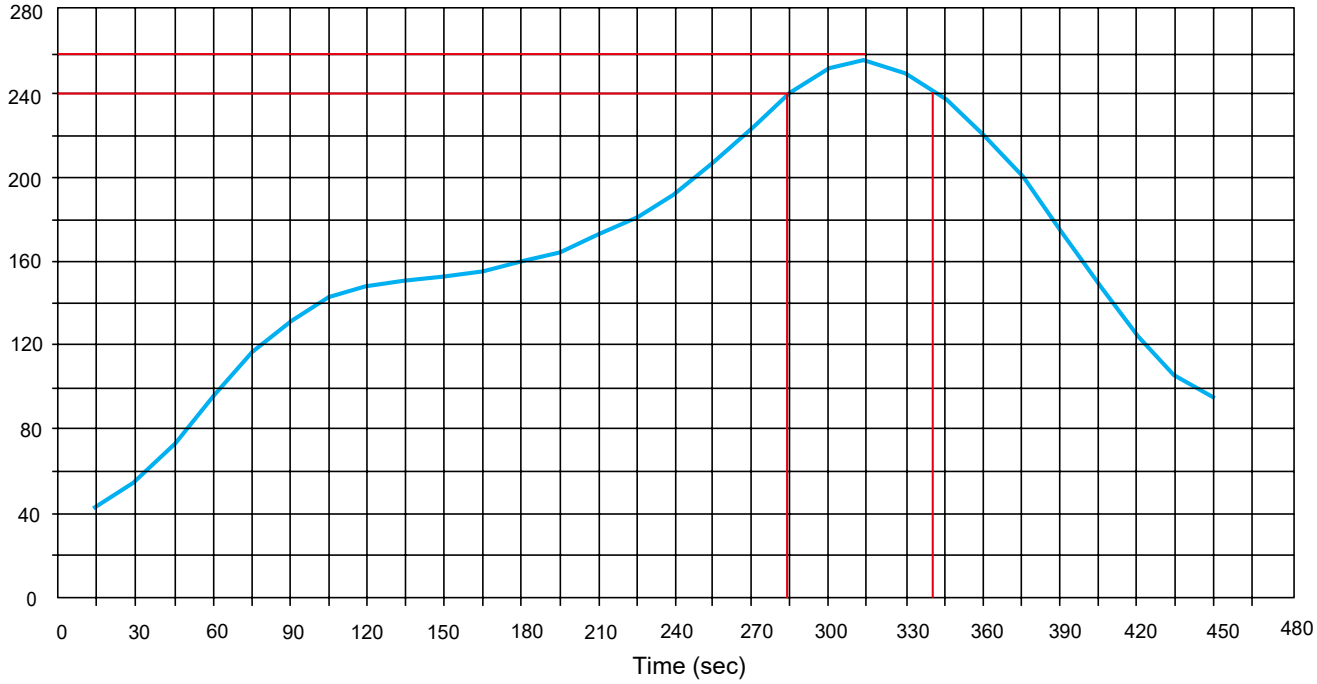


Fig 7 TLP Measuremen

Solder Reflow Recommendation

Peak Temp=257℃, Ramp Rate=0.802deg. ℃/sec

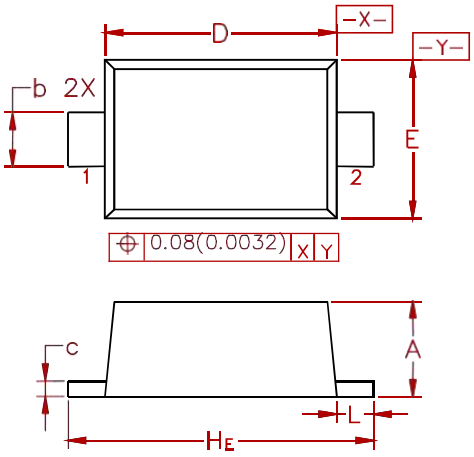


PCB Design

For TVS diodes a low-ohmic and low-inductive path to chassis earth is absolutely mandatory in order to achieve good ESD protection. Novices in the area of ESD protection should take following suggestions to heart:

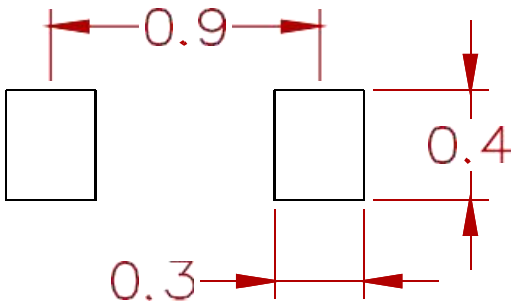
- Do not use stubs, but place the cathode of the TVS diode directly on the signal trace.
- Do not make false economies and save copper for the ground connection.
- Place via holes to ground as close as possible to the anode of the TVS diode.
- Use as many via holes as possible for the ground connection.
- Keep the length of via holes in mind! The longer the more inductance they will have.

PACKAGEMECHANICALDATA



Dim	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	0.36	0.40	0.43	0.014	0.016	0.017
b	0.15	0.20	0.25	0.006	0.008	0.010
c	0.07	0.12	0.17	0.003	0.005	0.007
D	0.75	0.80	0.85	0.030	0.031	0.033
E	0.55	0.60	0.65	0.022	0.024	0.026
HE	0.95	1.00	1.05	0.037	0.039	0.041
L	0.05	0.10	0.15	0.002	0.004	0.006

Suggested Pad Layout



Dimensions: Millimeters

Order information

Orderable Device	Package	Packing Option
ESD9B5.0ST5G	SOD-923	8000PCS

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