4-Bit Bidirectional Voltage-Level Translator with Automatic Direction Sensing

1 FEATURES

- **RS0204A-Q1 AEC-Q100 Qualification is Ongoing**
- **No Direction-Control**
- **Data Rates 100Mbps**
- **1.2V to 3.6V on A ports and 1.65V to 5.5V on B Ports ($V_{CCA} \leq V_{CCB}$)**
- **V_{CC} Isolation Feature: If Either V_{CC} Input is at GND, Both Ports are in the High-Impedance State**
- **Output Enable (OE) Input Circuit Referenced to V_{CCA}**
- **Low Power Consumption, 10µA Maximum I_{CC}**
- **No Power-Supply Sequencing Required: Either V_{CCA} or V_{CCB} can be Ramped First**
- **I_{OFF}: Supports Partial-Power-Down Mode Operation**
- **Extended Temperature: -40°C to 125°C**

2 APPLICATIONS

- **Automotive Infotainment**
- **Advance Driver Assistance Systems (ADAS)**

3 DESCRIPTIONS

This 4-bit non-inverting translator is a bidirectional voltage-level translator and can be used to establish digital switching compatibility between mixed-voltage systems. It uses two separate configurable power-supply rails, with the A ports supporting operating voltages from 1.2V to 3.6V while it tracks the V_{CCA} supply, and the B ports supporting operating voltages from 1.65V to 5.5V while it tracks the V_{CCB} supply. This allows the support of both lower and higher logic signal levels while providing bidirectional translation capabilities between any of the 1.2V, 1.5V, 1.8V, 2.5V, 3.3V and 5V voltage nodes.

V_{CCA} must not exceed V_{CCB}.

When the output-enable (OE) input is low, all outputs are placed in the high-impedance state, which significantly reduces the power-supply quiescent current consumption. OE has an internal pull-down current source, as long as V_{CCA} is powered.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pull-down resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The RS0204A-Q1 is available in Green UQFN1.7X2-12 and TSSOP14 packages. It operates over an ambient temperature range of -40°C to 125°C.

Device Information [1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS0204A-Q1	TSSOP14	5.00mm×4.40mm
	UQFN1.7X2-12	2.00mm×1.70mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
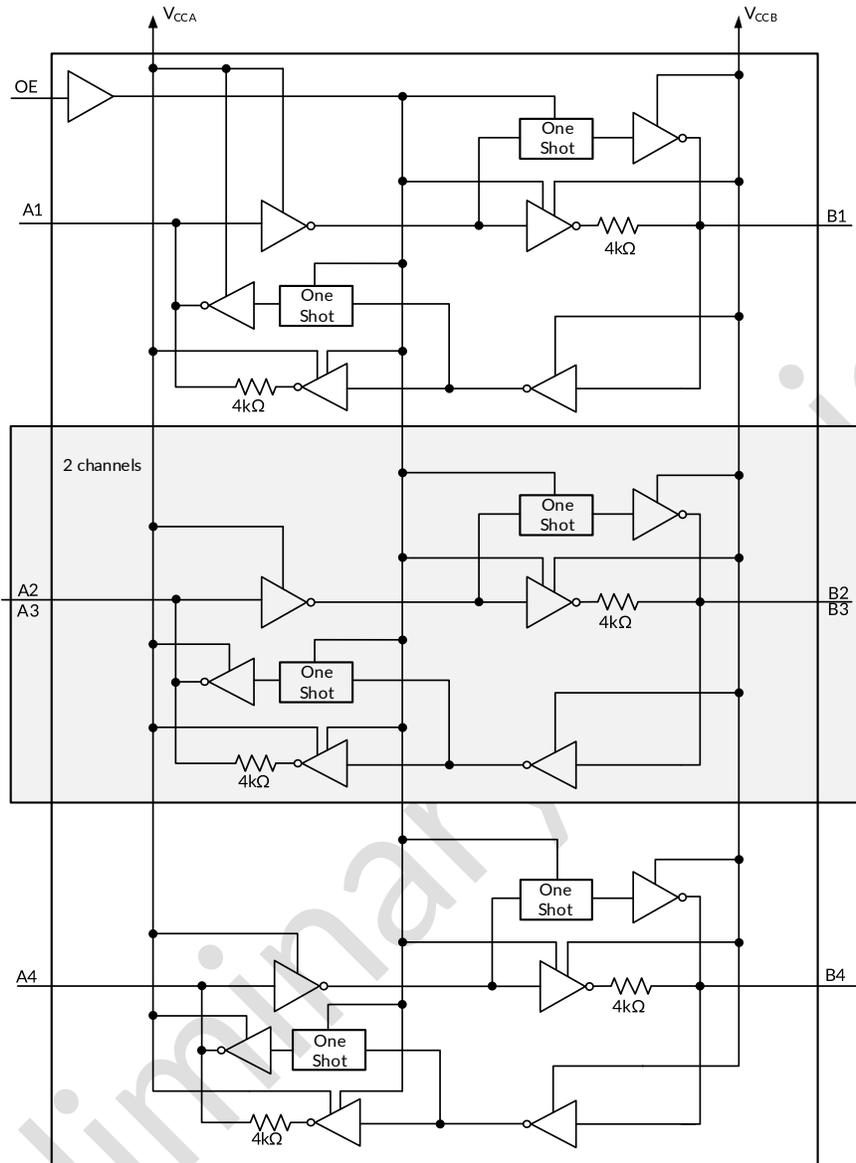
4 FUNCTIONAL BLOCK DIAGRAM

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5 REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version.

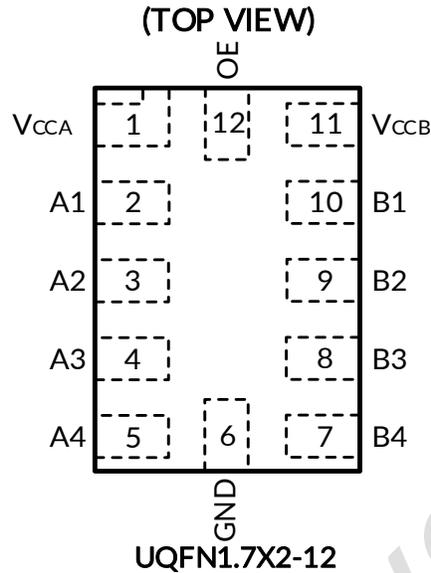| VERSION	Change Date	Change Item
A.0	2024/07/30	Preliminary version completed
A.0.1	2025/01/07	Update PACKAGE/ORDERING INFORMATION

6 PACKAGE/ORDERING INFORMATION [1]

PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	Lead finish/Ball material [2]	MSL Peak Temp [3]	PACKAGE MARKING [4]	PACKAGE OPTION
RS0204A -Q1	RS0204AXUTQH12 -Q1	-40°C ~+125°C	UQFN1.7X2-12	NIPDAU	MSL1-260°-Unlimited	0204A	Tape and Reel,4000
	RS0204AXQ-Q1	-40°C ~+125°C	TSSOP14	SN	MSL1-260°-Unlimited	RS0204A	Tape and Reel,4000

NOTE:

(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) Lead finish/Ball material. Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(3) RUNIC classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F, Please align with RUNIC if your end application is quite critical to the preconditioning setting or if you have special requirement.

(4) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

7 PIN CONFIGURATIONS

(TOP VIEW)

UQFN1.7X2-12

PIN DESCRIPTION

PIN UQFN1.7X2-12	NAME	TYPE [1]	FUNCTION
1	V_{CCA}	P	A Port Supply Voltage. $1.2V \leq V_{CCA} \leq 3.6V$ and $V_{CCA} \leq V_{CCB}$.
2	A1	I/O	Input/output A1. Reference to V_{CCA}.
3	A2	I/O	Input/output A2. Reference to V_{CCA}.
4	A3	I/O	Input/output A3. Reference to V_{CCA}.
5	A4	I/O	Input/output A4. Reference to V_{CCA}.
6	GND	–	Ground.
7	B4	I/O	Input/output B4. Reference to V_{CCB}.
8	B3	I/O	Input/output B3. Reference to V_{CCB}.
9	B2	I/O	Input/output B2. Reference to V_{CCB}.
10	B1	I/O	Input/output B1. Reference to V_{CCB}.
11	V_{CCB}	P	B Ports Supply Voltage. $1.65V \leq V_{CCB} \leq 5.5V$.
12	OE	I	Output Enable (Active High). Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA}.

(1) I=input, O=output, I/O=input and output, P=power

PIN CONFIGURATIONS

(TOP VIEW)

```
           ┌─────────────────┐
           │ O               │
  V_CCA  1 │                 │ 14  V_CCB
   A1    2 │                 │ 13  B1
   A2    3 │                 │ 12  B2
   A3    4 │                 │ 11  B3
   A4    5 │                 │ 10  B4
   NC    6 │                 │  9  NC
  GND    7 │                 │  8  OE
           └─────────────────┘
               TSSOP14
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PIN DESCRIPTION

PIN TSSOP14	NAME	TYPE [1]	FUNCTION
1	V_{CCA}	P	A Port Supply Voltage.$1.2V \leq V_{CCA} \leq 3.6V$ and $V_{CCA} \leq V_{CCB}$
2	A1	I/O	Input/output A1. Reference to V_{CCA}.
3	A2	I/O	Input/output A2. Reference to V_{CCA}.
4	A3	I/O	Input/output A3. Reference to V_{CCA}.
5	A4	I/O	Input/output A4. Reference to V_{CCA}.
6	NC	-	No internal connection.
7	GND	–	Ground.
8	OE	I	Output Enable (Active High). Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA}.
9	NC	-	No internal connection.
10	B4	I/O	Input/output B4. Reference to V_{CCB}.
11	B3	I/O	Input/output B3. Reference to V_{CCB}.
12	B2	I/O	Input/output B2. Reference to V_{CCB}.
13	B1	I/O	Input/output B1. Reference to V_{CCB}.
14	V_{CCB}	P	B Ports Supply Voltage.$1.65V \leq V_{CCB} \leq 5.5V$.

(1) I=input, O=output, I/O=input and output, P=power

8 SPECIFICATIONS

8.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) [1]

SYMBOL	PARAMETER		MIN	MAX	UNIT
V_{CCA}	Supply Voltage Range		-0.3	4.6	V
V_{CCB}	Supply Voltage Range		-0.3	6.5	V
V_I [2]	Input Voltage Range	A port	-0.3	4.6	V
		B port	-0.3	6.5	
		OE	-0.3	4.6	
V_O [2]	Voltage range applied to any output in the high-impedance or power-off state	A port	-0.3	4.6	V
		B port	-0.3	6.5	
V_O [2][3]	Voltage range applied to any output in the high or low state	A port	-0.3	V_{CCA}+0.3	V
		B port	-0.3	V_{CCB}+0.3	
I_{IK}	Input clamp current	V_I<0		-50	mA
I_{OK}	Output clamp current	V_o<0		-50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB} or GND			±100	mA
θ_{JA}	Package thermal impedance [4]	TSSOP14		121	°C/W
		UQFN1.7X2-12		120	
T_J	Junction Temperature [5]		-40	150	°C
T_{stg}	Storage temperature		-65	150	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.
(4) The package thermal impedance is calculated in accordance with JESD-51.
(5) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

8.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (HBM), per AEC Q100-002 [1]	TBD	V
		Charged-Device Model (CDM), per AEC Q100-011	TBD	
		Latch-Up (LU), per AEC Q100-004	TBD	mA

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.3 Recommended Operating Conditions

V_{CCI} is the supply voltage associated with the input port. V_{CCO} is the supply voltage associated with the output port. [1][2]

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
Supply voltage	V_{CCA}		1.2		3.6	V
	V_{CCB}		1.65		5.5	
High-level input voltage (V_{IH})	A-port inputs	V_{CCA} = 1.2 V to 3.6 V V_{CCB} = 1.65 V to 5.5 V	V_{CCI} x 0.65 [3]		V_{CCI}	V
	B-port inputs	V_{CCA} = 1.2 V to 3.6 V V_{CCB} = 1.65 V to 5.5 V	V_{CCI} x 0.65		V_{CCI}	
	OE input	V_{CCA} = 1.2 V to 3.6 V V_{CCB} = 1.65 V to 5.5 V	V_{CCA} x 0.65		5.5	
Low-level input voltage (V_{IL})	A-port inputs	V_{CCA} = 1.2 V to 3.6 V V_{CCB} = 1.65 V to 5.5 V	0		V_{CCI} x 0.35 [3]	V
	B-port inputs	V_{CCA} = 1.2 V to 3.6 V V_{CCB} = 1.65 V to 5.5 V	0		V_{CCI} x 0.35	
	OE input	V_{CCA} = 1.2 V to 3.6 V V_{CCB} = 1.65 V to 5.5 V	0		V_{CCA} x 0.35	
Voltage applied to any output in the high-impedance or power-off state (Vo)	A-port	V_{CCA} = 1.2 V to 3.6 V V_{CCB} = 1.65 V to 5.5 V	0		3.6	V
	B-port	V_{CCA} = 1.2 V to 3.6 V V_{CCB} = 1.65 V to 5.5 V	0		5.5	
Input transition rise or fall rate($\Delta t/\Delta v$)	A-port inputs	V_{CCA} = 1.2 V to 3.6 V V_{CCB} = 1.65 V to 5.5 V			40	ns/V
	B-port inputs	V_{CCA} = 1.2 V to 3.6 V	V_{CCB} = 1.65 V to 3.6 V			40	
			V_{CCB} = 4.5 V to 5.5 V			30	
T_A Operating free-air temperature			-40		125	°C

(1) The A and B sides of an unused data I/O pair must be held in the same state, that is, both at V_{CCI} or both at GND.
(2) V_{CCA} must be less than or equal to V_{CCB} and must not exceed 3.6 V.
(3) V_{CCI} is the supply voltage associated with the input port.

8.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted) [1] [2] [3]

PARAMETER		CONDITIONS	V_{CCA}	V_{CCB}	TEMP	MIN[4]	TYP[5]	MAX[4]	UNIT
V_{OHA}	Port A output high voltage	I_{OH} = −20 µA	1.2V		+25°C		1.1		V
			1.4V to 3.6V		Full	V_{CCA}-0.4			
V_{OLA}	Port A output low voltage	I_{OL} = 20 µA	1.2V		+25°C		0.3		
			1.4V to 3.6V		Full			0.4	
V_{OHB}	Port B output high voltage	I_{OH} = −20 µA		1.65V to 5.5V	Full	V_{CCB} - 0.4			
V_{OLB}	Port B output low voltage	I_{OL} = 20 µA		1.65V to 5.5V	Full			0.4	
I_I	Input leakage current	OE $V_I = V_{CCI}$ or GND	1.2V to 3.6V	1.65V to 5.5V	+25°C			±1	µA
					Full			±2	
I_{off}	Partial power down current	A Ports V_I or Vo=0 to 3.6V	0V	0V to 5.5V	+25°C			±1	µA
					Full			±2	
		B Ports V_I or Vo=0 to 5.5V	0V to 3.6V	0V	+25°C			±1	µA
					Full			±2	
I_{OZ} [6]	High-impedance State output current	A or B port OE=GND	1.2V to 3.6V	1.65V to 5.5V	+25°C			±1	µA
					Full			±2	
I_{CCA}	V_{CCA} supply current	$V_I = V_{CCI}$ or GND I_O = 0	1.2V	1.65V to 5.5V	+25°C		0.06		µA
			1.4V to 3.6V	1.65V to 5.5V	Full			5	
			3.6V	0V	Full			2	
			0V	5.5V	Full			-2	
I_{CCB}	V_{CCB} supply current	$V_I = V_{CCI}$ or GND I_O = 0	1.2V	1.65V to 5.5V	+25°C		3.4		µA
			1.4V to 3.6V	1.65V to 5.5V	Full			5	
			3.6V	0V	Full			-2	
			0V	5.5V	Full			2	
I_{CCA} + I_{CCB}	Combined supply current	$V_I = V_{CCI}$ or GND I_O = 0	1.2V	1.65V to 5.5V	+25°C		3.5		µA
			1.4V to 3.6V	1.65V to 5.5V	Full			10	
I_{CCZA}	V_{CCA} supply current	$V_I = V_{CCI}$ or GND I_O = 0, OE=GND	1.2V	1.65V to 5.5V	+25°C		0.05		µA
			1.4V to 3.6V	1.65V to 5.5V	Full			5	
I_{CCZB}	V_{CCB} supply current	$V_I = V_{CCI}$ or GND I_O = 0, OE=GND	1.2V	1.65V to 5.5V	+25°C		3.3		µA
			1.4V to 3.6V	1.65V to 5.5V	Full			5	
C_i	Input capacitance	OE	1.2V to 3.6V	1.65V to 5.5V	+25°C		4		pF
C_{io}	Input-to-output internal capacitance	A port	1.2V to 3.6V	1.65V to 5.5V	+25°C		5		pF
		B port	1.2V to 3.6V	1.65V to 5.5V	+25°C		9		

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port
(3) V_{CCA} must be less than or equal to V_{CCB}.
(4) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
(5) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.
(6) For I/O ports, the parameter I_{OZ} includes the input leakage current.

8.5 Timing Requirements:

8.5.1 V$_{CCA}$=1.2V

T$_A$=25°C, V$_{CCA}$=1.2V

		V$_{CCB}$=1.8V	V$_{CCB}$=2.5V	V$_{CCB}$=3.3V	V$_{CCB}$=5V	UNIT
		TYP	TYP	TYP	TYP	
Data rate		20	20	20	20	Mbps
Pulse duration(t$_w$)	data inputs	50	50	50	50	ns

8.5.2 V$_{CCA}$=1.5V±0.1 V

T$_A$=25°C, V$_{CCA}$=1.5V±0.1V (unless otherwise noted)

		V$_{CCB}$=1.8V ±0.15V	V$_{CCB}$=2.5V ±0.2V	V$_{CCB}$=3.3V ±0.3V	V$_{CCB}$=5V ±0.5V	UNIT
		TYP	TYP	TYP	TYP	
Data rate		40	40	40	40	Mbps
Pulse duration(t$_w$)	data inputs	25	25	25	25	ns

8.5.3 V$_{CCA}$=1.8V±0.15 V

T$_A$=25°C, V$_{CCA}$=1.8V±0.15V (unless otherwise noted)

		V$_{CCB}$=1.8V ±0.15V	V$_{CCB}$=2.5V ±0.2V	V$_{CCB}$=3.3V ±0.3V	V$_{CCB}$=5V ±0.5V	UNIT
		TYP	TYP	TYP	TYP	
Data rate		50	50	50	50	Mbps
Pulse duration(t$_w$)	data inputs	25	25	25	25	ns

8.5.4 V$_{CCA}$=2.5V±0.2 V

T$_A$=25°C, V$_{CCA}$=2.5V±0.2V (unless otherwise noted)

		V$_{CCB}$=2.5V ±0.2V	V$_{CCB}$=3.3V ±0.3V	V$_{CCB}$=5V ±0.5V	UNIT
		TYP	TYP	TYP	
Data rate		70	80	80	Mbps
Pulse duration(t$_w$)	data inputs	14	12	12	ns

8.5.5 V$_{CCA}$=3.3V±0.3 V

T$_A$=25°C, V$_{CCA}$=3.3V±0.3V (unless otherwise noted)

		V$_{CCB}$=3.3V ±0.3V	V$_{CCB}$=5V ±0.5V	UNIT
		TYP	TYP	
Data rate		80	100	Mbps
Pulse duration(t$_w$)	data inputs	12	10	ns

8.6 Switching Characteristics: V_{CCA}=1.2V

T_A=25℃, V_{CCA}=1.2V

PARAMETER		CONDITIONS	V_{CCB}=1.8V	V_{CCB}=2.5V	V_{CCB}=3.3V	V_{CCB}=5V	UNIT
			TYP	TYP	TYP	TYP	
t_{PHL}	Propagation delay time high-to-low output	A-to-B	30.3	26.1	24.3	21.3	ns
t_{PLH}	Propagation delay time low-to-high output	A-to-B	31.8	25	23.3	22.7	ns
t_{PHL}	Propagation delay time high-to-low output	B-to-A	39	34.8	20.9	20.1	ns
t_{PLH}	Propagation delay time low-to-high output	B-to-A	30.3	26.1	24.6	22.2	ns
t_{en}	Enable time	OE-to-A or B	368	313	290	288	ns
t_{dis}	Disable time	OE-to-A or B	716	687	659	578	ns
t_{rA}, t_{fA}	Input rise time	A port rise and fall time	12.4	12.3	12.7	12.4	ns
t_{rB}, t_{fB}	Input rise time	B port rise and fall time	3.2	1.5	1	0.9	ns
Maximum data rate			20	20	20	20	Mbps

8.7 Switching Characteristics: V_{CCA}=1.5V ± 0.1V

over recommended operating free-air temperature range, V_{CCA}=1.5V±0.1V (unless otherwise noted)

PARAMETER		CONDITIONS	V_{CCB}=1.8V ±0.15V	V_{CCB}=2.5V ±0.2V	V_{CCB}=3.3V ±0.3V	V_{CCB}=5V ±0.5V	UNIT
			TYP	TYP	TYP	TYP	
t_{PHL}	Propagation delay time high-to-low output	A-to-B	19.75	13.2	12	11.5	ns
t_{PLH}	Propagation delay time low-to-high output	A-to-B	22.5	15.3	14	12.8	ns
t_{PHL}	Propagation delay time high-to-low output	B-to-A	21.9	18.3	17.7	17.1	ns
t_{PLH}	Propagation delay time low-to-high output	B-to-A	21	16.8	15.8	15.1	ns
t_{en}	Enable time	OE-to-A or B	325	311	285	268	ns
t_{dis}	Disable time	OE-to-A or B	688	679	652	572	ns
t_{rA}, t_{fA}	Input rise time	A port rise and fall time	4.2	4.2	4.2	4.1	ns
t_{rB}, t_{fB}	Input rise time	B port rise and fall time	3.1	1.5	1	0.9	ns
Maximum data rate			40	40	40	40	Mbps

8.8 Switching Characteristics: V_{CCA}=1.8V ± 0.15V

over recommended operating free-air temperature range, V_{CCA}=1.8V±0.15V (unless otherwise noted)

PARAMETER		CONDITIONS	V_{CCB}=1.8V ±0.15V	V_{CCB}=2.5V ±0.2V	V_{CCB}=3.3V ±0.3V	V_{CCB}=5V ±0.5V	UNIT
			TYP	TYP	TYP	TYP	
t_{PHL}	Propagation delay time high-to-low output	A-to-B	17	11.3	10	9.3	ns
t_{PLH}	Propagation delay time low-to-high output	A-to-B	18.5	12	10.5	9.5	ns
t_{PHL}	Propagation delay time high-to-low output	B-to-A	16.5	11.7	10.5	10	ns
t_{PLH}	Propagation delay time low-to-high output	B-to-A	16.5	12.6	11.1	8.7	ns
t_{en}	Enable time	OE-to-A or B	315	307	278	259	ns
t_{dis}	Disable time	OE-to-A or B	661	648	641	540	ns
t_{rA}, t_{fA}	Input rise time	A port rise and fall time	3	3.1	3.2	3	ns
t_{rB}, t_{fB}	Input rise time	B port rise and fall time	3.1	1.1	0.9	0.9	ns
Maximum data rate			50	50	50	50	Mbps

8.9 Switching Characteristics: V_{CCA}=2.5V ± 0.2V

over recommended operating free-air temperature range, V_{CCA}=2.5V±0.2V (unless otherwise noted)

PARAMETER		CONDITIONS	V_{CCB}=2.5V ±0.2V	V_{CCB}=3.3V ±0.3V	V_{CCB}=5V ±0.5V	UNIT
			TYP	TYP	TYP	
t_{PHL}	Propagation delay time high-to-low output	A-to-B	10	9	8.5	ns
t_{PLH}	Propagation delay time low-to-high output	A-to-B	10.5	9	8.3	ns
t_{PHL}	Propagation delay time high-to-low output	B-to-A	9.3	8.4	7.8	ns
t_{PLH}	Propagation delay time low-to-high output	B-to-A	9.3	7.8	7.5	ns
t_{en}	Enable time	OE-to-A or B	288	257	243	ns
t_{dis}	Disable time	OE-to-A or B	637	621	530	ns
t_{rA}, t_{fA}	Input rise time	A port rise and fall time	1	0.9	0.9	ns
t_{rB}, t_{fB}	Input rise time	B port rise and fall time	1.1	0.9	0.9	ns
Maximum data rate			70	80	80	Mbps

8.10 Switching Characteristics: V_{CCA}=3.3V ± 0.3V

over recommended operating free-air temperature range, V_{CCA}=3.3V±0.3V (unless otherwise noted)

	PARAMETER	CONDITIONS	V_{CCB}=3.3V ±0.3V	V_{CCB}=5V ±0.5V	UNIT
			TYP	TYP	
t_{PHL}	Propagation delay time high-to-low output	A-to-B	8.5	7.5	ns
t_{PLH}	Propagation delay time low-to-high output	A-to-B	8.4	7.3	ns
t_{PHL}	Propagation delay time high-to-low output	B-to-A	7.5	6.9	ns
t_{PLH}	Propagation delay time low-to-high output	B-to-A	8.1	7.5	ns
t_{en}	Enable time	OE-to-A or B	248	233	ns
t_{dis}	Disable time	OE-to-A or B	610	503	ns
t_{rA}	Input rise time	A port rise time	0.8	0.9	ns
t_{rB}	Input rise time	B port rise time	0.9	0.9	ns
t_{fA}	Input fall time	A port fall time	0.8	0.9	ns
t_{fB}	Input fall time	B port fall time	0.9	0.9	ns
Maximum data rate			80	100	Mbps

9 OPERATING CHARACTERISTICS

T_A=25°C

PARAMETER		CONDITIONS		V_{CCA}							UNIT
				1.2V	1.2V	1.5V	1.8V	2.5V	2.5V	3.3V	
				V_{CCB}							
				5V	1.8V	1.8V	1.8V	2.5V	5V	3.3V to 5V	
				TYP	TYP	TYP	TYP	TYP	TYP	TYP	
C_{pdA}	Power dissipation capacitance	C_L=0 f=10MHz t_r=t_f=1ns OE=V_{CCA} (outputs enabled)	A-port input B-port output	0.53	28	16	17	4	5	15	pF
			B-port input A-port output	11	11	11	11	11	11	11	
C_{pdB}	Power dissipation capacitance		A-port input B-port output	23	18	18	17	19	23	7	
			B-port input A-port output	41	24	20	20	19	35	23	
C_{pdA}	Power dissipation capacitance	C_L=0 f=10MHz t_r=t_f=1ns OE=GND (outputs enabled)	A-port input B-port output	0.01	0.01	0.01	0.01	0.01	0.01	0.01	pF
			B-port input A-port output	0.01	0.01	0.01	0.01	0.01	0.01	0.01	
C_{pdB}	Power dissipation capacitance		A-port input B-port output	0.01	0.01	0.01	0.01	0.01	0.01	0.01	
			B-port input A-port output	0.01	0.01	0.01	0.01	0.01	0.01	0.01	

10 PARAMETER MEASUREMENT INFORMATION

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

• PRR 10 MHz

• Z_O = 50 Ω

• dv/dt ≥ 1 V/ns

Note: All input pulses are measured one at a time, with one transition per measurement.
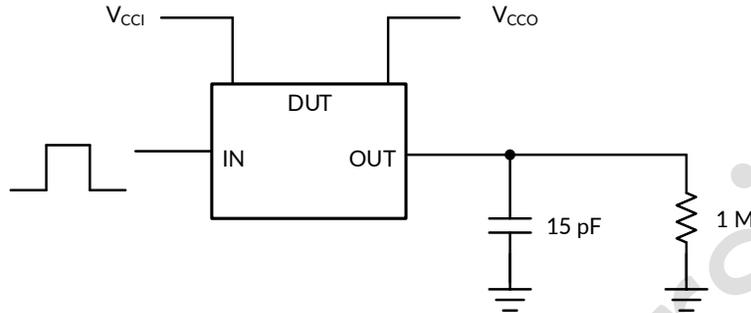
Figure 1. Data Rate, Pulse Duration, Propagation Delay, Output Rise And Fall Time Measurement Using A Push-Pull Driver
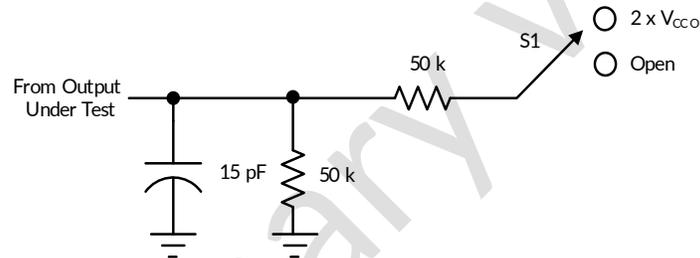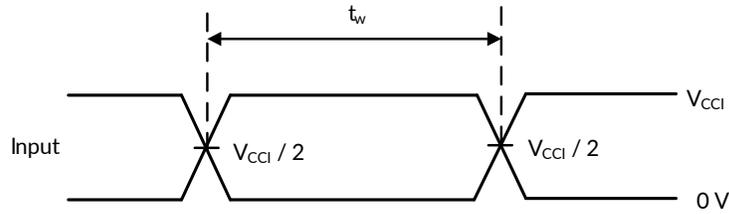
Figure 2. Load Circuit for Enable/Disable Time Measurement

Table 1. Switch Configuration for Enable/Disable Timing

TEST	S1
t_{PZL}[1], t_{PLZ}[2]	2 × V_{CCO}
t_{PHZL}[1], t_{PZH}[2]	Open

(1) t_{PZL} and t_{PZH} are the same as t_{en}.
(2) t_{PLZ} and t_{PHZ} are the same as t_{dis}.

(1) All input pulses are measured one at a time, with one transition per measurement.

Figure 3. Voltage Waveforms Pulse Duration
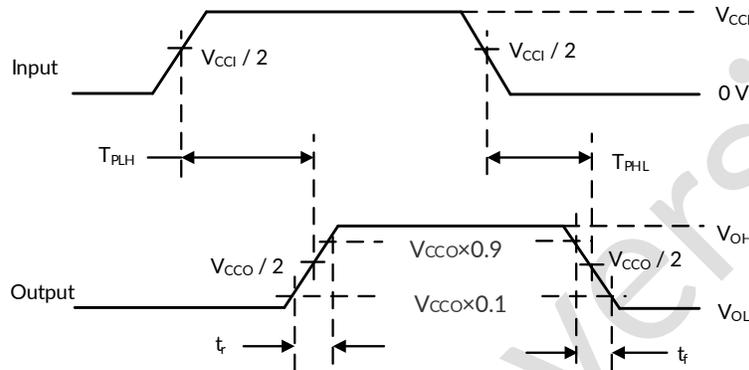
Figure 4. Voltage Waveforms Propagation Delay Times
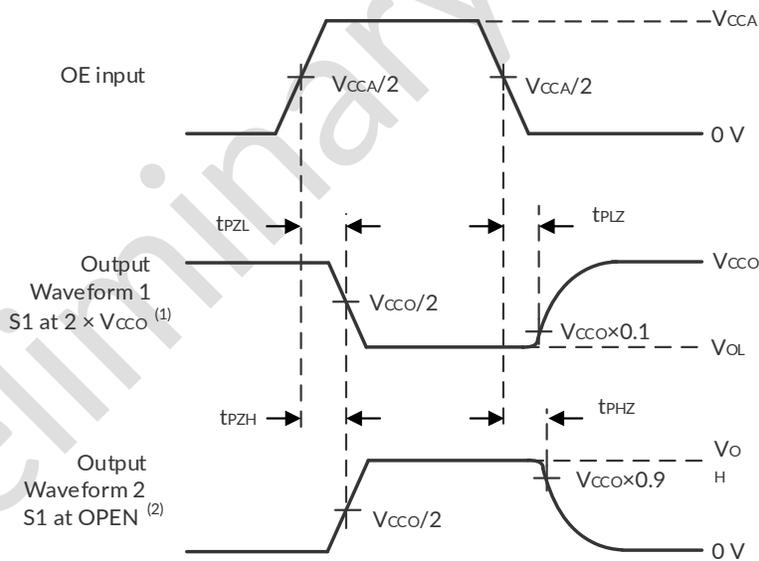
A. Waveform 1 is for an output with internal such that the output is high, except when OE is high.
B. Waveform 2 is for an output with conditions such that the output is low, except when OE is high.

Figure 5. Voltage Waveforms Enable and Disable

11 DETAILED DESCRIPTION

11.1 Overview

The RS0204A-Q1 device is a 4-bit, directionless voltage-level translator specifically designed for translating logic voltage levels. The A port is able to accept I/O voltages ranging from 1.2 V to 3.6 V, while the B port can accept I/O voltages from 1.65 V to 5.5 V. The device is a buffered architecture with edge-rate accelerators (one-shots) to improve the overall data rate. This device can only translate push-pull CMOS logic outputs. If for open-drain signal translation, please refer to RS010X products.

11.2 Architecture

The RS0204A-Q1 device architecture (see Figure 6) does not require a direction-control signal to control the direction of data flow from A to B or from B to A. In a DC state, the output drivers of the device maintain a high or low, but are designed to be weak, so the output drivers can be overdriven by an external driver when data on the bus flows the opposite direction.

The output one-shots detect rising or falling edges on the A or B ports. During a rising edge, the one-shot turns on the PMOS transistors (T1, T3) for a short duration, which speeds up the low-to-high transition. Similarly, during a falling edge, the one-shot turns on the NMOS transistors (T2, T4) for a short duration, which speeds up the high-to-low transition. The typical output impedance during output transition is 70 Ω at V_{CCO} = 1.2 V to 1.8 V, 50 Ω at V_{CCO} = 1.8 V to 3.3 V, and 40Ω at V_{CCO} = 3.3 V to 5 V.
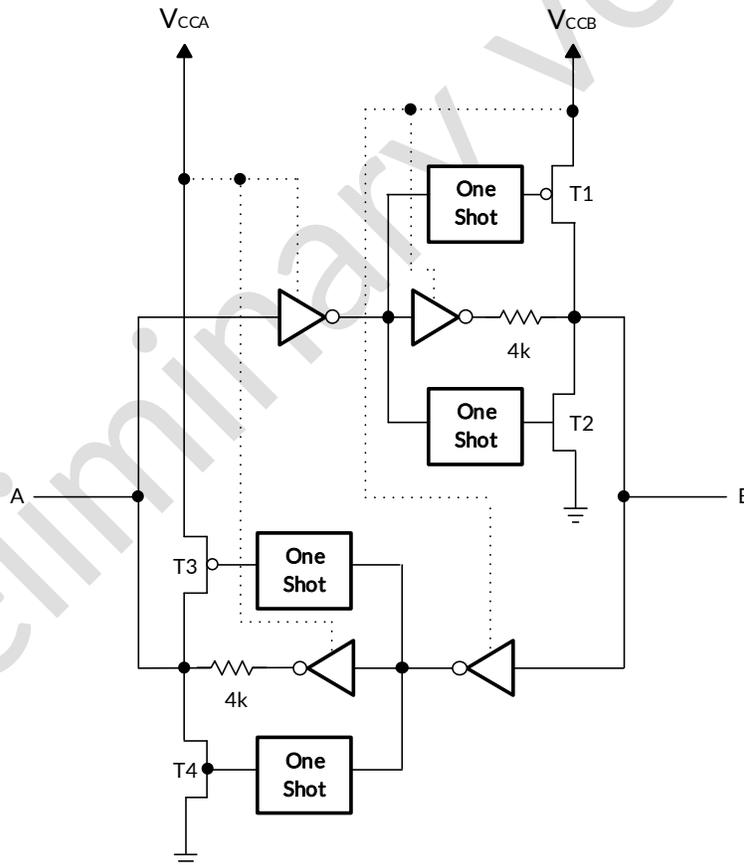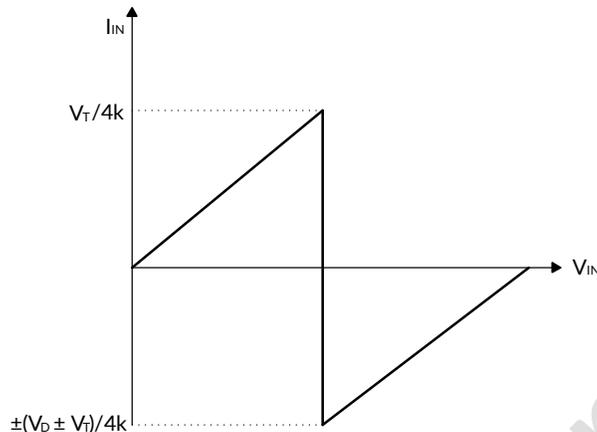

Figure 6. Architecture of RS0204A-Q1 Device I/O Cell

11.3 Input Driver Requirements

Typical I_{IN} vs V_{IN} characteristics of the device are shown in Figure 7. For proper operation, the device driving the data I/Os of the RS0204A-Q1 device must have driven strength of at least ±2 mA.

(1) V_T is the input threshold of the RS0204A-Q1 device, (typically V_{CC} / 2).
(2) V_D is the supply voltage of the external driver.

Figure 7. Typical I_{IN} vs V_{IN} Curve

11.4 Output Load Considerations

We recommend careful PCB layout practices with short PCB trace lengths to avoid excessive capacitive loading and to ensure that proper O.S. triggering takes place. PCB signal trace-lengths must be kept short enough such that the round-trip delay of any reflection is less than the one-shot duration. This improves signal integrity by ensuring that any reflection sees a low impedance at the driver. The O.S. circuits have been designed to stay on for approximately 10 ns. The maximum capacitance of the lumped load that can be driven also depends directly on the one-shot duration. With very heavy capacitive loads, the one-shot can time-out before the signal is driven fully to the positive rail. The O.S. duration has been set to best optimize trade-offs between dynamic I_{CC}, load driving capability, and maximum bit-rate considerations. Both PCB trace length and connectors add to the capacitance that the device output sees, so it is recommended that this lumped-load capacitance be considered to avoid O.S. retriggering, bus contention, output signal oscillations, or other adverse system-level affects.

11.5 Enable and Disable

The RS0204A-Q1 device has an OE input that is used to disable the device by setting OE = low, which places all I/Os in the high-impedance (Hi-Z) state. The disable time (t_{dis}) indicates the delay between when OE goes low and when the outputs actually get disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken high.

11.6 Pullup or Pulldown Resistors on I/O Lines

The device is designed to drive capacitive loads of up to 70 pF. The output drivers of the RS0204A-Q1 device have low dc drive strength. If pullup or pulldown resistors are connected externally to the data I/Os, their values must be kept higher than 50 kΩ to ensure that they do not contend with the output drivers of the RS0204A-Q1device.

For the same reason, the RS0204A-Q1 device must not be used in applications such as I^{2}C or 1-Wire where an open-drain driver is connected on the bidirectional data I/O. For these applications, use a device from the RS010X series of level translators.

11.7 Device Functional Modes

The device has two functional modes, enabled and disabled. To disable the device, set the OE input to low, which places all I/Os in a high impedance state. Setting the OE input to high will enable the device.

12 APPLICATION AND IMPLEMENTATION

Information in the following applications sections is not part of the RUNIC component specification, and RUNIC does not warrant its accuracy or completeness. RUNIC's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

12.1 Application Information

The RS0204A-Q1 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. It can only translate push-pull CMOS logic outputs. Any external pulldown or pullup resistors are recommended larger than 50 kΩ.
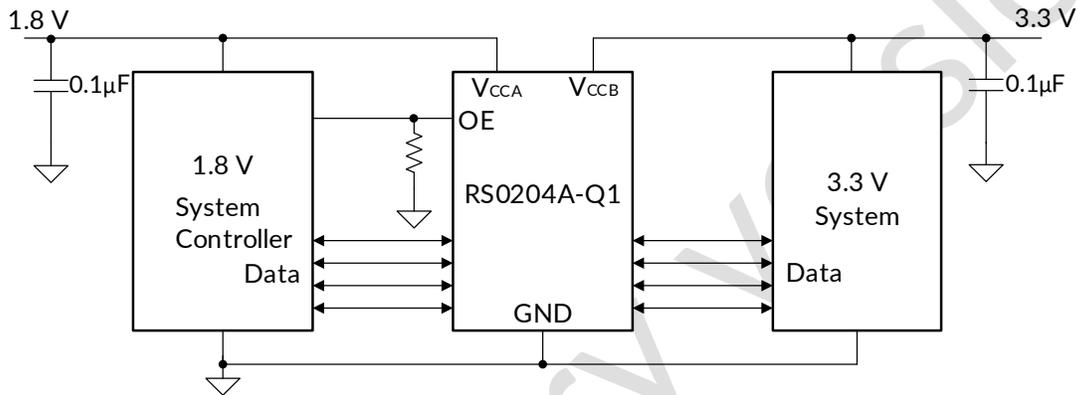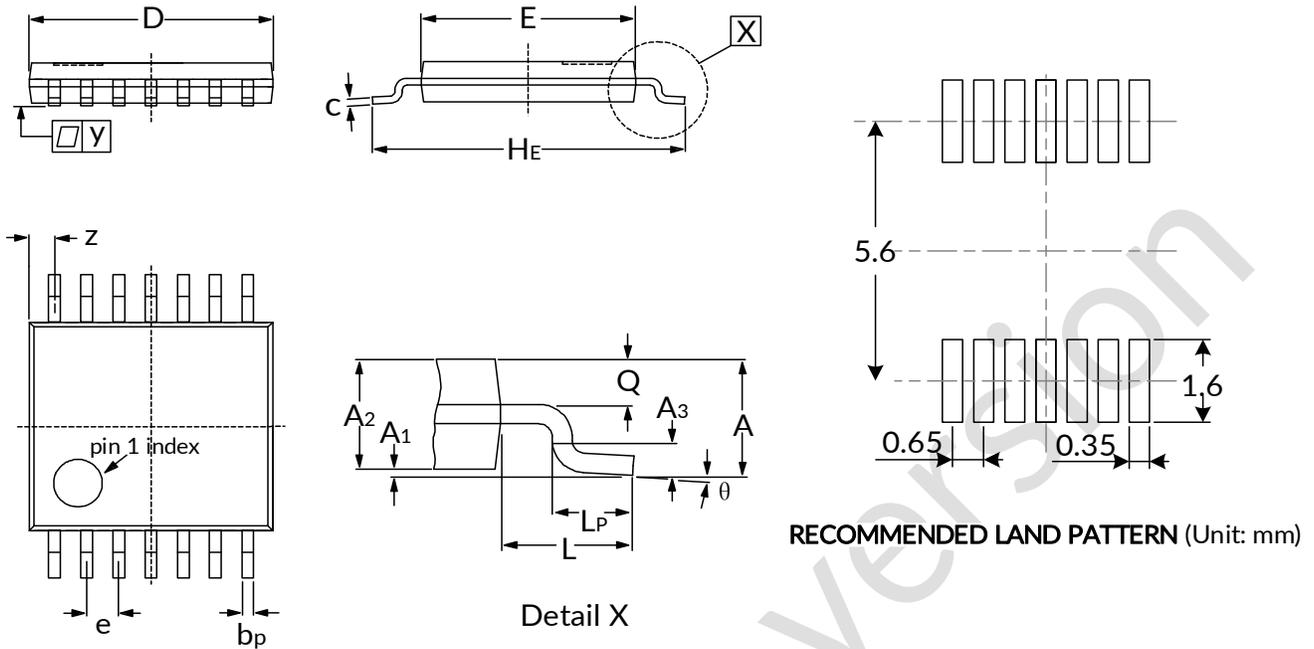
12.2 Typical Application


Figure 8. Typical Application Circuit

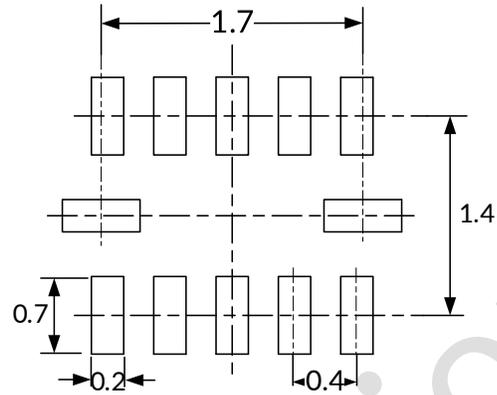# 13 PACKAGE OUTLINE DIMENSIONS

TSSOP14 [2]

Detail X

RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A [1]		1.100		0.043
A_1	0.050	0.150	0.002	0.006
A_2	0.800	0.950	0.031	0.037
A_3	0.250		0.010	
b_p	0.190	0.300	0.007	0.012
c	0.100	0.200	0.004	0.008
D [1]	4.900	5.100	0.193	0.201
E [1]	4.300	4.500	0.169	0.177
H_E	6.200	6.600	0.244	0.260
e	0.650		0.026	
L	1		0.039	
L_P	0.500	0.750	0.020	0.030
Q	0.300	0.400	0.012	0.016
Z	0.380	0.720	0.015	0.028
y	0.1		0.004	
θ	0°	8°	0°	8°

NOTE:
1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. This drawing is subject to change without notice.

UQFN1.7X2-12 [(2)]
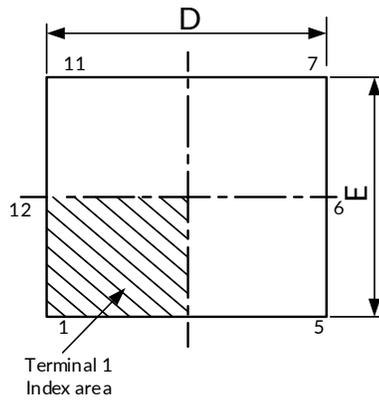
TOP VIEW

RECOMMENDED LAND PATTERN (Unit: mm)
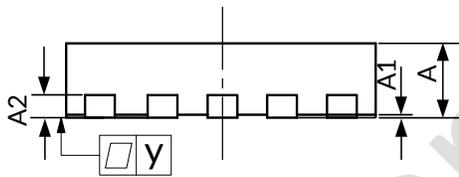
SIDE VIEW
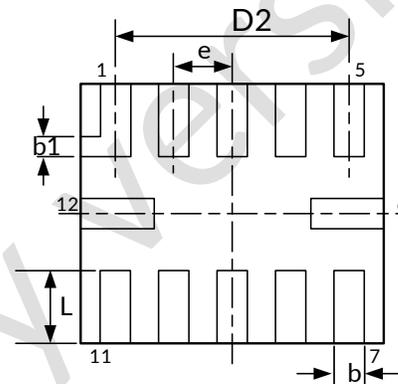
BOTTOM VIEW

| Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A [(1)]		0.500		0.020
A1	0.000	0.050	0.000	0.002
A2	0.127		0.005	
D [(1)]	1.900	2.100	0.075	0.083
E [(1)]	1.600	1.800	0.063	0.071
D2	1.500	1.700	0.059	0.067
b	0.150	0.250	0.006	0.010
b1	0.150		0.006	
e	0.400		0.016	
y	0.050		0.002	
L	0.450	0.550	0.017	0.022

NOTE:
1. Plastic or metal protrusions of 0.075mm maximum per side are not included.
2. This drawing is subject to change without notice.

14 TAPE AND REEL INFORMATION
REEL DIMENSIONS   TAPE DIMENSION
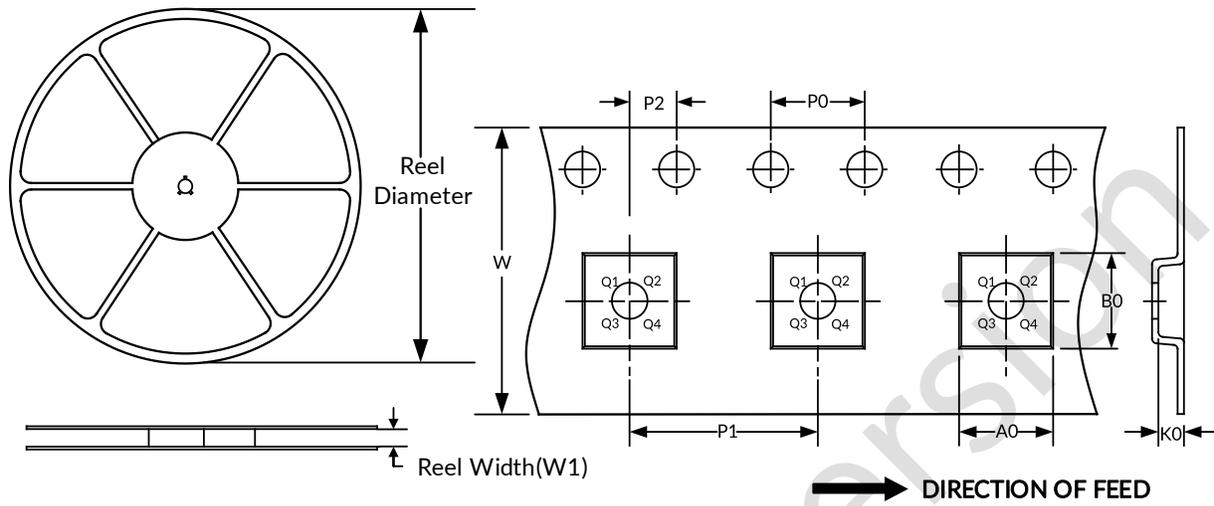
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP14	13"	12.4	6.95	5.60	1.20	4.0	8.0	2.0	12.0	Q1
UQFN1.7X2-12	7"	9.0	1.90	2.30	0.75	4.0	4.0	2.0	8.0	Q1

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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