芯伯乐®
XINBOLE

Product Specification

XBLW CD4017

5-stage Johnson Decade Counter

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Description

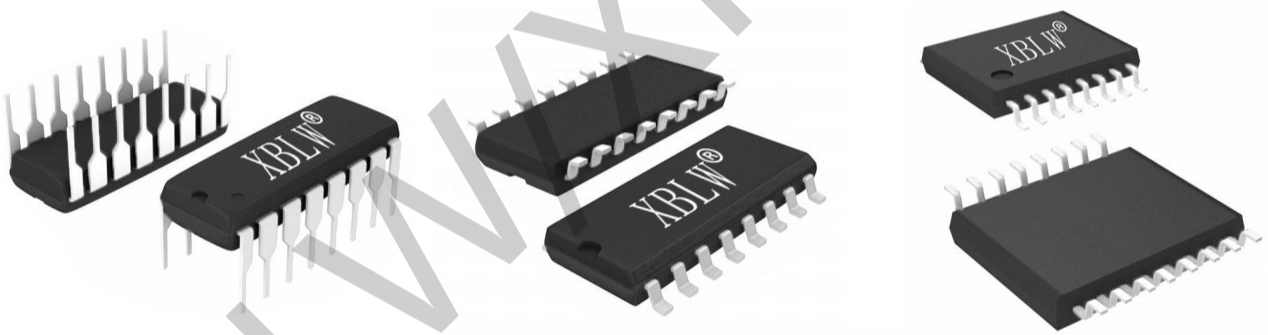
The CD4017 is a 5-stage Johnson decade counter with ten spike-free decoded active HIGH outputs (Q0 to Q9), an active LOW carry output from the most significant flip-flop ($\overline{Q}$5-9), active HIGH and active LOW clock inputs (CP0, $\overline{CP}$1) and an overriding asynchronous master reset input (MR).

The counter is advanced by either a LOW-to-HIGH transition at CP0 while $\overline{CP}$1 is LOW or a HIGH-to-LOW transition at $\overline{CP}$1 while CP0 is HIGH.

When cascading counters, the $\overline{Q}$5-9 output, which is LOW while the counter is in states 5, 6, 7, 8, and 9, can be used to drive the CP0 input of the next counter. A HIGH on MR resets the counter to zero (Q0=$\overline{Q}$ 5-9=HIGH; Q1 to Q9=LOW) independent of the clock inputs (CP0, $\overline{CP}$1).

Automatic counter code correction is provided by an internal circuit: following any illegal code the counter returns to a proper counting mode within 11 clock pulses.

It operates over a recommended V_{DD} power supply range of 3V to 15V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD}, V_{SS}, or another input.



DIP-16　　SOP-16　　TSSOP-16

Feature

- Wide supply voltage range from 3V to 15V
- Automatic counter correction
- Tolerant of slow clock rise and fall times
- 5V, 10V, and 15V parametric ratings
- Standardized symmetrical output characteristics
- Specified from -40℃ to +85℃
- Packaging information: DIP16/ SOP16/ TSSOP16

Ordering Information

Product Model	Package Type	Marking	Packing	Packing Qty
CD4017BE	DIP-16	CD4017BE	Tube	1000/Box
CD4017BDTR	SOP-16	CD4017B	Tape	2500/Reel
CD4017BTDTR	TSSOP-16	CD4017B	Tape	3000/Reel

Block Diagram

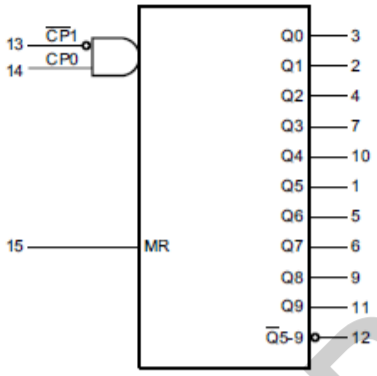


Figure 1 . Logic symbol

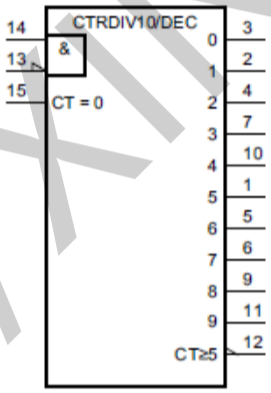


Figure 2 . IEE logic symbol

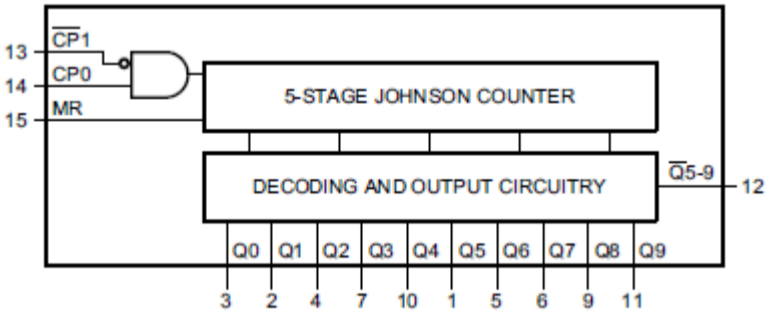


Figure 3 . Functional diagram

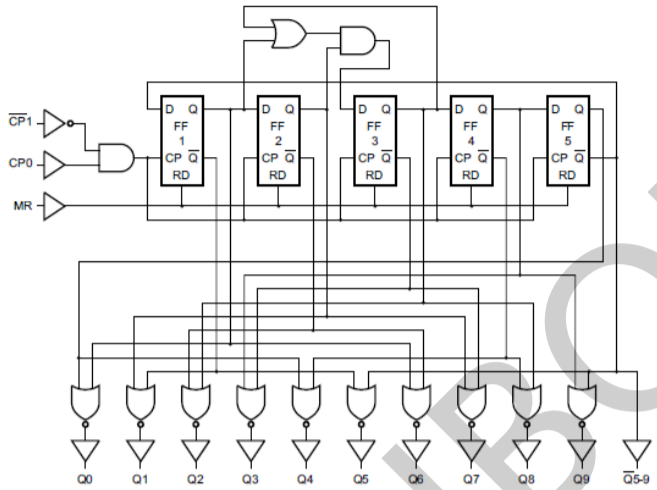


Figure 4 . Logic diagram

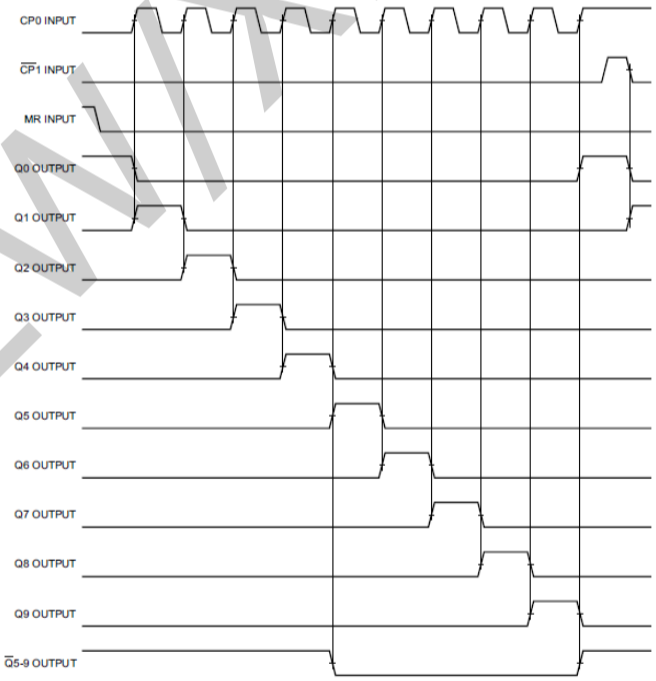
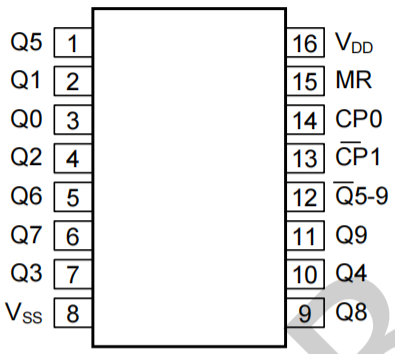


Figure 5 . Timing diagram

Pin Configurations



Pin Description

Pin No.	Pin Name	Description
1	Q5	decoded output
2	Q1	decoded output
3	Q0	decoded output
4	Q2	decoded output
5	Q6	decoded output
6	Q7	decoded output
7	Q3	decoded output
8	VSS	ground (0 V)
9	Q8	decoded output
10	Q4	decoded output
11	Q9	decoded output
12	$\overline{Q}$5-9	carry output (active LOW)
13	$\overline{CP}$1	clock input (HIGH- to- LOW edge- triggered)
14	CP0	clock input (LOW- to- HIGH edge- triggered)
15	MR	master reset input
16	VDD	supply voltage

Function Table

Input			Operation
MR	CP0	C—P1	
H	X	X	Q0= $\overline{Q}$5 - 9 = H; Q1 to Q9= L
L	H	↓	counter advances
L	↑	L	counter advances
L	L	X	no change
L	X	H	no change
L	H	↑	no change
L	↓	L	no change

Note: H= HIGH voltage level; L= LOW voltage level; X= don't care; ↑ =positive- going transition; ↓=negative- going transition.

Electrical Parameter

Absolute Maximum Ratings

(Voltages are referenced to V_{SS} (ground=0 V) , unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V_{DD}	-		-0.5	+18	V
DC input current	I_{IK}	any one input		-	±10	mA
input voltage	V_I	all inputs		-0.5	V_{DD}+0.5	V
storage temperature	T_{stg}	-		-65	+150	℃
total power dissipation	P_{tot}	-		-	500	mW
device dissipation	P	per output transistor		-	100	mW
Soldering temperature	T_L	10s	DIP	245		℃
			SOP	250		

Note:

[1] For DIP16 packages: above 70℃ the value of P_{tot} derates linearly with 12 mW/K.

[2] For SOP16 packages: above 70℃ the value of P_{tot} derates linearly with 8 mW/K.

[3] For (T) SSOP16 packages: above 60℃ the value of P_{tot} derates linearly with 5.5 mW/K.

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{DD}	-	3	-	15	V
ambient temperature	T_{amb}	in free air	-40	-	+125	℃
clock input frequency	f_{CL}	V_{DD}=5V	-	-	2.5	MHz
		V_{DD}=10V	-	-	5	MHz
		V_{DD}=15V	-	-	5.5	MHz
clock pulse width	t_w	V_{DD}=5V	200	-	-	ns
		V_{DD}=10V	90	-	-	ns
		V_{DD}=15V	60	-	-	ns
clock rise and fall time	t_{rCL}, t_{fCL}	V_{DD}=5V	unlimited			-
		V_{DD}=10V				-
		V_{DD}=15V				-
clock inhibit setup time	t_s	V_{DD}=5V	230	-	-	ns
		V_{DD}=10V	100	-	-	ns
		V_{DD}=15V	70	-	-	ns
reset pulse width	t_{RW}	V_{DD}=5V	260	-	-	ns
		V_{DD}=10V	110	-	-	ns
		V_{DD}=15V	60	-	-	ns
reset removal time	t_{rec}	V_{DD}=5V	400	-	-	ns
		V_{DD}=10V	280	-	-	ns
		V_{DD}=15V	150	-	-	ns

Electrical Characteristics

DC Characteristics 1

(T_{amb}=25℃, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions (V)			T_{amb}=25℃			Unit
		V_O	V_{IN}	V_{DD}	Min.	Typ.	Max.	
supply current	I_{DD}	-	0, 5	5	-	-	5	uA
		-	0, 10	10	-	-	10	uA
		-	0, 15	15	-	-	20	uA
LOW-level output current	I_{OL}	0.4	0, 5	5	0.51	1	-	mA
		0.5	0, 10	10	1.3	2.6	-	mA
		1.5	0, 15	15	3.4	6.8	-	mA
HIGH-level output current	I_{OH}	4.6	0, 5	5	-0.51	-1	-	mA
		2.5	0, 5	5	-1.6	-3.2	-	mA
		9.5	0, 10	10	-1.3	-2.6	-	mA
		13.5	0, 15	15	-3.4	-6.8	-	mA
LOW-level output voltage	V_{OL}	-	0, 5	5	-	0	0.05	V
		-	0, 10	10	-	0	0.05	V
		-	0, 15	15	-	0	0.05	V
HIGH-level output voltage	V_{OH}	-	0, 5	5	4.95	5	-	V
		-	0, 10	10	9.95	10	-	V
		-	0, 15	15	14.95	15	-	V
LOW-level input voltage	V_{IL}	0.5, 4.5	-	5	-	-	1.5	V
		1, 9	-	10	-	-	3	V
		1.5, 13.5	-	15	-	-	4	V
HIGH-level input voltage	V_{IH}	0.5, 4.5	-	5	3.5	-	-	V
		1, 9	-	10	7	-	-	V
		1.5, 13.5	-	15	11	-	-	V
input leakage current	I_I	-	0, 15	15	-	-	±1	uA

DC Characteristics 2

(T_{amb}=-40℃ to +125℃, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions (V)			T_{amb}=-40℃		T_{amb}=+85℃		T_{amb}=+125℃		Unit
		V_O	V_{IN}	V_{DD}	Min.	Max.	Min.	Max.	Min.	Max.	
supply current	I_{DD}	-	0, 5	5	-	5	-	150	-	150	uA
		-	0, 10	10	-	10	-	300	-	300	uA
		-	0, 15	15	-	20	-	600	-	600	uA
LOW-level output current	I_{OL}	0.4	0, 5	5	0.61	-	0.42	-	0.36	-	mA
		0.5	0, 10	10	1.5	-	1.1	-	0.9	-	mA
		1.5	0, 15	15	4	-	2.8	-	2.4	-	mA
HIGH-level output current	I_{OH}	4.6	0, 5	5	-0.61	-	-0.42	-	-0.36	-	mA
		2.5	0, 5	5	-1.8	-	-1.3	-	-1.15	-	mA
		9.5	0, 10	10	-1.5	-	-1.1	-	-0.9	-	mA
		13.5	0, 15	15	-4.2	-	-2.8	-	-2.4	-	mA
LOW-level output voltage	V_{OL}	-	0, 5	5	-	0.05	-	0.05	-	0.05	V
		-	0, 10	10	-	0.05	-	0.05	-	0.05	V
		-	0, 15	15	-	0.05	-	0.05	-	0.05	V
HIGH-level output voltage	V_{OH}	-	0, 5	5	4.95	-	4.95	-	4.95	-	V
		-	0, 10	10	9.95	-	9.95	-	9.95	-	V
		-	0, 15	15	14.95	-	14.95	-	14.95	-	V
LOW-level input voltage	V_{IL}	0.5, 4.5	-	5	-	1.5	-	1.5	-	1.5	V
		1, 9	-	10	-	3	-	3	-	3	V
		1.5, 13.5	-	15	-	4	-	4	-	4	V
HIGH-level input voltage	V_{IH}	0.5, 4.5	-	5	3.5	-	3.5	-	3.5	-	V
		1, 9	-	10	7	-	7	-	7	-	V
		1.5, 13.5	-	15	11	-	11	-	11	-	V
input leakage current	I_I	-	0, 15	15	-	±1	-	±1	-	±1	uA

AC Characteristics

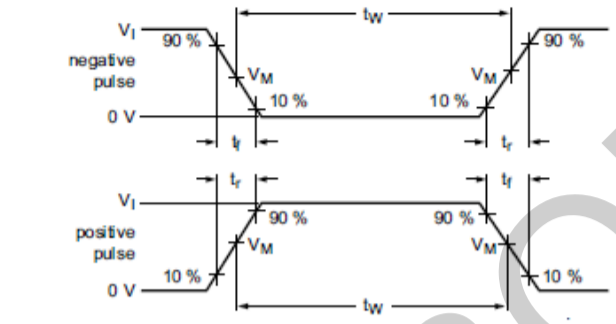
(T_{amb}=25℃, V_{SS}=0V, t_r, t_f=20ns, C_L=50pF, R_L=200kΩ, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
propagation delay time	t_{PHL}, t_{PLH}	CP0, $\overline{CP}$1 to Q0 to Q9; see Figure 7	V_{DD}=5V	-	325	650	ns
			V_{DD}=10V	-	135	270	ns
			V_{DD}=15V	-	85	170	ns
		CP0, $\overline{CP}$1 to $\overline{Q}$5-9; see Figure 7	V_{DD}=5V	-	300	600	ns
			V_{DD}=10V	-	125	250	ns
			V_{DD}=15V	-	80	160	ns
		MR to Q0 to Q9; see Figure 7	V_{DD}=5V	-	265	530	ns
			V_{DD}=10V	-	115	230	ns
			V_{DD}=15V	-	85	170	ns
transition time	t_t	see Figure 7	V_{DD}=5V	-	100	200	ns
			V_{DD}=10V	-	50	100	ns
			V_{DD}=15V	-	40	80	ns
pulse width	t_W	see Figure 8	V_{DD}=5V	-	100	200	ns
			V_{DD}=10V	-	45	90	ns
			V_{DD}=15V	-	30	60	ns
clock rise and fall time	t_{rCL}, t_{fCL}	-	V_{DD}=5V	unlimited			-
			V_{DD}=10V				-
			V_{DD}=15V				-
maximum clock frequency	f_{CL}	see Figure 8	V_{DD}=5V	2.5	5	-	MHz
			V_{DD}=10V	5	10	-	MHz
			V_{DD}=15V	5.5	11	-	MHz
setup time	t_s	CP0 to $\overline{CP}$1; see Figure 9	V_{DD}=5V	-	115	230	ns
			V_{DD}=10V	-	50	100	ns
			V_{DD}=15V	-	35	70	ns
reset removal time	t_{rec}	MR input; see Figure 8	V_{DD}=5V	-	200	400	ns
			V_{DD}=10V	-	140	280	ns
			V_{DD}=15V	-	75	150	ns
input capacitance	C_I	any input		-	5	-	pF

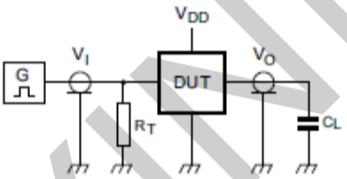
Note: t_t is the same as t_{TLH} and t_{THL}.

Testing Circuit

AC Testing Circuit



a. Input waveforms



b. Test circuit

Figure 6. Test circuit for switching times

Definitions for test circuit: DUT= Device Under Test.

C_L= Load capacitance including jig and probe capacitance.

R_T= Termination resistance should be equal to the output impedance Z_o of the pulse generator.

AC Testing Waveforms

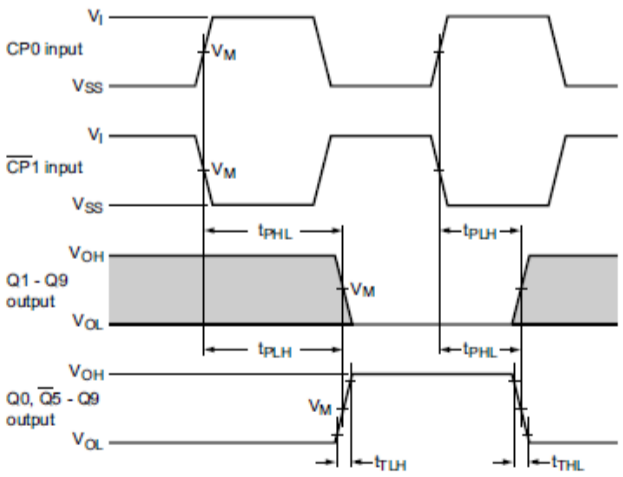


Figure 7. Waveforms showing the propagation delays for CP0, $\overline{CP}$1 to Qn, $\overline{Q}$5-9 outputs and the output transition times

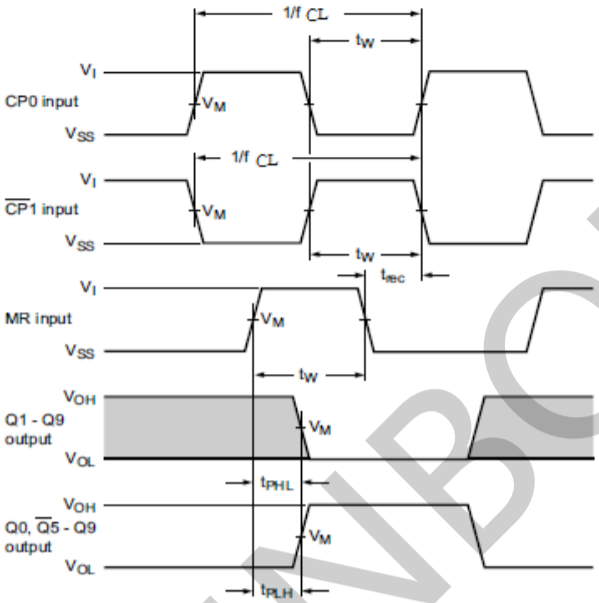


Figure 8. Waveforms showing the minimum pulse width for CP0, $\overline{CP}1$ and MR input; the maximum frequency for CP0 and $\overline{CP}1$ input; the recovery time for MR and the MR input to Qn and $\overline{Q}5$-9 output propagation dela

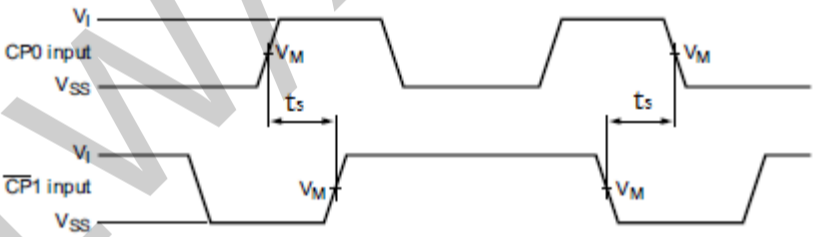


Figure 9. Waveforms showing hold times for CP0 to $\overline{CP}1$ and $\overline{CP}1$ to CP0

Measurement Points

Supply voltage	Input	Output
V_{DD}	V_M	V_M
5V to 15V	$0.5\times V_{DD}$	$0.5\times V_{DD}$

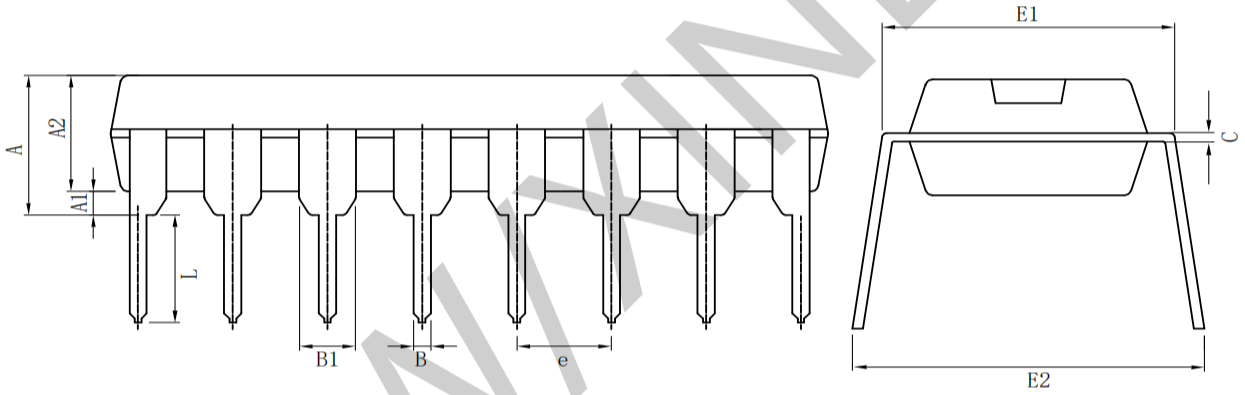
Test Data

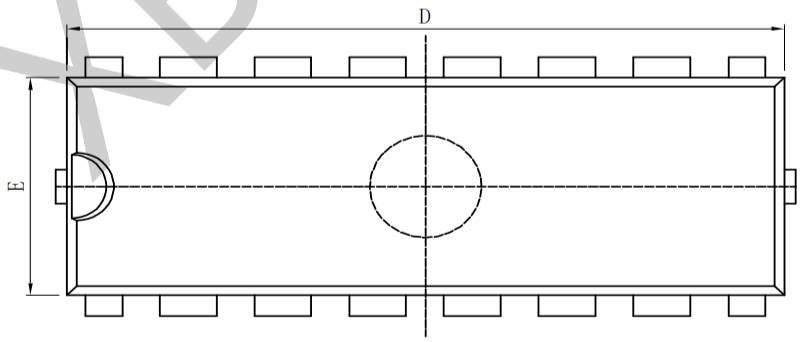
Supply voltage	Input		Load
V_{DD}	V_I	t_r , t_f	C_L
5V to 15V	V_{SS} or V_{DD}	≤ 20ns	50pF

Package Information

· DIP-16

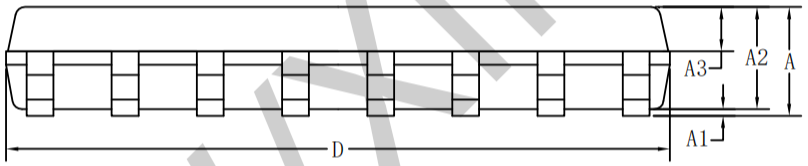
Size / Symbol	Dimensions In Millimeters		Size / Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A	3.710	4.310	A	0.146	0.170
A1	0.510		A1	0.020	
A2	3.200	3.600	A2	0.126	0.142
B	0.380	0.570	B	0.015	0.022
B1	1.524(BSC)		B1	0.060(BSC)	
C	0.204	0.360	C	0.008	0.014
D	18.80	19.20	D	0.740	0.756
E	6.200	6.600	E	0.244	0.260
E1	7.320	7.920	E1	0.288	0.312
e	2.540(BSC)		e	0.100(BSC)	
L	3.000	3.600	L	0.118	0.142
E2	8.400	9.000	E2	0.331	0.354

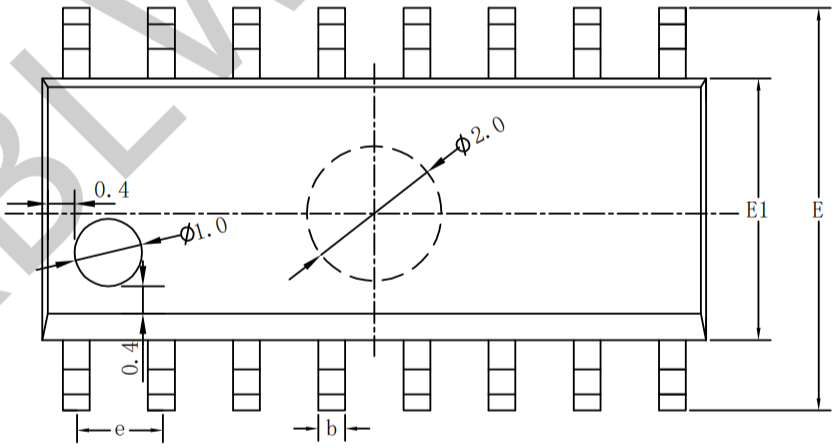


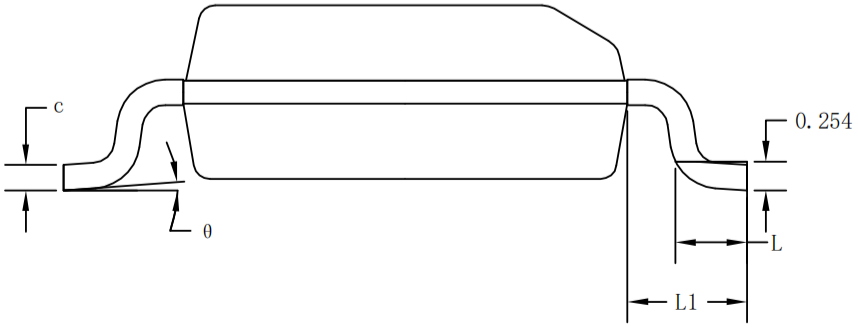


· SOP-16

Size / Symbol	Dimensions In Millimeters			Size / Symbol	Dimensions In Inches		
	Min(mm)	Nom(mm)	Max(mm)		Min(in)	Nom(in)	Max(in)
A	1.500	1.600	1.700	A	0.059	0.063	0.067
A1	0.100	0.150	0.250	A1	0.004	0.006	0.010
A2	1.400	1.450	1.500	A2	0.055	0.057	0.059
A3	0.600	0.650	0.700	A3	0.024	0.026	0.028
b	0.300	0.400	0.500	b	0.012	0.016	0.020
c	0.150	0.200	0.250	c	0.006	0.008	0.010
D	9.800	9.900	10.00	D	0.386	0.390	0.394
E	5.800	6.000	6.200	E	0.228	0.236	0.244
E1	3.850	3.900	3.950	E1	0.152	0.154	0.156
e		1.27(BSC)		e		0.050(BSC)	
L	0.500	0.600	0.700	L	0.020	0.024	0.028
L1		1.05(BSC)		L1		0.041(BSC)	
θ	0°	4°	8°	θ	0°	4°	8°

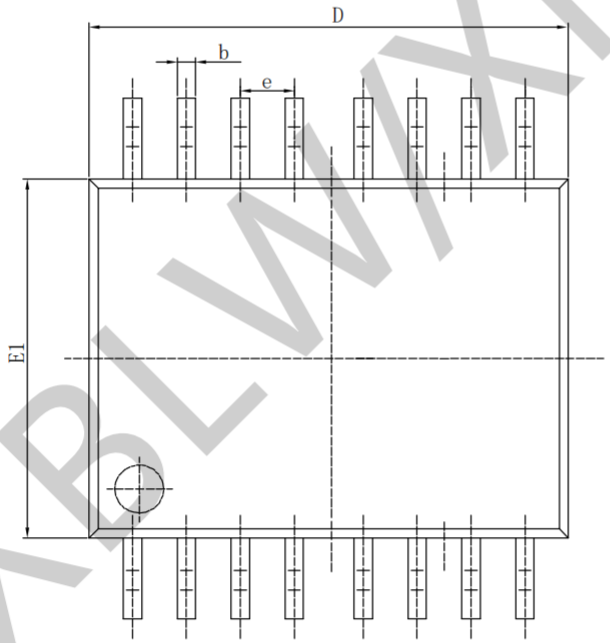


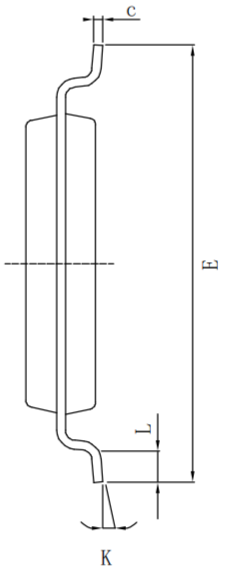


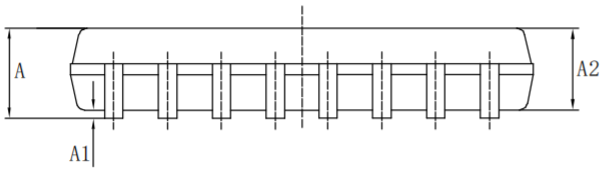


· TSSOP-16

Size / Symbol	Dimensions In Millimeters		Size / Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A		1.200	A		0.047
A1	0.050	0.150	A1	0.002	0.006
A2	0.800	1.050	A2	0.031	0.041
b	0.190	0.300	b	0.007	0.012
c	0.090	0.200	c	0.004	0.0089
D	4.900	5.100	D	0.193	0.201
E	6.200	6.600	E	0.244	0.260
E1	4.300	4.480	E1	0.169	0.176
e	0.65(BSC)		e	0.0256(BSC)	
K	0°	8°	K	0°	8°
L	0.450	0.750	L	0.018	0.030







Statement:

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