

Product Specification

XBLW SN74HC74

Dual D-type flip-flop with set and reset;
positive-edge trigger

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Description

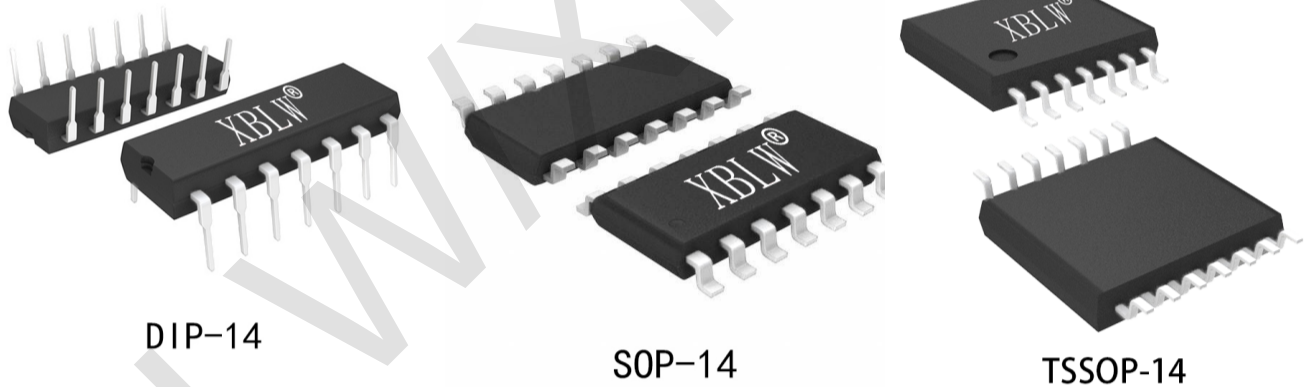
The SN74HC74 is a dual positive edge triggered D-type flip-flop. They have individual data (nD), clock (nCP), set ($n\bar{SD}$) and reset ($n\bar{RD}$) inputs, and complementary nQ and $n\bar{Q}$ outputs. Data at the nD -input, that meets the set-up and hold time requirements on the LOW-to-HIGH clock transition, is stored in the flip-flop and appears at the nQ output. Schmitt-trigger action in the clock input, makes the circuit highly tolerant to slower clock rise and fall times. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

Features

- Buffered inputs
- Wide operating voltage range: 2 V to 6 V
- Symmetrical output impedance
- Low power dissipation
- Balanced propagation delays
- Specified from -40°C to $+125^{\circ}\text{C}$
- Packaging information: DIP-14/SOP-14/TSSOP-14

Applications

- Convert a momentary switch to a toggle switch
- Divide a clock signal by 2 or 4



Ordering Information

Product Model	Package Type	Marking	Packing	Packing Qty
XBLW SN74HC74N	DIP-14	74HC74N	Tube	1000Pcs/Box
XBLW SN74HC74DTR	SOP-14	74HC74	Tape	2500Pcs/Reel
XBLW SN74HC74TDTR	TSSOP-14	74HC74	Tape	3000Pcs/Reel

Block Diagram

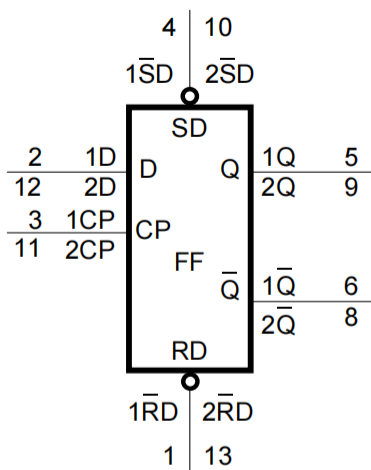


Figure 1. Logic symbol

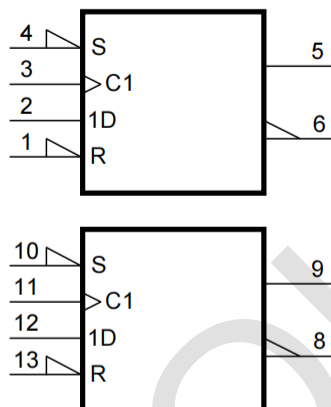


Figure 2. IEC logic symbol

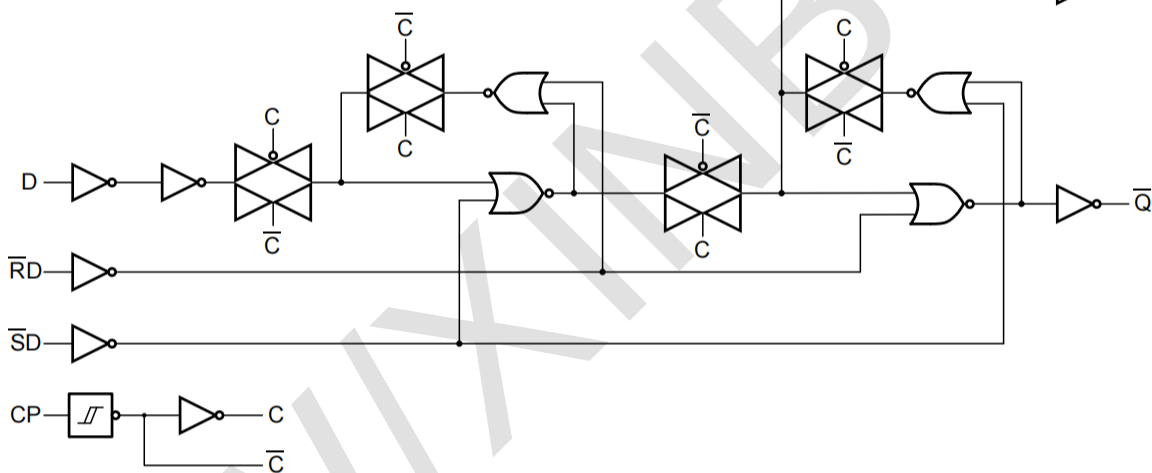


Figure 3. Logic diagram for one flip-flop

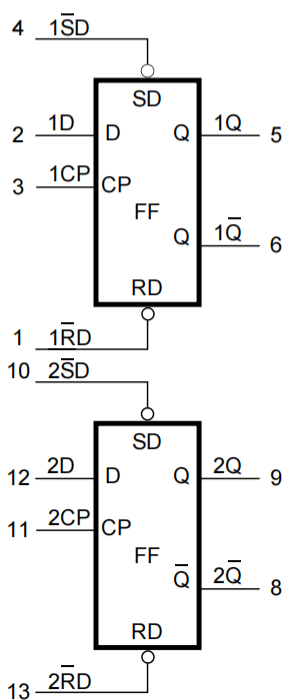
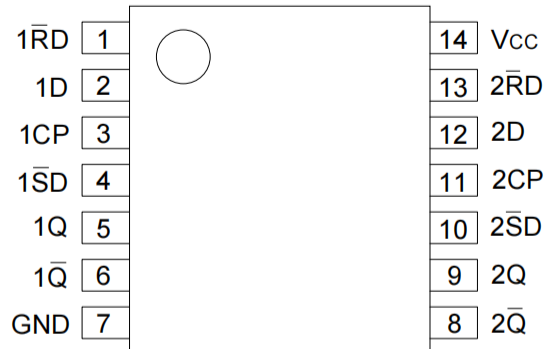


Figure 4. Functional diagram

Pin Configurations



Pin Description

Pin No.	Pin Name	Description
1	$\overline{1RD}$	asynchronous reset-direct input (active LOW)
2	1D	data input
3	1CP	clock input (LOW-to-HIGH, edge-triggered)
4	$\overline{1SD}$	asynchronous set-direct input (active LOW)
5	1Q	output
6	$\overline{1Q}$	complement output
7	GND	ground (0V)
8	$\overline{2Q}$	complement output
9	2Q	output
10	$\overline{2SD}$	asynchronous set-direct input (active LOW)
11	2CP	clock input (LOW-to-HIGH, edge-triggered)
12	2D	data input
13	$\overline{2RD}$	asynchronous reset-direct input (active LOW)
14	V _{CC}	supply voltage

Function Table

Input				Output	
$\overline{nSD}$	$\overline{nRD}$	nCP	nD	nQ	$\overline{nQ}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

Input				Output	
$\overline{nSD}$	$\overline{nRD}$	nCP	nD	nQ _{n+1}	$\overline{nQ}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care;

↑=LOW-to-HIGH transition; Q_{n+1}=state after the next LOW-to-HIGH CP transition.

Electrical Parameter

Absolute Maximum Ratings

(Voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V _{CC}	-		-0.5	+7	V
input clamping current	I _{IK}	V _I < -0.5V or V _I > V _{CC} +0.5V		-	±20	mA
output clamping current	I _{OK}	V _O < -0.5V or V _O > V _{CC} +0.5V		-	±20	mA
output current	I _O	-0.5V < V _O < V _{CC} +0.5V		-	±25	mA
supply current	I _{CC}	-		-	100	mA
ground current	I _{GND}	-		-100	-	mA
total power dissipation	P _{tot}	-		-	500	mW
storage temperature	T _{stg}	-		-65	+150	°C
soldering temperature	T _L	10s	DIP	245		°C
			SOP/TSSOP	260		

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{CC}	-	2.0	5.0	6.0	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
input transition rise and fall rate	$\Delta t/\Delta V$	$V_{CC}=2.0V$	-	-	625	ns/V
		$V_{CC}=4.5V$	-	1.67	139	ns/V
		$V_{CC}=6.0V$	-	-	83	ns/V
ambient temperature	T_{amb}	-	-40	-	+125	°C

Electrical Characteristics

DC Characteristics 1

($T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	$V_{CC}=2.0\text{V}$	1.5	1.2	-	V
		$V_{CC}=4.5\text{V}$	3.15	2.4	-	V
		$V_{CC}=6.0\text{V}$	4.2	3.2	-	V
LOW-level input voltage	V_{IL}	$V_{CC}=2.0\text{V}$	-	0.8	0.5	V
		$V_{CC}=4.5\text{V}$	-	2.1	1.35	V
		$V_{CC}=6.0\text{V}$	-	2.8	1.8	V
HIGH-level output voltage	V_{OH}	$V_I = V_{IH}$ or V_{IL} $I_O = -4.0\text{mA}$; $V_{CC}=4.5\text{V}$	3.84	4.32	-	V
		$I_O = -5.2\text{mA}$; $V_{CC}=6.0\text{V}$	5.34	5.81	-	V
LOW-level output voltage	V_{OL}	$V_I = V_{IH}$ or V_{IL} $I_O = 4.0\text{mA}$; $V_{CC}=4.5\text{V}$	-	0.15	0.33	V
		$I_O = 5.2\text{mA}$; $V_{CC}=6.0\text{V}$	-	0.16	0.33	V
input leakage current	I_I	$V_I = V_{CC}$ or GND; $V_{CC}=6.0\text{V}$	-	-	± 1.0	μA
supply current	I_{CC}	$V_I = V_{CC}$ or GND; $I_O = 0\text{A}$; $V_{CC}=6.0\text{V}$	-	-	40	μA
input capacitance	C_I	-	-	3.5	-	pF

DC Characteristics 2

($T_{amb} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	$V_{CC}=2.0\text{V}$	1.5	-	-	V
		$V_{CC}=4.5\text{V}$	3.15	-	-	V
		$V_{CC}=6.0\text{V}$	4.2	-	-	V
LOW-level input voltage	V_{IL}	$V_{CC}=2.0\text{V}$	-	-	0.5	V
		$V_{CC}=4.5\text{V}$	-	-	1.35	V
		$V_{CC}=6.0\text{V}$	-	-	1.8	V
HIGH-level output voltage	V_{OH}	$V_I = V_{IH}$ or V_{IL} $I_O = -4.0\text{mA}$; $V_{CC}=4.5\text{V}$	3.7	-	-	V
		$I_O = -5.2\text{mA}$; $V_{CC}=6.0\text{V}$	5.2	-	-	V
LOW-level output voltage	V_{OL}	$V_I = V_{IH}$ or V_{IL} $I_O = 4.0\text{mA}$; $V_{CC}=4.5\text{V}$	-	-	0.4	V
		$I_O = 5.2\text{mA}$; $V_{CC}=6.0\text{V}$	-	-	0.4	V
input leakage current	I_I	$V_I = V_{CC}$ or GND; $V_{CC}=6.0\text{V}$	-	-	± 1.0	μA
supply current	I_{CC}	$V_I = V_{CC}$ or GND; $I_O = 0\text{A}$; $V_{CC}=6.0\text{V}$	-	-	80	μA

AC Characteristics 1

($T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
nCP to nQ, nQ propagation delay	t_{pd}	see Figure 6 ^[1]	$V_{CC}=2.0\text{V}$	-	47	220 ns
			$V_{CC}=4.5\text{V}$	-	17	44 ns
			$V_{CC}=5.0\text{V}; C_L=15\text{pF}$	-	14	- ns
			$V_{CC}=6.0\text{V}$	-	14	37 ns
nSD to nQ, nQ propagation delay	t_{pd}	see Figure 7 ^[1]	$V_{CC}=2.0\text{V}$	-	50	250 ns
			$V_{CC}=4.5\text{V}$	-	18	50 ns
			$V_{CC}=5.0\text{V}; C_L=15\text{pF}$	-	15	- ns
			$V_{CC}=6.0\text{V}$	-	14	43 ns
nRD to nQ, nQ propagation delay	t_{pd}	see Figure 7 ^[1]	$V_{CC}=2.0\text{V}$	-	52	250 ns
			$V_{CC}=4.5\text{V}$	-	19	50 ns
			$V_{CC}=5.0\text{V}; C_L=15\text{pF}$	-	16	- ns
			$V_{CC}=6.0\text{V}$	-	15	43 ns
nQ, nQ transition time	t_t	see Figure 6 ^[2]	$V_{CC}=2.0\text{V}$	-	19	95 ns
			$V_{CC}=4.5\text{V}$	-	7	19 ns
			$V_{CC}=6.0\text{V}$	-	6	16 ns
CP pulse width	t_w	see Figure 6	$V_{CC}=2.0\text{V}$	100	19	- ns
			$V_{CC}=4.5\text{V}$	20	7	- ns
			$V_{CC}=6.0\text{V}$	17	6	- ns
nSD, nRD pulse width	t_w	see Figure 7	$V_{CC}=2.0\text{V}$	100	19	- ns
			$V_{CC}=4.5\text{V}$	20	7	- ns
			$V_{CC}=6.0\text{V}$	17	6	- ns
nSD, nRD recovery time	t_{rec}	see Figure 7	$V_{CC}=2.0\text{V}$	40	3	- ns
			$V_{CC}=4.5\text{V}$	8	1	- ns
			$V_{CC}=6.0\text{V}$	7	1	- ns
nD to nCP set-up time	t_{su}	see Figure 6	$V_{CC}=2.0\text{V}$	75	6	- ns
			$V_{CC}=4.5\text{V}$	15	2	- ns
			$V_{CC}=6.0\text{V}$	13	2	- ns
nD to nCP hold time	t_h	see Figure 6	$V_{CC}=2.0\text{V}$	3	-6	- ns
			$V_{CC}=4.5\text{V}$	3	-2	- ns
			$V_{CC}=6.0\text{V}$	3	-2	- ns
nCP maximum frequency	f_{max}	see Figure 6	$V_{CC}=2.0\text{V}$	4.8	23	- MHz
			$V_{CC}=4.5\text{V}$	24	69	- MHz
			$V_{CC}=5.0\text{V}; C_L=15\text{pF}$	-	76	- MHz
			$V_{CC}=6.0\text{V}$	28	82	- MHz
power dissipation capacitance	C_{PD}	$C_L=50\text{pF}; f=1\text{ MHz}; V_I = \text{GND to } V_{CC}^{[3]}$	-	24	-	pF

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL} .

[2] t_t is the same as t_{THL} and t_{TLH} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D = (C_{PD} \times V_{CC}^2 \times f_i \times N) + \sum (C_L \times V_{CC}^2 \times f_o)$ where: f_i =input frequency in MHz;

f_o =output frequency in MHz;

C_L =output load capacitance in pF; V_{CC} =supply voltage in V;

N =number of inputs switching; $\sum (C_L \times V_{CC}^2 \times f_o)$ =sum of outputs.

AC Characteristics 2

($T_{amb} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
nCP to nQ, nQ̄ propagation delay	t_{pd}	see Figure 6 ^[1]	$V_{CC}=2.0\text{V}$	-	-	265 ns
			$V_{CC}=4.5\text{V}$	-	-	53 ns
			$V_{CC}=6.0\text{V}$	-	-	45 ns
nSD̄ to nQ, nQ̄ propagation delay	t_{pd}	see Figure 7 ^[1]	$V_{CC}=2.0\text{V}$	-	-	300 ns
			$V_{CC}=4.5\text{V}$	-	-	60 ns
			$V_{CC}=6.0\text{V}$	-	-	51 ns
nRD̄ to nQ, nQ̄ propagation delay	t_{pd}	see Figure 7 ^[1]	$V_{CC}=2.0\text{V}$	-	-	300 ns
			$V_{CC}=4.5\text{V}$	-	-	60 ns
			$V_{CC}=6.0\text{V}$	-	-	51 ns
nQ, nQ̄ transition time	t_t	see Figure 6 ^[2]	$V_{CC}=2.0\text{V}$	-	-	110 ns
			$V_{CC}=4.5\text{V}$	-	-	22 ns
			$V_{CC}=6.0\text{V}$	-	-	19 ns
CP pulse width	t_w	see Figure 6	$V_{CC}=2.0\text{V}$	120	-	ns
			$V_{CC}=4.5\text{V}$	24	-	ns
			$V_{CC}=6.0\text{V}$	20	-	ns
nSD̄, nRD̄ pulse width	t_w	see Figure 7	$V_{CC}=2.0\text{V}$	120	-	ns
			$V_{CC}=4.5\text{V}$	24	-	ns
			$V_{CC}=6.0\text{V}$	20	-	ns
nSD̄, nRD̄ recovery time	t_{rec}	see Figure 7	$V_{CC}=2.0\text{V}$	45	-	ns
			$V_{CC}=4.5\text{V}$	9	-	ns
			$V_{CC}=6.0\text{V}$	8	-	ns
nD to nCP set-up time	t_{su}	see Figure 6	$V_{CC}=2.0\text{V}$	90	-	ns
			$V_{CC}=4.5\text{V}$	18	-	ns
			$V_{CC}=6.0\text{V}$	15	-	ns
nD to nCP hold time	t_h	see Figure 6	$V_{CC}=2.0\text{V}$	3	-	ns
			$V_{CC}=4.5\text{V}$	3	-	ns
			$V_{CC}=6.0\text{V}$	3	-	ns
nCP maximum frequency	f_{max}	see Figure 6	$V_{CC}=2.0\text{V}$	4.0	-	MHz
			$V_{CC}=4.5\text{V}$	20	-	MHz
			$V_{CC}=6.0\text{V}$	24	-	MHz

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL} .

[2] t_t is the same as t_{THL} and t_{TLH} .

Testing Circuit

AC Testing Circuit

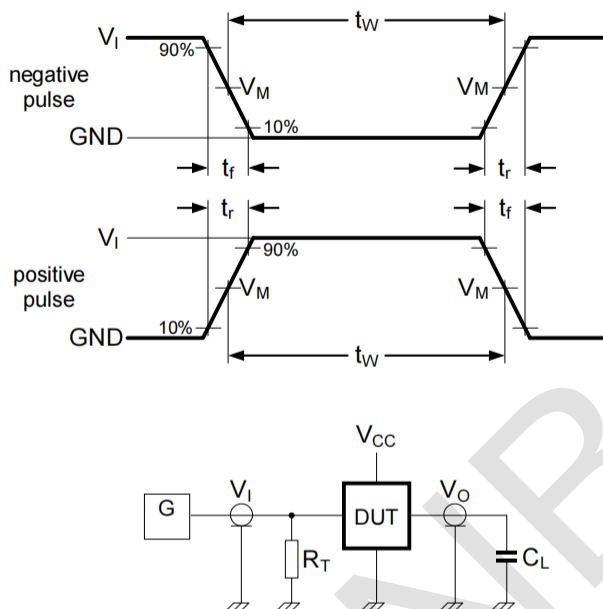


Figure 5. Test circuit for measuring switching times

Definitions for test circuit:

C_L =load capacitance including jig and probe capacitance.

R_T =termination resistance should be equal to the output impedance Z_o of the pulse generator.

AC Testing Waveforms

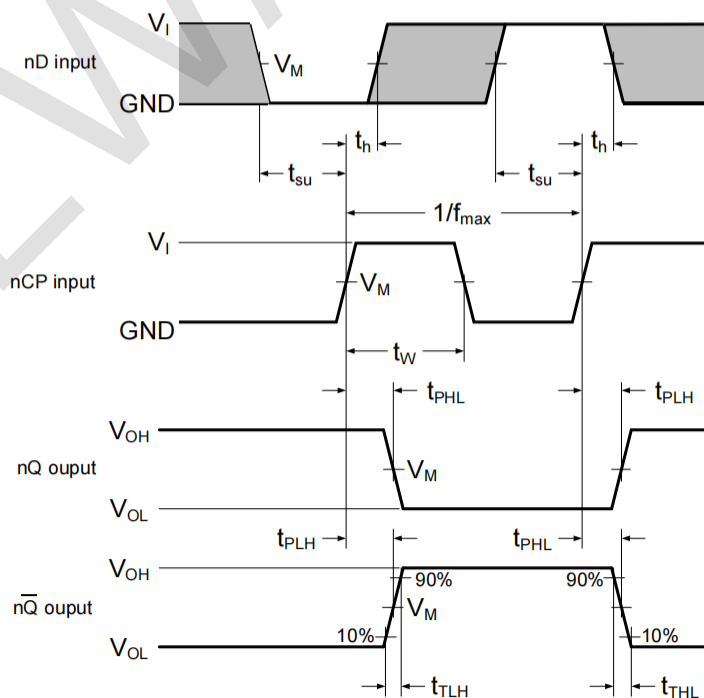


Figure 6. Input to output propagation delays

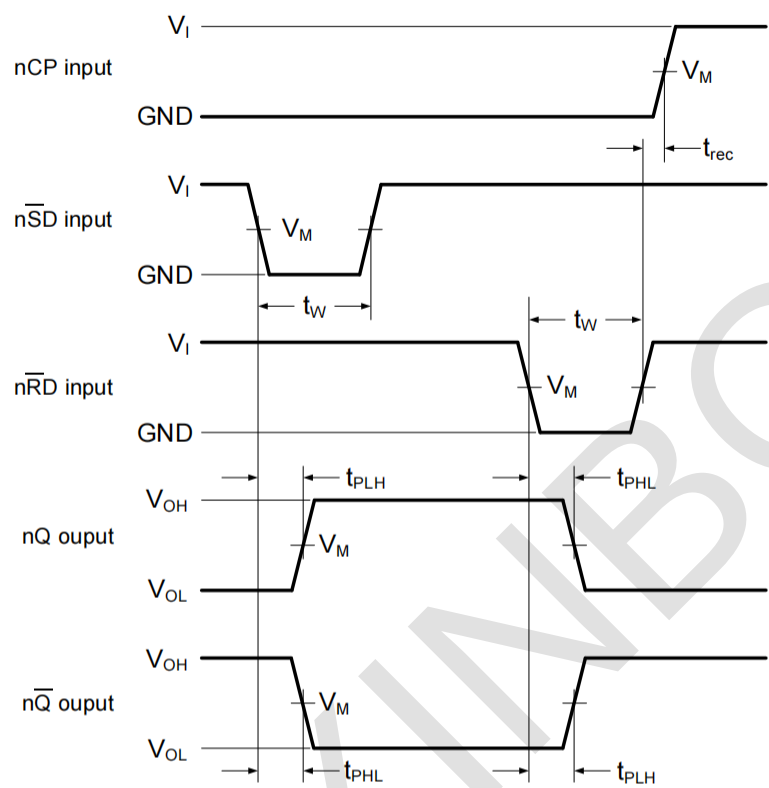


Figure 7. Set and reset propagation delays, pulse widths and recovery time

Measurement Points

Type	Input	Output
	V_M	V_M
SN74HC74	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$

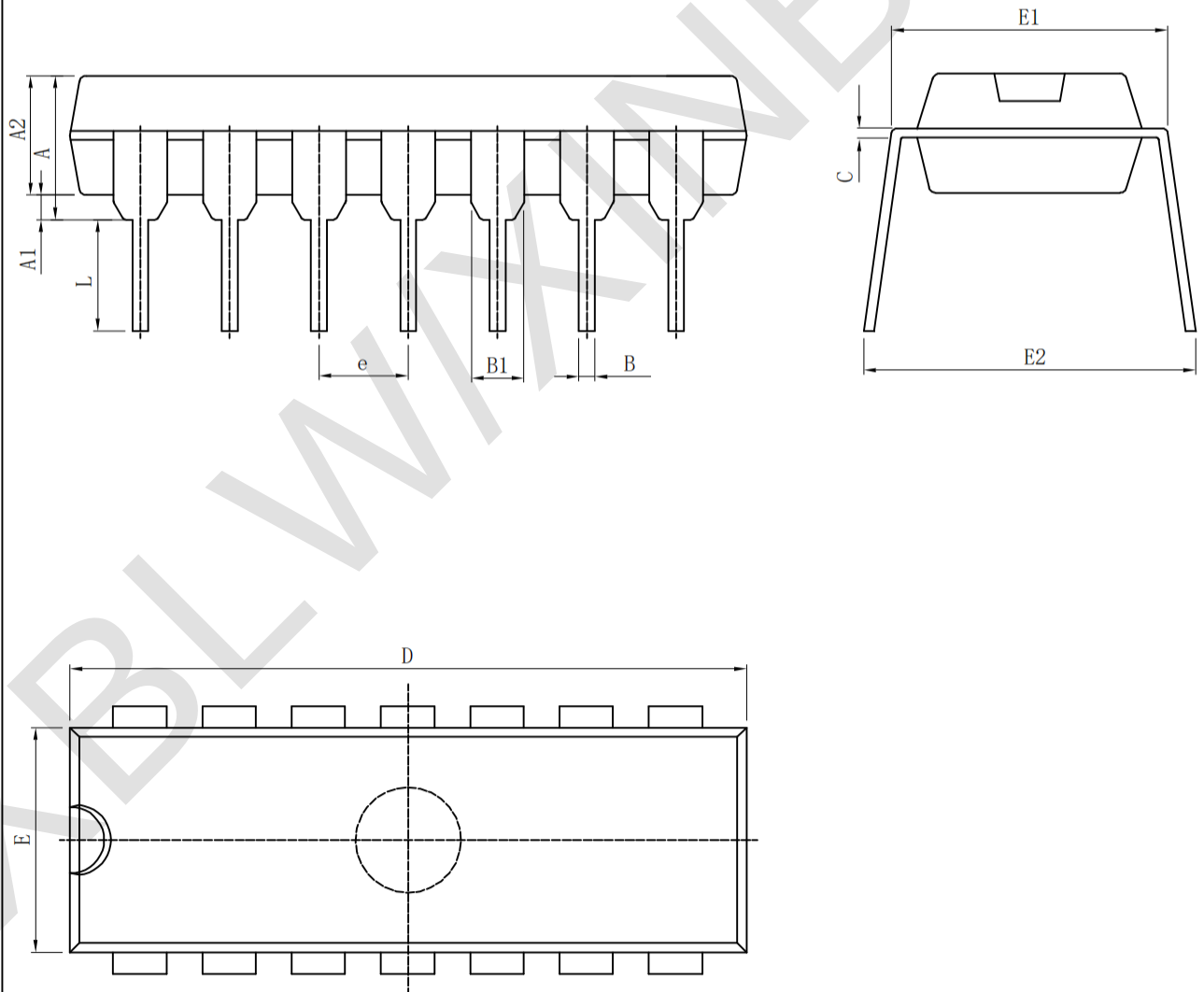
Test Data

Type	Input		Load		Test
	V_I	t_r, t_f	C_L	R_L	
SN74HC74	V_{CC}	6.0ns	15pF, 50pF	1k Ω	t_{PLH}, t_{PHL}

Package Information

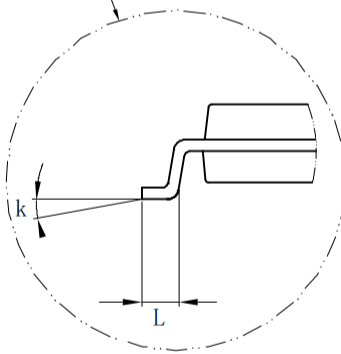
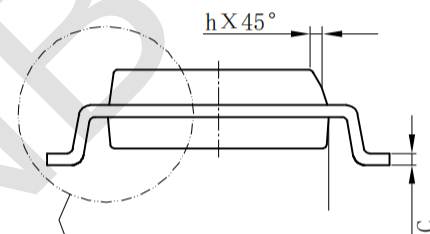
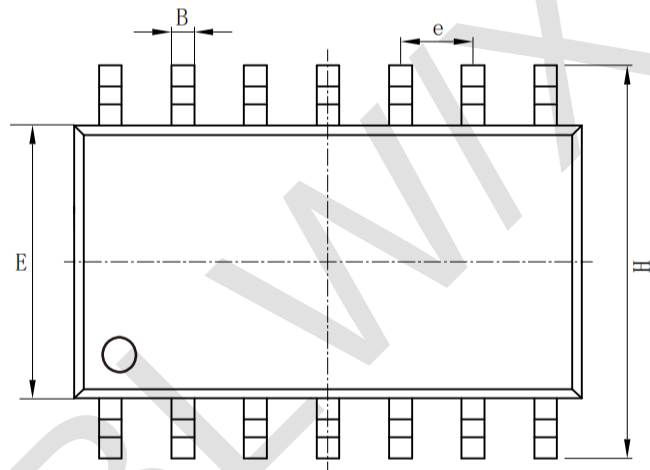
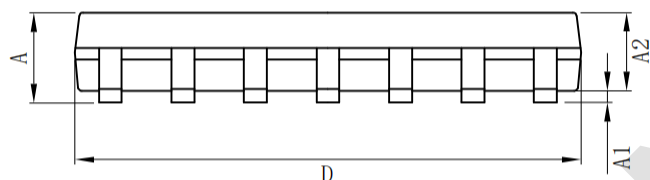
· DIP-14

Symbol	Size		Dimensions In Millimeters		Symbol	Size		Dimensions In Inches	
			Min (mm)	Max (mm)				Min (in)	Max (in)
A			3.710	4.310	A			0.146	0.170
A1			0.510		A1			0.020	
A2			3.200	3.600	A2			0.126	0.142
B			0.380	0.570	B			0.015	0.022
B1			1.524 (BSC)		B1			0.060 (BSC)	
C			0.204	0.360	C			0.008	0.014
D			18.800	19.200	D			0.740	0.756
E			6.200	6.600	E			0.244	0.260
E1			7.320	7.920	E1			0.288	0.312
e			2.540 (BSC)		e			0.100 (BSC)	
L			3.000	3.600	L			0.118	0.142
E2			8.400	9.000	E2			0.331	0.354



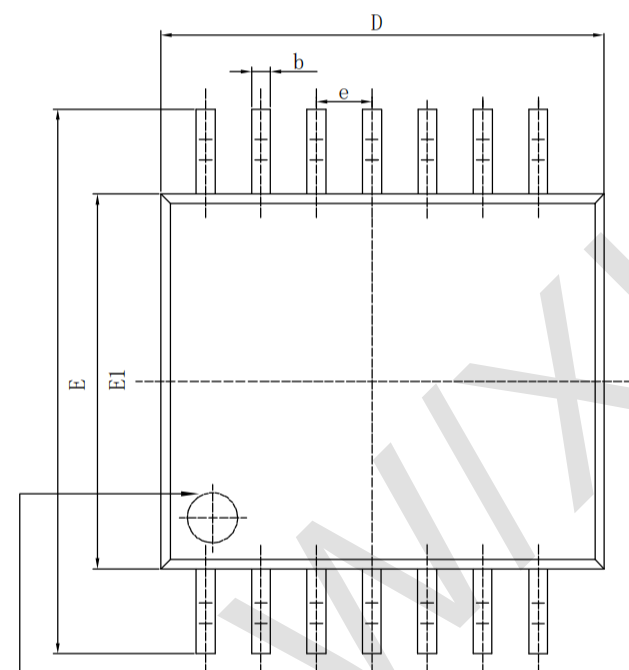
· SOP-14

Size Symbol	Dimensions In Millimeters		Size Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A	1.350	1.750	A	0.050	0.068
A1	0.100	0.250	A1	0.004	0.009
A2	1.100	1.650	A2	0.040	0.060
B	0.330	0.510	B	0.010	0.020
C	0.190	0.250	C	0.007	0.009
D	8.550	8.750	D	0.330	0.340
E	3.800	4.000	E	0.150	0.150
e	1.27		e	0.05	
H	5.800	6.200	H	0.220	0.240
h	0.250	0.500	h	0.009	0.020
L	0.400	1.270	L	0.015	0.050
k	8° (max)		k	8° (max)	

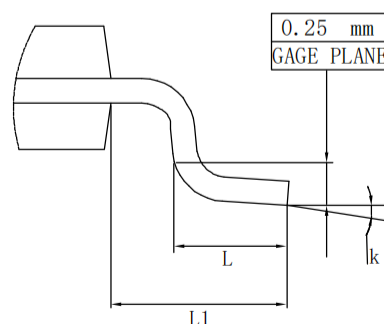
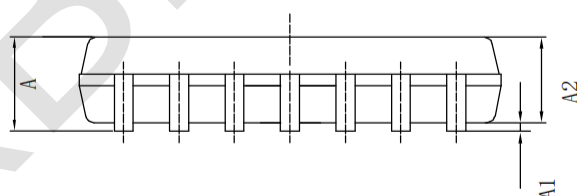
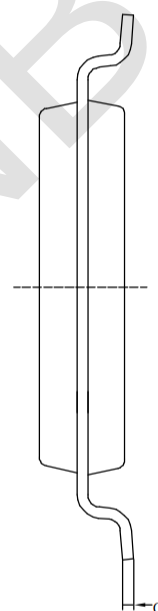


• TSSOP-14

Size Symbol	Dimensions In Millimeters		Size Symbol	Dimensions In Inches	
	Min (mm)	Max (mm)		Min (in)	Max (in)
A		1.200	A		0.047
A1	0.050	0.150	A1	0.002	0.006
A2	0.800	1.050	A2	0.031	0.041
b	0.190	0.300	b	0.007	0.012
c	0.090	0.200	c	0.004	0.0089
D	4.900	5.100	D	0.193	0.201
E	6.200	6.600	E	0.244	0.260
E1	4.300	4.500	E1	0.169	0.176
e	0.65		e	0.0256	
L	0.450	0.750	L	0.018	0.030
L1	1.00		L1	0.039	
k	0°	8°	k	0°	8°



PIN #1 IDENT.



Statement

- XBLW reserves the right to modify the product manual without prior notice! Before placing an order, customers need to confirm whether the obtained information is the latest version and verify the completeness of the relevant information.
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