Features

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

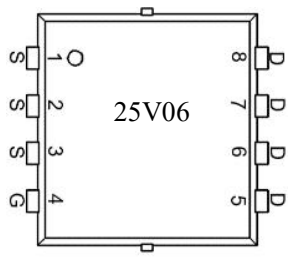
Bvdss	Rdson	ID
60V	11mΩ	25A

Application

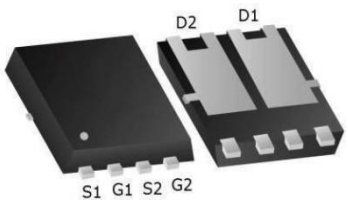
- DC-DC Converters
- Power management functions
- Synchronous-rectification applications

RoHS

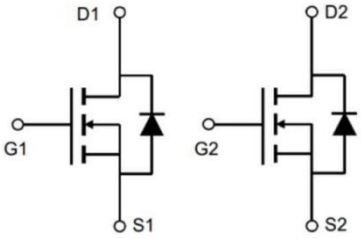
Package



Marking and pin assignment



PDFN3x3-8L top view



Schematic diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Quantity
25V06	S25V06D	PDFN3x3-8L	5000

Absolute Maximum Ratings (T_A=25℃unless otherwise specified)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C=25℃	I_D	25	A
	T_C=100℃		18	A
Pulsed Drain Current[1]		I_{DM}	136	A
Single Pulsed Avalanche Energy[2]		E_{AS}	33.8	mJ
Avalanche Current		I_{AS}	-	A
Power Dissipation		P_D@T_C=25℃	27	W
Operating Junction Temperature Range		T_J	-55 ~ +150	℃
Storage Temperature Range		T_{STG}	-55 ~ +150	℃

Thermal Resistance Ratings

Parameter	Symbol	Typ.	Max.	Unit
Thermal Resistance,Junction-to-Case	$R_{\theta JC}$	--	4.6	℃/W
Thermal Resistance,Junction-to-Ambient[3]	$R_{\theta JA}$	--	55	℃/W

Ordering Information

Ordering Number	Package	Pin Assignment						Packing
Halogen Free		G1	G2	D1	D2	S1	S2	
HLS25V06D	PDFN3x3-8L	2	4	7,8	5,6	1	3	Tape Reel

Electrical Characteristics (T_J=25℃,unless otherwise specified)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{DSS}	V_{GS}=0V,I_D=250μA	60	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=65V,V_{GS}=0V,T_J=25℃	-	-	1	μA
		V_{DS}=65V,V_{GS}=0V,T_J=100℃	-	-	100	μA
Gate to Body Leakage Current	I_{GSS}	V_{DS}=0V, V_{GS}=±20V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1.2	1.7	2.2	V
Static Drain-Source On-Resistance[4]	$R_{DS(on)}$	V_{GS}=10V, I_D=20A	-	11	14	mΩ
		V_{GS}=4.5V, I_D=10A	-	14	19	
Forward Transconductance[4]	gfs	V_{DS}=10V,I_D=20A	-	42	-	S
Gate Resistance	R_G	f=1MHz	-	1.2	-	Ω
Input Capacitance	C_{iss}	V_{DS}=30V,V_{GS}=0V, f=1MHz	-	738	-	pF
Output Capacitance	C_{oss}		-	225	-	
Reverse Transfer Capacitance	C_{rss}		-	13.5	-	
Total Gate Charge	Q_g	V_{DS}=30V,V_{GS}=10V, I_D=20A	-	14	-	nC
Gate-Source Charge	Q_{gs}		-	2.6	-	
Gate-Drain Charge	Q_{gd}		-	2.9	-	
Turn-on Delay Time	$T_{d(on)}$	V_{GS}=10V,V_{DD}=30V, R_G=3Ω,I_D=20A	-	5.7	-	nS
Turn-on Rise Time	t_r		-	5.1	-	
Turn-Off Delay Time	$T_{d(off)}$		-	14.8	-	
Turn-Off Fall Time	T_f		-	4.6	-	
Body Diode Reverse Recovery Time	t_{rr}	I_F=20A,dI/dt=100A/us	-	24	-	nC
Body Diode Reverse Recovery Charge	Q_{rr}		-	9.6	-	
Maximum Continuous Drain to Source Diode Forward Current	I_S	T_C=25℃	-	-	25	A
Diode Forward Voltage[4]	V_{SD}	V_{GS}=0V,I_S=20A	-	-	1.2	V

Notes:

1. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150℃.

2. The test condition is V_{DD}= 25V, V_{GS}= 10V, L= 0.4mH, I_{AS}= 13A.

3. The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%.
5. This value is guaranteed by design hence it is not included in the production test.

Typical Characteristics

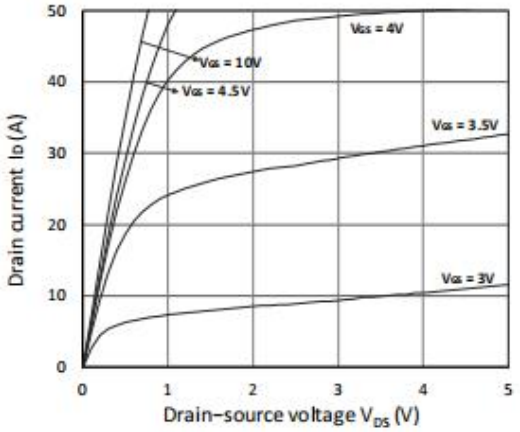


Figure 1. Output Characteristics

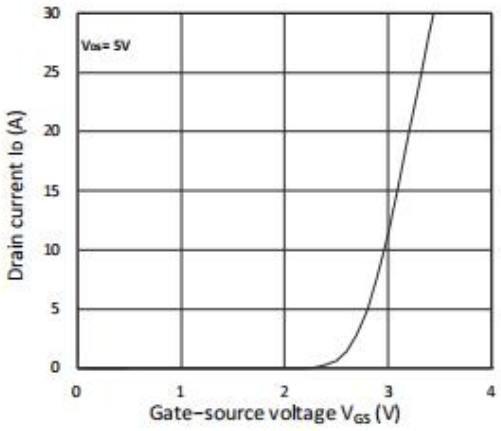


Figure 2. Transfer Characteristics

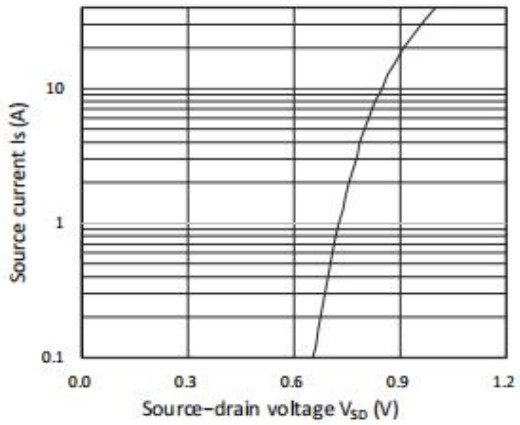


Figure 3. Forward Characteristics of Reverse

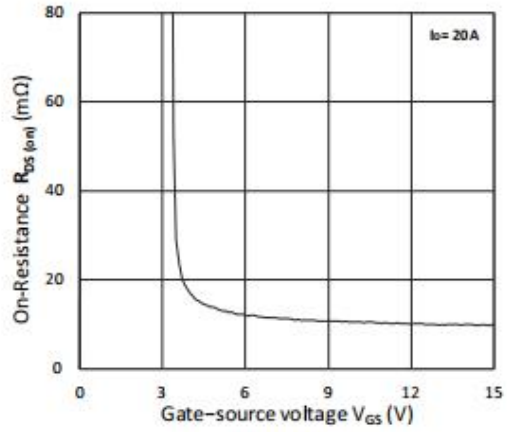


Figure 4. $R_{DS(ON)}$ vs. V_{GS}

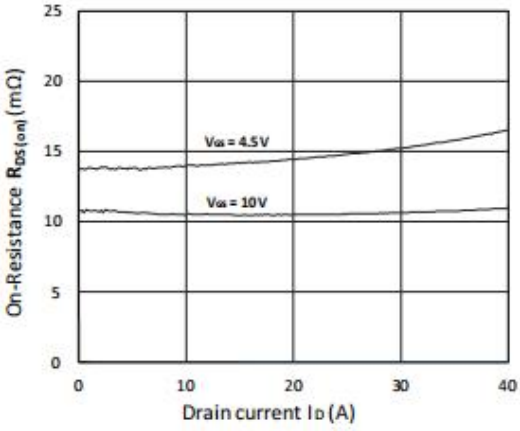


Figure 5. $R_{DS(ON)}$ vs. I_D

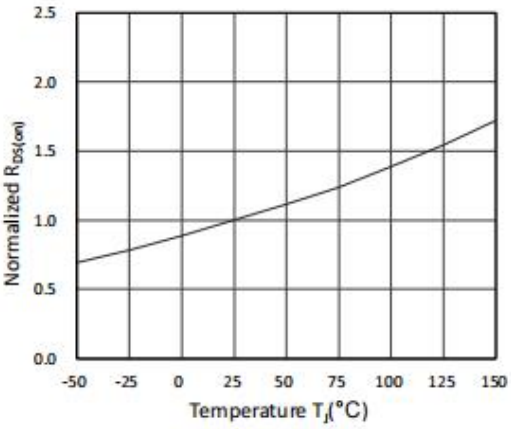


Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

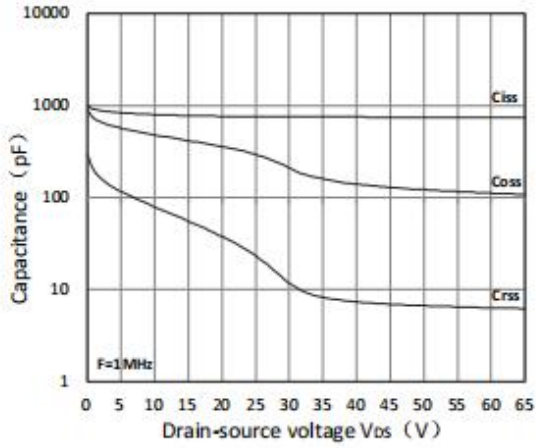


Figure 7. Capacitance Characteristics

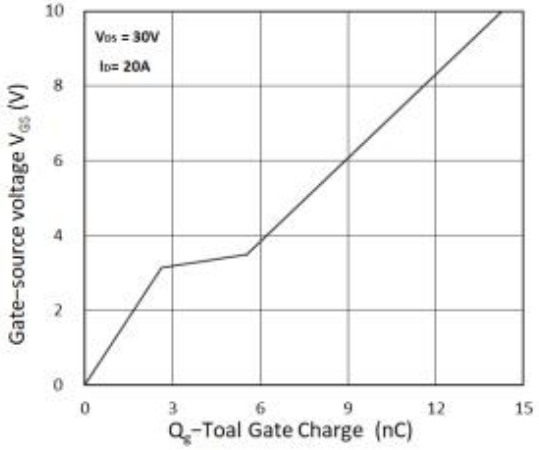


Figure 8. Gate Charge Characteristics

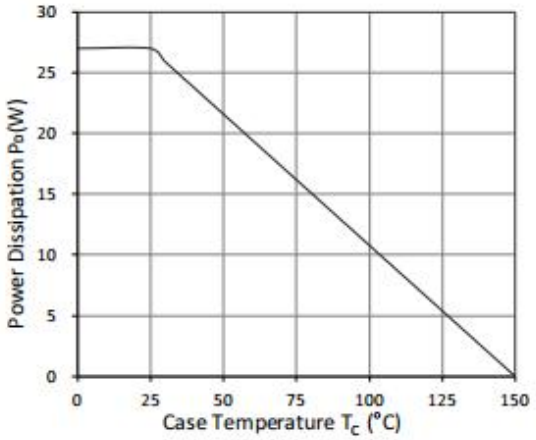


Figure 9. Power Dissipation

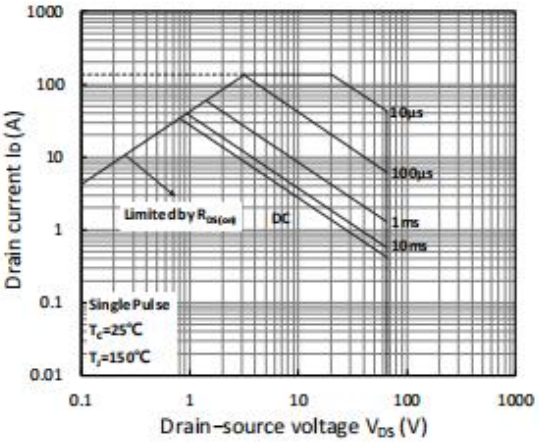


Figure10. Safe Operating Area

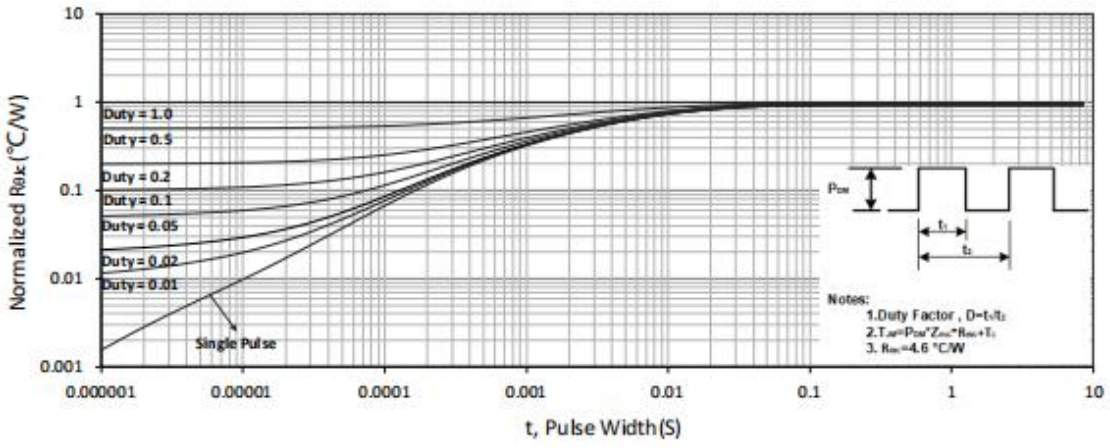
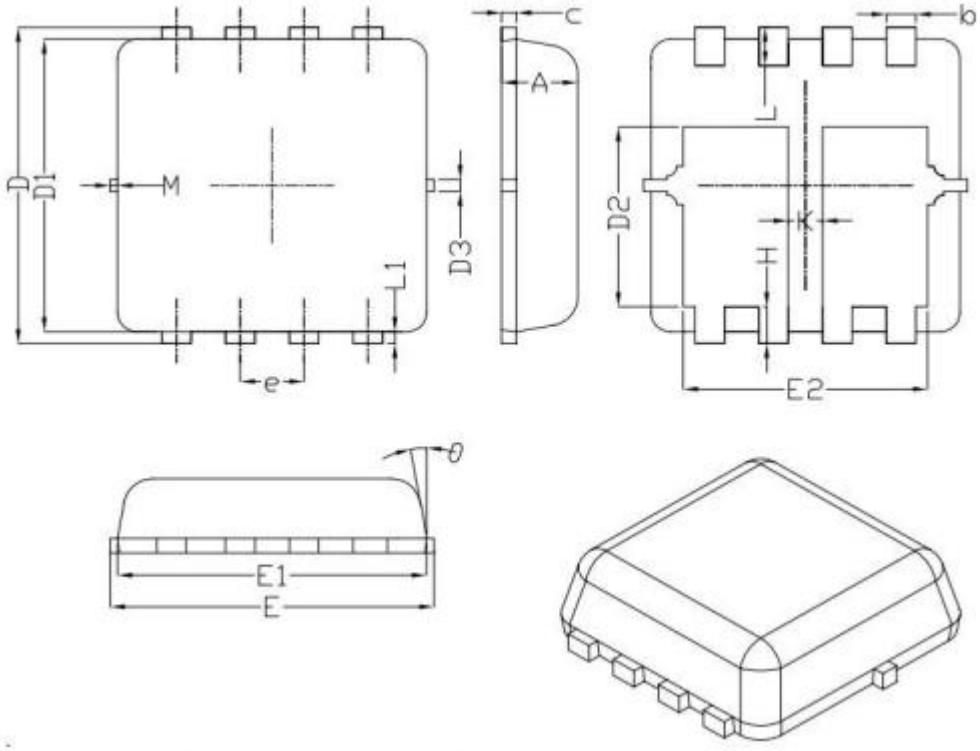


Figure 11. Normalized Maximum Transient Thermal Impedance

Package Dimensions PDFN3x3-8L



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.78	1.88	1.98
D3	--	0.13	–
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65 BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	--	0.13	–
K	0.30	–	–
θ	--	10°	12°
M	*	*	0.15
* Not Specified			

Notes:
1. Refer to JEDEC MO-240 variation CA.
2. Dimensions "D1" and "E1" do NOT include mold flash protrusions or gate burrs.
3. Dimensions "D1" and "E1" include interterminal flash or protrusion.

Important Notice and Disclaimer

HL Microelectronics reserves the right to make changes to this document and its products and specifications at any time without notice.
Customers should obtain and confirm the latest product information and specifications before final design, purchase or use.

HL Microelectronics makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, not does HL Microelectronics assume any liability for application assistance or customer product design.

HL Microelectronics does not warrant or accept any liability with products which are purchased or used for any unintended or unauthorized application.

No license is granted by implication or otherwise under any intellectual property rights of HL Microelectronics.

HL Microelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of HL Microelectronics.