Sine Wave PWM Drive, Pre Driver IC

Bi-CMOS IC for Brushless Motor Drive

LV8133JA

ON Semiconductor®

Overview

The LV8133JA is a PWM system pre driver IC designed for three-phase brushless motors.

This IC reduces motor driving noise by using a high-efficiency, quiet PWM drive (150-degree drive system).

It incorporates a full complement of protection circuits, and is capable of reducing the number of components used and achieving a high level of reliability. This IC is ideally suited for driving various large-sized motors such as those used in ventilators, air purifiers and other such products.

Features

- Three-phase Bipolar Drive
- Quiet PWM Drive (150-degree Current-Carrying)
- Drive Phase Setting Function (Set in 16 Steps from 0 to 28 degrees)
- Supports Motor Stop Mode (When the SS Pin is Set to the Low Level, the Motor Stop Mode is Turned On, HB Pin Turned Off)
- Supports Bootstrap (Maximum Duty Ratio is Limited)
- Automatic Recovery Type Constraint Protection Circuit (Constraint Protection Detection Signal Output LDA Pin Provided)
- Forward/Reverse Switching Circuit, Hall Bias Pin
- Current Limiter Circuit, Low-voltage Protection Circuit, and Thermal Shutdown Protection Circuit
- FG1 Output (360-degree Electrical Angle/1 Pulse)
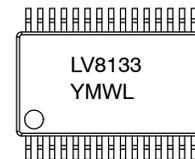- This is a Pb−Free Device
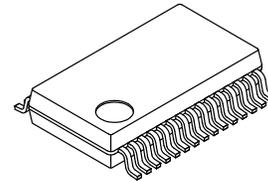
SSOP30 (225 mil)
CASE 565AZ

MARKING DIAGRAM

LV8133
YMWL

LV8133 = Specific Device Code
Y = Year of Production, Last Number
M = Assembly Operation Month
WL = Wafer Lot Number

*Pb−Free indicator, "G" or microdot " ▪ ", may or may not be present.

ORDERING INFORMATION

Device	Package	Shipping[†]
LV8133JA−AH	SSOP30 (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Specifications

Table 1. MAXIMUM RATINGS at Ta = 25°C (Note 1)

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	V_{CC} max	V_{CC} pin	18	V
Output Current	I_O max		15	mA
Allowable Power Dissipation	Pd max1	Independent IC	0.35	W
	Pd max2	Mounted on a specified circuit board. (Note 2)	0.95	W
FG Pin Applied Voltage	V_{FG} max		18	V
LDA Pin Applied Voltage	V_{LDA} max		18	V
Junction Temperature	T_j max		150	°C
Operating Temperature	T_{opr}		−40 to +105	°C
Storage Temperature	Tstg		−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for further details.
2. Specified circuit board: 114.3 mm × 76.1 mm × 1.6 mm, glass epoxy.

Table 2. RECOMMENDED OPERATING RANGES at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage Range	V_{CC}		8.5 to 16.5	V
5 V Constant Voltage Output Current	I_{REG}		0 to −10	mA
HB Pin Output Current	I_{HB}		0 to −30	mA
CTL Pin Applied Voltage	V_{CTL}		0 to VREG	V
FG Pin Applied Voltage	V_{FG}		0 to V_{CC}	V
FG Pin Output Current	I_{FG}		0 to 10	mA
LDA Pin Applied Voltage	V_{LDA}		0 to V_{CC}	V
LDA Pin Output Current	I_{LDA}		0 to 10	mA

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 3. ELECTRICAL CHARACTERISTICS at Ta = 25°C, V_{CC} = 15 V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Current	I_{CC}			4.5	7.0	mA
Output Block (Pin HIN1, HIN2, HIN3, LIN1, LIN2 and LIN3)						
High Level Output Voltage	V_{HO}	I_O = −10 mA	VREG-0.40	VREG-0.25		V
Upper Output ON Resistance	R_{ON} (H1)	I_O = −10 mA		25	40	Ω
Low Level Output Voltage	V_{LO}	I_O = 10 mA		0.15	0.30	V
Lower Output ON Resistance	R_{ON} (L1)	I_O = 10 mA		15	30	Ω
Output Leakage Current	$I_O$leak				10	μA
Maximum Duty Ratio Limit OFF Time	Toff	VCTL = 5 V	5	7	9	μs
5 V Constant Voltage Output (VREG5 pin)						
Output Voltage	VREG	I_O = −5 mA	4.7	5.0	5.3	V
Voltage Fluctuation	ΔV (REG1)	V_{CC} = 9.5 to 16.5 V, I_O = −5 mA			100	mV
Load Fluctuation	ΔV (REG2)	I_O = −5 to −10 mA			100	mV
Hall Amplifier (Pin IN1+, IN1−, IN2+, IN2−, IN3+ and IN3−)						
Input Bias Current	IB (HA)		−2		0	μA

Table 3. ELECTRICAL CHARACTERISTICS at Ta = 25°C, V_{CC} = 15 V (continued)

Parameter	Symbol	Conditions	Ratings			Unit
			Min	Typ	Max	
Common-mode Input Voltage Range 1	VICM1	When a Hall element is used	0.3		VREG-1.7	V
Common-mode Input Voltage Range 2	VICM2	Single-sided input bias mode (when a Hall IC is used)	0		VREG	V
Hall Input Sensitivity	VHIN	Sine wave	120			mVp-p
Hysteresis Width	ΔV_{IN} (HA)		±10	±25	±40	mV
Input Voltage Low → High	VSLH		-5	0	+5	mV
Input Voltage High → Low	VSHL		-5	0	+5	mV
CSD Oscillator Circuit						
High Level Output Voltage	V_{OH} (CSD)		2.75	2.95	3.15	V
Low Level Output Voltage	V_{OL} (CSD)		0.85	1.05	1.25	V
Amplitude	V (CSD)		1.7	1.9	2.1	Vp-p
External Capacitor Charging Current	ICHG1 (CSD)	VCHG1 = 2.0 V	−14	−10	−6	μA
External Capacitor Discharging Current	ICHG2 (CSD)	VCHG2 = 2.0 V	6	10	14	μA
PWM Oscillator (CPWM pin)						
High Level Output Voltage	V_{OH} (PWM)		3.3	3.5	3.7	V
Low Level Output Voltage	V_{OL} (PWM)		1.35	1.5	1.65	V
Amplitude	V (PWM)		1.8	2.0	2.2	Vp-p
Oscillation Frequency	f (PWM)	C = 2200 pF, R = 15 kΩ (design target value)		17.3		kHz
Current Limiter Operation (RF pin)						
Limiter Voltage	VRF		0.225	0.25	0.275	V
Thermal Shutdown Protection Operation						
Thermal Shutdown Protection Operating Temperature	TSD	* Design target value (junction temperature)	150	175		°C
Hysteresis Width	ΔTSD	* Design target value (junction temperature)		35		°C
HB pin						
High Output Voltage	V_{HO} (HB)	IHB = −10 mA	V_{CC}-0.2	V_{CC}-0.1		V
Output ON Resistance	R_{ON} (HB)	IHB = −10 mA		10	20	Ω
Output Leakage Current	I_L (HB)	Stop mode V_{CC} = 15 V			10	μA
Low Voltage Protection Circuit (detecting VREG5 voltage)						
Operation Voltage (VREG5 Voltage)	VSD		3.1	3.6	4.1	V
Hysteresis Width	ΔVSD		0.2	0.4	0.6	V
FG1 LDA Pin						
Output ON Resistance	$R_{ON}L$ (FG) $R_{ON}L$ (LDA)	IFG/ILDA = 5 mA		40	60	Ω
Output Leakage Current	I_L (FG) I_L (LDA)	VFG/VLDA = 18 V			10	μA
CTL Amplifier (Drive Mode)						
Input Voltage Range	V_{IN} (CTL)		0		VREG	V
High Level Input Voltage	V_{IH} (CTL)	Amplitude modulated signal 100%	3.3	3.5	3.7	V
Middle Level Input Voltage	V_{IM} (CTLI)	Amplitude modulated signal 0%	1.35	1.5	1.65	V
F/R Pin						
High Level Input Voltage Range	V_{IH} (FR)		2.5		VREG	V
Low Level Input Voltage Range	V_{IL} (FR)		0		0.7	V

Table 3. ELECTRICAL CHARACTERISTICS at Ta = 25°C, V_{CC} = 15 V (continued)

Parameter	Symbol	Conditions	Ratings			Unit
			Min	Typ	Max	
Input Open Voltage	V$_{IO}$ (FR)			0	0.3	V
Hysteresis Width	V$_{IS}$ (FR)		0.15	0.30	0.45	V
High Level Input Current	I$_{IH}$ (FR)	VF/R = VREG	25	45	65	μA
Low Level Input Current	I$_{IL}$ (FR)	VF/R = 0 V	−2	0	+2	μA
SS Pin						
Drive Start Voltage	VON		2.9		VREG	V
Drive Stop Voltage	VOFF		0		0.8	V
ADP1 Pin (Drive Phase Adjustment)						
Minimum Lead Angle	Vadp01	VADP1 = 0 V		0	2	Deg
Maximum Lead Angle	Vadp16	VADP1 = VREG	26	28		Deg
Current Ratio with the ADP1/ADP2 Pin Current	IADPR	VCTL = 2.5 V, IADP1/IADP2	1.8	2	2.2	A/A
ADP2 Pin (Drive Phase Adjustment)						
High Level Output Voltage	VADP2H	VCTL = VREG	(VREG/2) −0.2	(VREG/2)	(VREG/2) +0.2	V
Low Level Output Voltage	VADP2L	VCTL = 0 V	0		0.3	V
DPL Pin (Drive Phase Adjustment)						
Lead Angle Limit High Level Voltage	VDPLH		3.3	3.5	3.7	V
Lead Angle Limit Low Level Voltage	VDPLL		1.35	1.5	1.65	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
*These are design target values and no measurements are made.
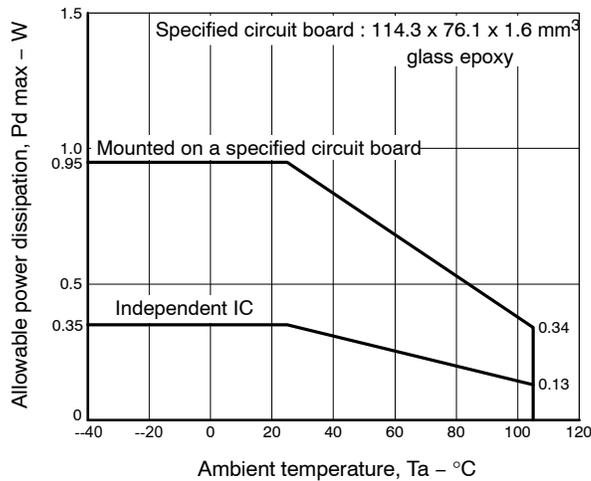
Figure 1. Pd max – Ta

LV8133JA

Sample Application Circuit 1 (Hall Element)
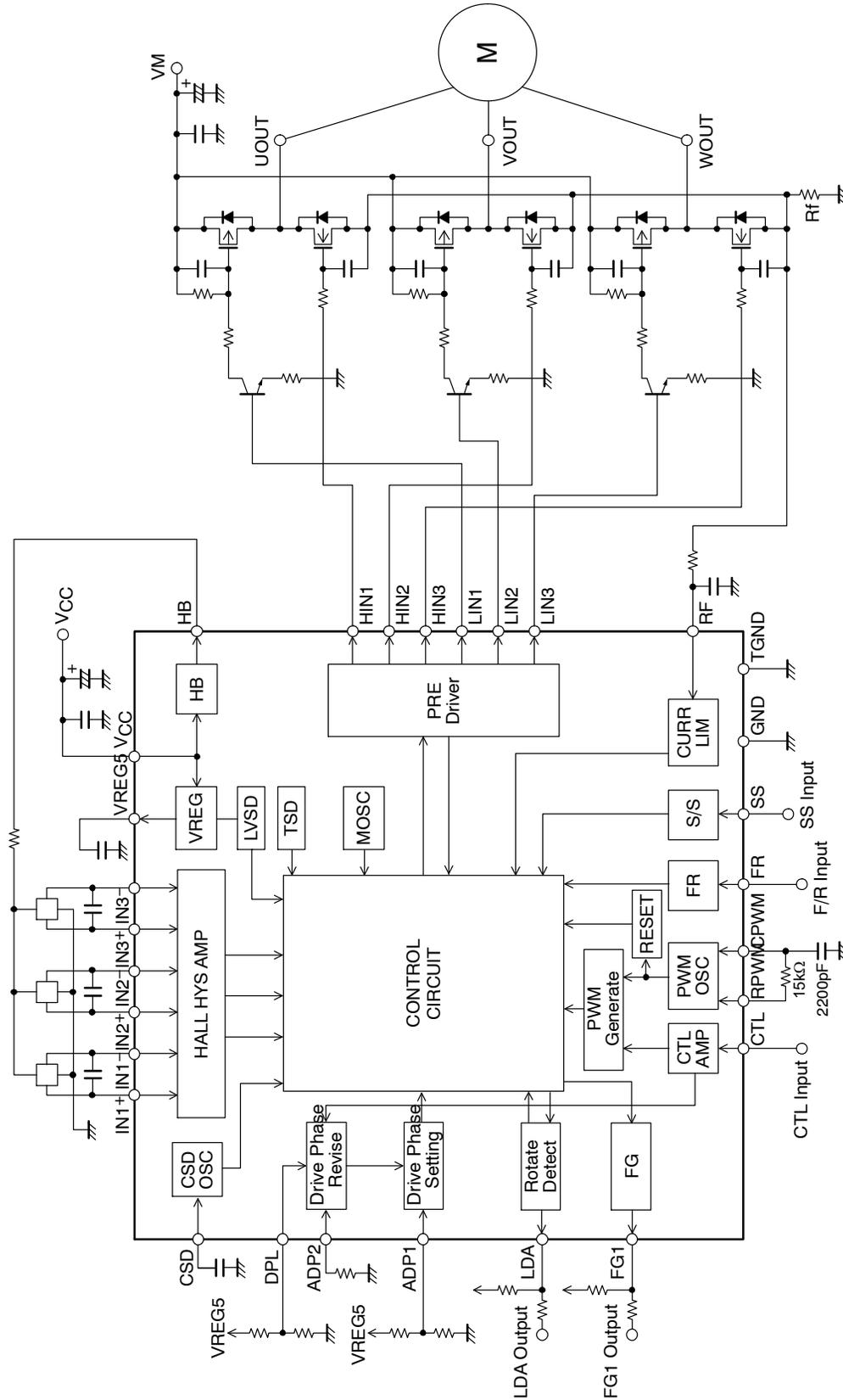
Figure 2. Application Circuit 1 (Hall Element)
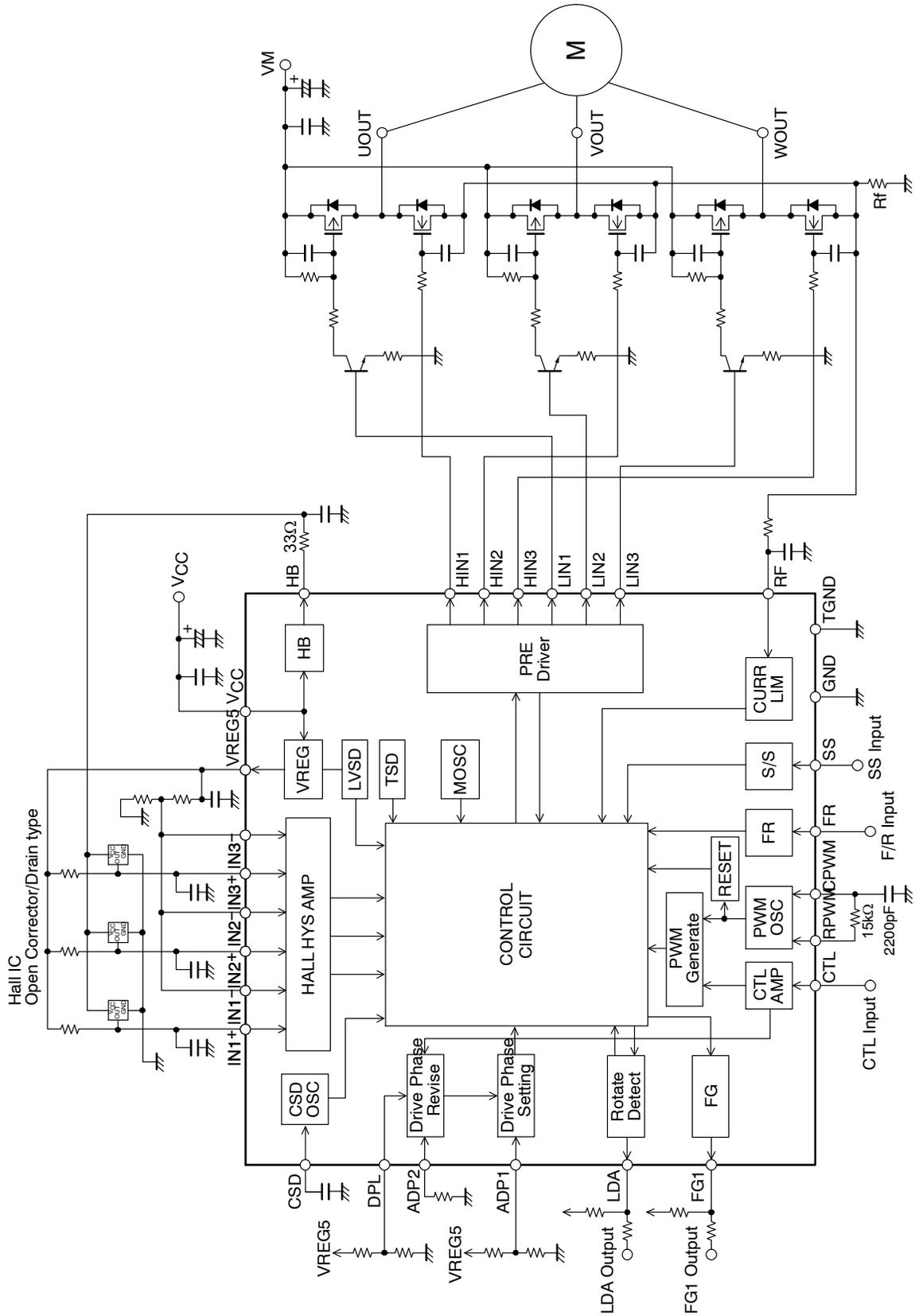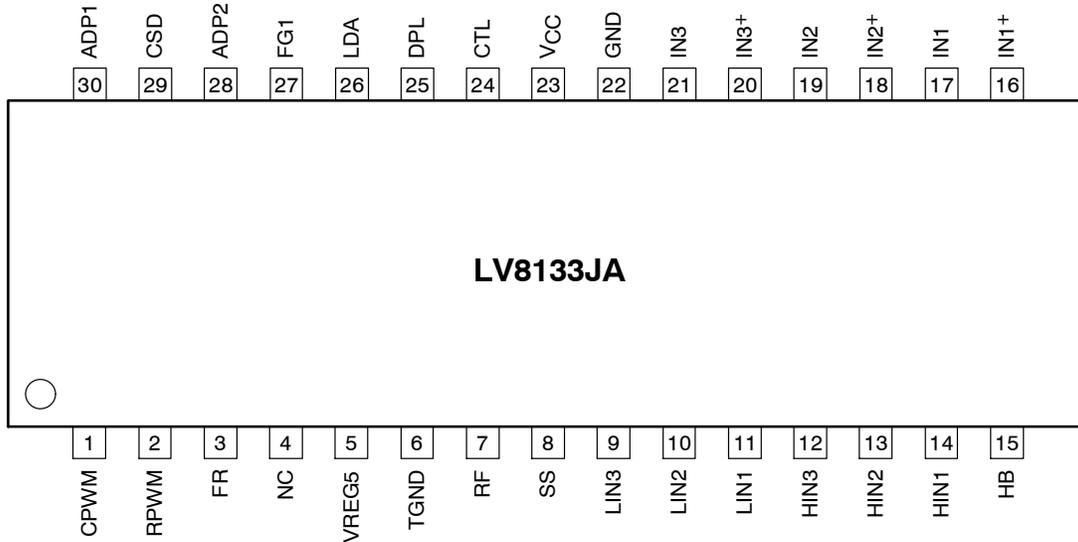
Sample Application Circuit 2 (Hall IC)

Figure 3. Application Circuit 2 (Hall IC)

Pin Assignment

Top View

Figure 4. Pin Assignment

Table 4. PIN FUNCTIONS

Pin No.	Pin Name	Pin Function	Equivalent Circuit
1	CPWM	Triangle wave oscillation pin for PWM generation. Insert a capacitor between this pin and ground and a resistor between this pin and RPWM for triangle wave oscillation.	
2	RPWM	Oscillation pin for PWM generation. Insert a resistor between this pin and CPWM.	

Table 4. PIN FUNCTIONS (continued)

Pin No.	Pin Name	Pin Function	Equivalent Circuit
3	FR	FR Forward/reverse rotation setting pin. A low-level specifies forward rotation and a high-level specifies reverse rotation. This pin is held low when open.	
6	TGND	TGND Test pin. Connect this pin to ground.	
4	NC		
5	VREG5	5 V regulator output pin (control circuit power supply). Insert a capacitor between this pin and ground for power stabilization. 0.1 μF or so is desirable.	
7	RF	Output current detection pin. This pin is used to detect the voltage across the current detection resistor (Rf). The maximum output current is determined by the equation $I_{OUT} = 0.25$ V/Rf.	
8	SS	Start/stop pin. When the SS pin is set to the high level, S/S switching circuit enters the start mode. Inversely, when the SS pin is set to the low level, S/S switching circuit enters the stop mode. In the stop mode, the drive output and HB pin are OFF, and the FG signal is output. This pin cannot be used in the open state.	

Table 4. PIN FUNCTIONS (continued)

Pin No.	Pin Name	Pin Function	Equivalent Circuit
9 10 11	LIN3 LIN2 LIN1	LIN1, LIN2, and LIN3 : L-side output pins. Generate 0 to VREG5 push-pull outputs.	VREG 10 12 14 9 11 13 500Ω
12 13 14	HIN3 HIN2 HIN1	HIN1, HIN2, and HIN3 : H-side output pins. Generate 0 to VREG5 push-pull outputs.	
15	HB	Hall bias power supply pin. This pin is set to the high impedance state when in the stop mode. By supplying the Hall bias power from this pin, the power that is consumed by the Hall bias in the stop mode can be reduced to zero.	V_{CC} 15
16 17 18 19 20 21	$IN1^+$ $IN1^-$ $IN2^+$ $IN2^-$ $IN3^+$ $IN3^-$	Hall signal input pins. The high state is when IN^+ is greater than IN^-, and the low state is the reverse. An amplitude of at least 120 mVp-p (differential) is desirable for the Hall signal inputs. If noise on the Hall signals is a problem, insert capacitors between IN^+ and IN^- pins. If input is provided from a Hall IC, the common-mode input range can be expanded by biasing either + or −.	VREG 16 18 20 500Ω 500Ω 17 19 21
22	GND	Ground pin of the control circuit block.	
23	V_{CC}	Power supply pin for control. Insert a capacitor between this pin and ground to prevent the influence of noise, etc.	
24	CTL	Control input pin. When CTL pin voltage rises, the IC changes the output signal PWM duty to increase the torque output.	VREG V_{CC} 5kΩ 24

Table 4. PIN FUNCTIONS (continued)

Pin No.	Pin Name	Pin Function	Equivalent Circuit
25	DPL	Setting pin for drive phase adjustment limit. This pin is used to limit the lead angle of the drive phase. The lead angle is limited to zero degrees when the voltage is 1.5 V or lower and the limit is released when the voltage is 3.5 V or higher.	
26 27	LDA FG1	LDA: Constraint protection detection output pin. A low level is output during normal rotation and a high level is output in the constraint protection state. FG1: 1-Hall FG signal output pin. 8-pole motor outputs 4 pulses per one rotation.	
28	ADP2	Setting pin for phase drive correction. This pin sets the amount of correction made to the lead angle according to the CTL input. Insert a resistor between this pin and ground to adjust the amount of correction.	

Table 4. PIN FUNCTIONS (continued)

Pin No.	Pin Name	Pin Function	Equivalent Circuit
29	CSD	Pin to set the operating time of the motor constraint protection circuit. Insert a capacitor between this pin and ground. This pin must be connected to ground if the constraint protection circuit is not used.	
30	ADP1	Drive phase adjustment pin. The drive phase can be advanced from 0 to 28 degrees during 150-degree current carrying drive. The lead angle becomes 0 degrees when 0 V is input and 28 degrees when VREG is input.	

LV8133JA

Timing Chart (IN = "H" indicates the state in which IN+ is greater than IN−.)

(1) F/R pin = L
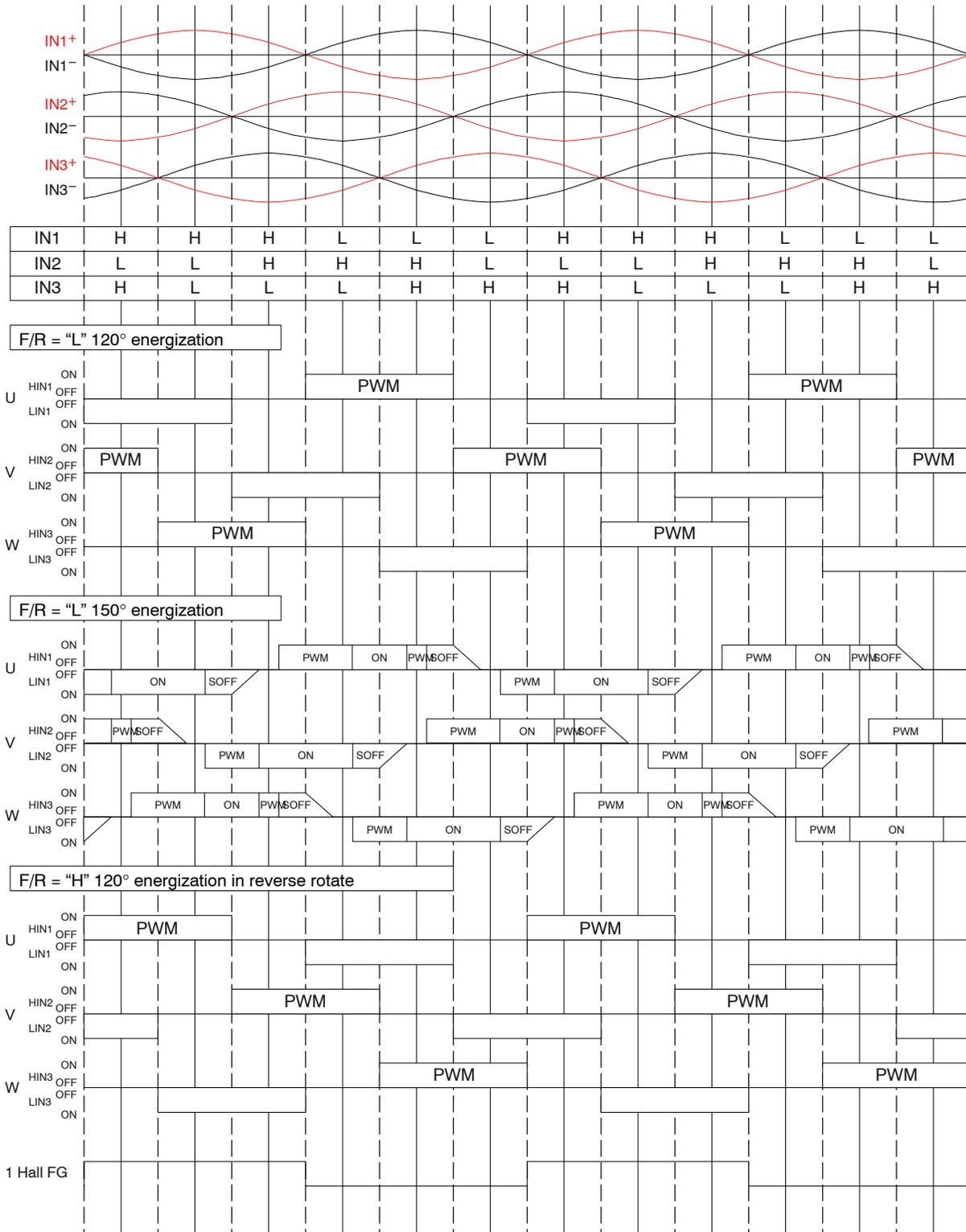
	IN1	H	H	H	L	L	L	H	H	H	L	L	L
IN2	L	L	H	H	H	L	L	L	H	H	H	L
IN3	H	L	L	L	H	H	H	L	L	L	H	H

The energization is switched to 120° where 1 Hall FG frequency is 3.6 Hz (typ) or lower
A direction of rotation is detected from Hall signal according to F/R pin input
If the motor rotates in reverse against F/R pin input 120° energization is maintained forcibly

(2) F/R pin = H
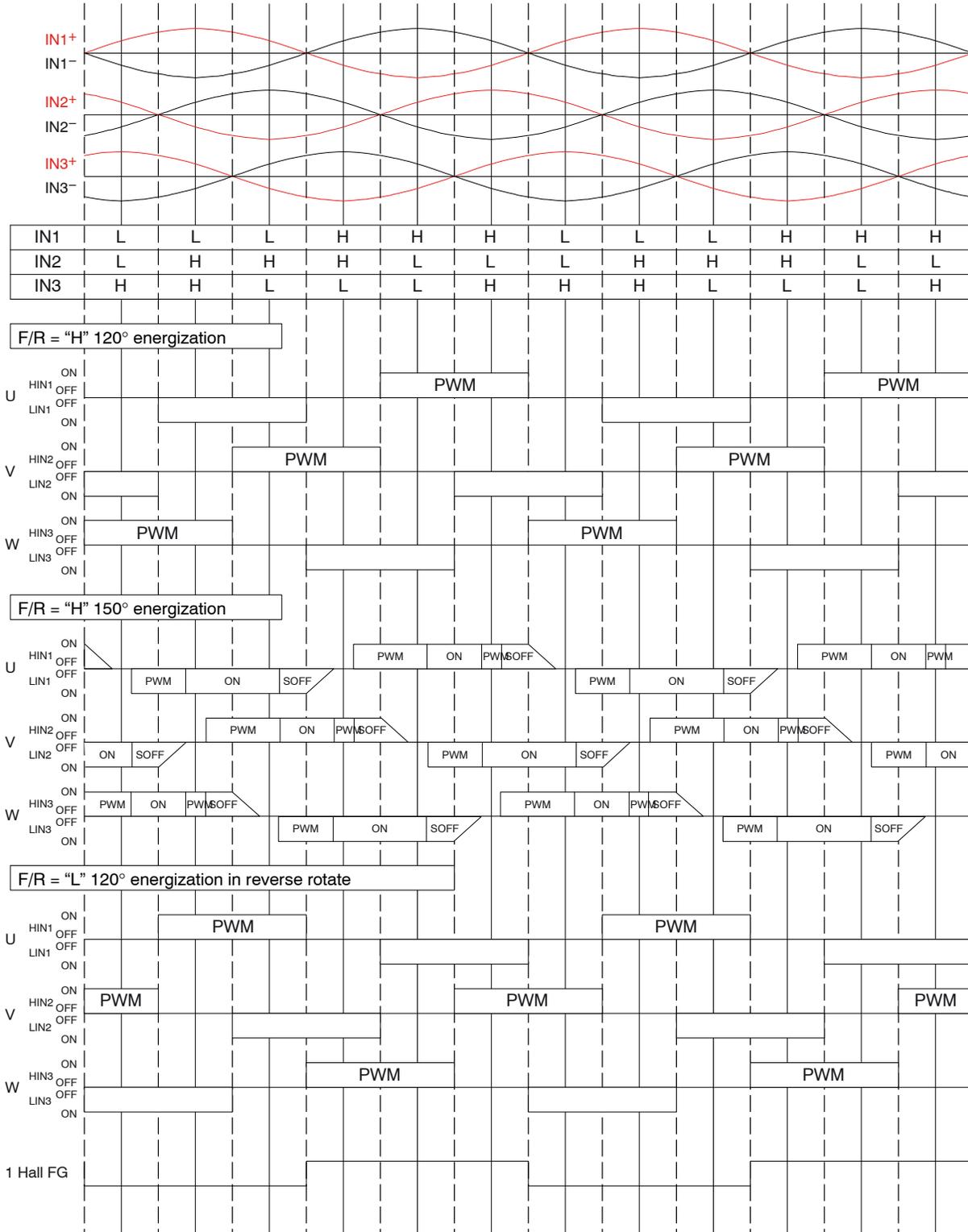
The energization is switched to 120° where 1 Hall FG frequency is 3.6 Hz (typ) or lower
A direction of rotation is detected from Hall signal according to F/R pin input
If the motor rotates in reverse against F/R pin input 120° energization is maintained forcibly

Functional Description

- Basic operation of 120-degree ⇔ 150-degree current-carrying switching

At startup, this IC starts at 120-degree current-carrying. The rotation direction is detected using the Hall signal in accordance with the F/R pin input, and if the motor is rotating in the reverse direction with respect to the F/R pin input, the 120-degree current-carrying is forcibly continued. If the motor is rotating in the forward direction with respect to the F/R pin input, the 120-degree current-carrying is switched to 150-degree current-carrying when 1 Hall FG frequency is 3.6 Hz (typ) or higher and the rising edge of the IN2 signal has been detected twice in succession.

- ♦ Concerning the Hall signal input sequence
  This IC controls the motor rotation direction commands and Hall signal input sequence in order to set the lead angle. If the motor rotation direction commands and Hall signal input sequence do not conform to what is shown on the timing chart, the motor is driven by 120-degree current-carrying.

Sequence 1: When the Hall signal has been input with the following logic

```
IN1   H      H      H      L      L      L
IN2   L  →   L  →   H  →   H  →   H  →   L
IN3   H      L      L      L      H      H
          ↑ _____|
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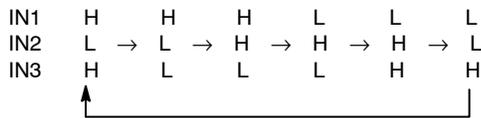
When F/R pin input is high → 120-degree current-carrying
When F/R pin input is low → 150-degree current-carrying

Sequence 2: When the Hall signal has been input with the following logic

```
IN1   H      L      L      L      H      H
IN2   L  →   L  →   H  →   H  →   H  →   L
IN3   H      H      H      L      L      L
          ↑ _____|
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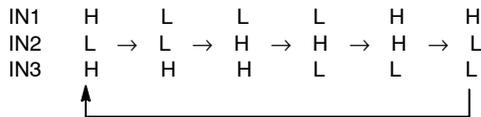
When F/R pin input is high → 150-degree current-carrying
When F/R pin input is low → 120-degree current-carrying

- CTL pin input

a) Standby mode $V_{CTL} < V_{IM}$ (1.5 V : typ)

When the CTL pin voltage is lower than V_{IM}, the IC enters the standby mode. All the H_{IN} and L_{IN} outputs are set to the low level, and the motor prepares to start being driven.

b) Drive mode $V_{IM} \leq V_{CTL} \leq VREG$

When the CTL pin voltage is $V_{IM} \leq V_{CTL} \leq VREG$, the IC enters the drive mode, and the motor is driven at the PWM duty ratio corresponding to V_{CTL}. When V_{CTL} is increased,

the PWM duty ratio increases, and the duty ratio is set internally to 100% at V_{IH} (3.5 V: typ), but the output maximum duty ratio is limited to 88%: typ (when the PWM frequency is 17 kHz).

- SS pin input

a) Start mode 2.9 V < V_{SS} ≤ VREG

When the SS pin voltage is 2.9 V < V_{SS} < VREG, the IC enters the start mode, and the motor is driven by 150-degree current-carrying.

b) Stop mode 0 V ≤ V_{SS} < 0.8 V

When the SS pin voltage is 0 V ≤ V_{SS} < 0.8 V, the IC enters the stop mode, and the motor stops. In the stop state, the drive output and HB pin are OFF, and the FG signal is output.

c) Test mode 2 V < V_{SS} < 2.4 V (Design target)

When the SS pin voltage is 2 V < V_{SS} < 2.4 V, the IC enters the stop mode, and the motor stops. In the stop state, the drive output and HB pin are OFF, and the FG signal is output.
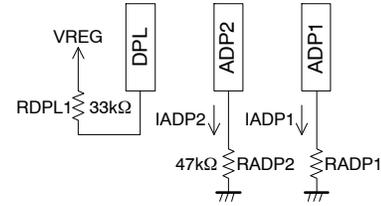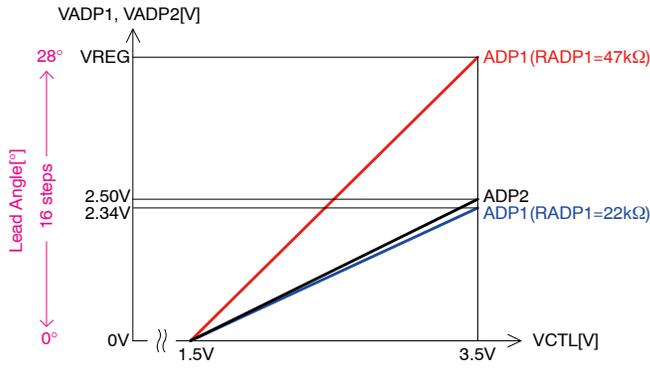
- Bootstrap capacitor initial charging mode

When the mode is changed from stop to start or when the mode is changed from standby to drive, the IC enters the bootstrap capacitor charging mode ($H_{IN}1, H_{IN}2, H_{IN}3 = L$ $L_{IN}1, L_{IN}2, L_{IN}3$ constitute the output (2.2 ms typ) that supports the 120-degree current-carrying mode) in order to charge the bootstrap capacitor.

- Drive phase adjustment

During 150-degree current-carrying drive, current-carrying is started from the phase that is 20 degrees ahead of the 120-degree current-carrying. From this state, any lead angle from 0 to 28 degrees can be set using the ADP1 pin voltage (lead angle control). This setting can be adjusted in 16 steps (in 1.875-degree increments) from 0 to 28 degrees using the ADP1 pin voltage, and it is updated every Hall signal cycle (it is sampled at the rising edge of the IN3 input and updated at its falling edge).

A number of lead angle adjustments proportionate to the CTL pin voltage can be undertaken by adjusting the resistance levels of resistors connected to the ADP1 pin, ADP2 pin and DPL pin. When these pins are not going to be used, reference must be made to section 5. 6, and the pins must not be used in the open status. Furthermore, a resistance of 47 kΩ or more must be used for the resistor (RADP2) that is connected to the ADP2 pin.

1. The slopes of V_{CTL} and VADP1 can be adjusted by setting the resistance level of the resistor (RADP1) connected to ADP1 (pin 30).

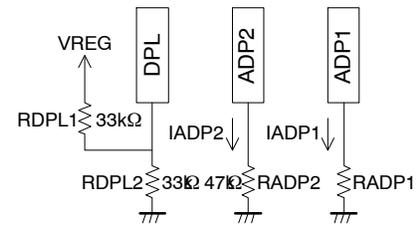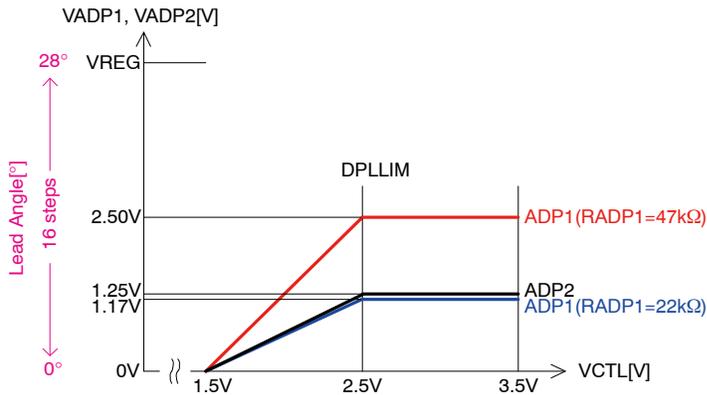Graph 1: VADP1, VADP2[V] vs VCTL[V]. Lead Angle[°] 16 steps, 0° to 28°.
- ADP1(RADP1=47kΩ)
- ADP2
- ADP1(RADP1=22kΩ)
- Values: VREG (28°), 2.50V, 2.34V, 0V; VCTL: 1.5V, 3.5V
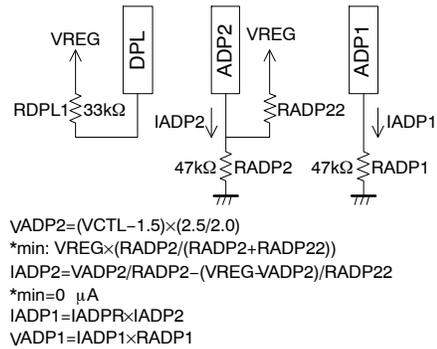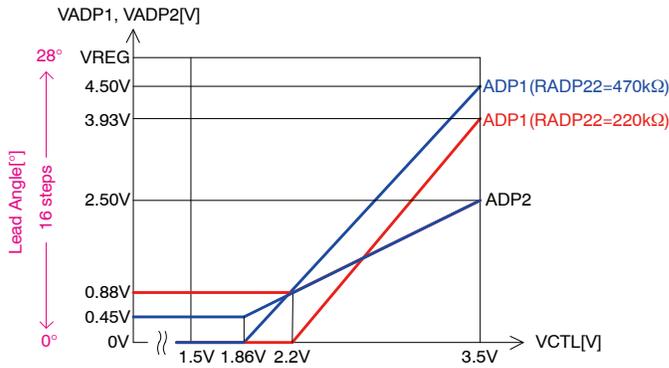- VREG, RDPL1 33kΩ, DPL, ADP2, ADP1, IADP2, IADP1, 47kΩ RADP2, RADP1

$$VADP2=(VCTL-1.5)\times(2.5/2.0)$$
$$IADP2=VADP2/RADP2$$
$$IADP1=IADPR\times IADP2$$
$$VADP1=IADP1\times RADP1$$

2. The ADP2 pin rise can be halted (a limit on the lead angle adjustment can be set by means of the CTL voltage) by setting DPL (pin 25).

Graph 2: VADP1, VADP2[V] vs VCTL[V]. Lead Angle[°] 16 steps, 0° to 28°.
- DPLLIM
- ADP1(RADP1=47kΩ)
- ADP2
- ADP1(RADP1=22kΩ)
- Values: VREG (28°), 2.50V, 1.25V, 1.17V, 0V; VCTL: 1.5V, 2.5V, 3.5V
- VREG, RDPL1 33kΩ, DPL, ADP2, ADP1, IADP2, IADP1, RDPL2 33kΩ, 47kΩ RADP2, RADP1

$$VADP2=(VCTL-1.5)\times(2.5/2.0)$$
$$IADP2=VADP2/RADP2$$
$$IADP1=IADPR\times IADP2$$
$$VADP1=IADP1\times RADP1$$
$$DPLLIM=VDPL$$

3. The offset and slope can be adjusted as desired by setting RADP1 and RADP12 of ADP1 (pin 30). (It is also possible to set a limit on the lead angle adjustment by means of the CTL voltage by setting DPL.)

Graph 3: VADP1, VADP2[V] vs VCTL[V]. Lead Angle[°] 16 steps, 0° to 28°.
- ADP1 (RADP1=47kΩ,RADP12=220kΩ)
- ADP1 (RADP1=33kΩ,RADP1=33kΩ)
- ADP2
- Values: VREG (28°), 4.26V, 2.50V, 0.88V, 0V; VCTL: 1.5V, 3.5V
- VREG, RDPL1 33kΩ, DPL, ADP2, ADP1, VREG, IADP2, IADP1, RADP12, 47kΩ RADP2, RADP1
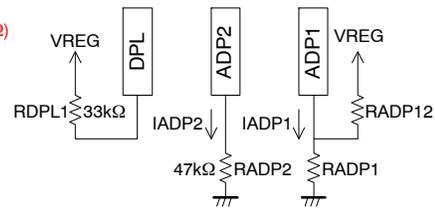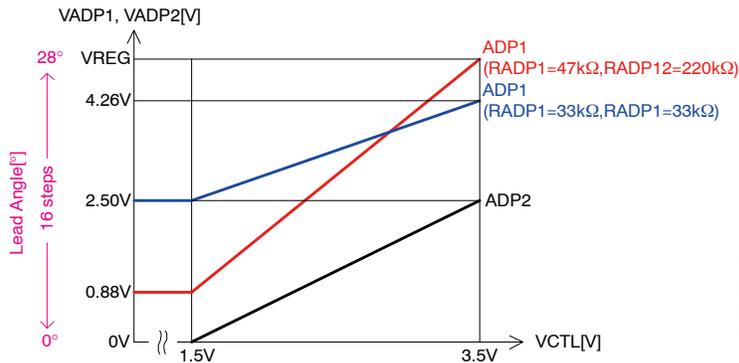
$$VADP2=(VCTL-1.5)\times(2.5/2.0)$$
$$IADP2=VADP2/RADP2$$
$$IADP1=IADPR\times IADP2$$
$$VADP1=((RADP1\times RADP12)/(RADP1+RADP12))\times IADP1$$
$$+(RADP1/(RADP1+RADP12))\times VREG$$

4. The rising voltage of ADP1 can be adjusted using the settings of RADP21 and RADP22 of ADP2 (pin 28). However, they must be set in such a way that the ADP2 voltage does not exceed 1 V when V_{CTL} is lower than 1.5 V.

$VADP2 = (VCTL - 1.5) \times (2.5/2.0)$
*min: $VREG \times (RADP2/(RADP2 + RADP22))$
$IADP2 = VADP2/RADP2 - (VREG - VADP2)/RADP22$
*min = 0 µA
$IADP1 = IADPR \times IADP2$
$VADP1 = IADP1 \times RADP1$

5. When the lead angle is not adjusted
   ADP1 pin: shorted to ground; ADP2 pin and DPL pin: pulled down to ground using the resistors
6. When the lead angle is not adjusted by means of the CTL pin voltage (for use with a fixed lead angle)
   ADP1 pin: lead angle setting by resistance division from VREG; ADP2 pin and DPL pin: pulled down to ground by the resistors

Description of LV8133

1. Current Limiter Circuit

The current limiter circuit limits the output current peak value to a level determined by the equation $I = V_{RF}/Rf$ (where V_{RF} = 0.25 V typ, Rf is the value of the current detection resistor). The current limiter operates by reducing the output on duty to suppress the current.

The current limiter circuit detects the reverse recovery current of the diode due to PWM operation. To assure that the current limiting function does not malfunction, its operation has a delay of approx. 1 µs. If the motor coils resistance or a low inductance, current fluctuation at startup (when there is no back electromotive force in the motor) will be rapid. The delay in this circuit means that at such times the current limiter circuit may operate at a point well above the set current. Application must take this increase in the current due to the delay into account when the current limiter value is set.

2. Motor Stop (SS pin)

With the motor stop operation using the SS pin, the current consumption can be reduced by setting the drive output and HB pin to OFF.

Furthermore, since the VREG5 voltage and FG1 signal can be output, the motor rotation information can be output even in the motor stop mode by supplying the Hall bias from VREG5.

3. Hall Input Signal

Signals with an amplitude in excess of the hysteresis (40 mV max) is required for the Hall inputs. However, considering the influence of noise and phase displacement, an amplitude of over 120 mV is desirable.

If noise disrupts the output waveform (at phase change), this must be prevented by inserting capacitors or other devices across the Hall inputs. The constraint protection circuit uses the Hall inputs to discriminate the motor constraint state. Although the circuit is designed to tolerate a certain amount of noise, care is required.

If all three phases of the Hall input signal go to the same input state (HHH or LLL), the H_{IN}/L_{IN} outputs are all set to the low state.

If the outputs from a Hall IC are used, fixing one side of the inputs (either the + or – side) at a voltage within the common-mode input voltage range (0.3 V to VREG-1.7 V) allows the other input side to be used as an input over the 0 V to VREG range.

4. Constraint Protection Circuit

A constraint protection circuit is incorporated in order to protect the output elements and motor when the motor is constrained. The circuit is activated when the Hall signal is not switched for a specific period of time when the motor is in operation. The counter is reset each time the motor rotates 360 degrees in terms of the electrical angle.

All the H_{IN} and L_{IN} outputs are set to the low level when the constraint protection circuit is in operation.

This time is determined by the capacitance of the capacitor connected to the CSD pin.

Oscillation time of CSD pin (1 pulse)
$T = | (V_{OH} - V_{OL}) / ICHG1 | \times C \, (\mu F) +$
$+ | (V_{OH} - V_{OL}) / ICHG2 | \times C \, (\mu F)$
Constraint protection detection time T1 (s) = $T \times 256$ (count)
Constraint protection time T2 (s) = $T \times 2816$ (count)

When a 0.022 µF capacitor is attached, T = 8.36 ms, T1 = 2.14 s and T2 = 23.54 s are established as the typical ratings. After the motor has been constrained, the constraint protection state is established at 2.14 (s), and then after 23.54 (s) has elapsed, the constraint protection circuit is reset automatically. A time that provides some leeway in the

motor start time that factors in any fluctuations must be selected as the setting.

Conditions for releasing the constraint protection state other than by automatic resetting:

When CTL pin voltage < V_{IM} input $\rightarrow$ protection release and CSD count reset

When the low level is detected on the SS pin $\rightarrow$ protection release and CSD count reset

When FR has been switched $\rightarrow$ protection release and CSD count reset

When TSD protection is detected $\rightarrow$ CSD count stop

5. Power Supply Stabilization

Since this IC adopts a switching drive technique, the power-supply line level can be disrupted easily. Thus capacitors large enough to stabilize the power supply voltage must be inserted between the V_{CC} pins and ground. If the electrolytic capacitors cannot be connected close to their corresponding pins, ceramic capacitors of about 0.1 µF must be connected near these pins.

If diodes are inserted in the power-supply line to prevent destruction of the device when the power supply is connected with reverse polarity, the power supply line levels will be even more easily disrupted, and even larger capacitors must be used.

6. VREG Stabilization

Connect a capacitor with a capacitance of 0.1 µF or more between VREG5 and ground in order to stabilize the VREG voltage that is the power supply of the control circuit.

The ground lead of that capacitor must be located as close as possible to the control system ground (SGND) of the IC.

7. Forward/Reverse Switching (F/R pin)

Switching between forward rotation and reverse rotation must not be undertaken while the motor is running.

8. PWM Frequency Setting

fCPWM ≈ 1/ (1.7CR)

Components with good temperature characteristics must be used.

An oscillation frequency of about 17 kHz is obtained when a 2200 pF capacitor and 15 kΩ resistor are used. If the PWM frequency is too low, switching noise will be heard from the motor; conversely, if it is too high, the output power loss will increase. For this reason, a frequency between 15 kHz and 30 kHz or so is desirable. The capacitor ground must be connected as close as possible to the control system ground (SGND pin) of the IC to minimize the effects of the outputs.

If there are no fluctuations in the capacitance or resistance of the external capacitors or resistors and only the IC fluctuations are to be considered, an actual capability of ±3% can be expected.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SSOP30 (225 mil)
CASE 565AZ
ISSUE A

DATE 25 OCT 2013

8.25 MAX
8.0±0.1

30

4.4±0.1

6.4±0.3

1 2

0.5

(0.5)

0.22 +0.1/−0.05

⊕ | 0.12 Ⓜ

0~10°

0.5±0.2

0.15 +0.15/−0.05

(1.5) 1.7 MAX

⌀ | 0.10

0.1±0.1

SOLDERING FOOTPRINT*

(Unit: mm)

1.00

5.80

0.50   0.32

NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
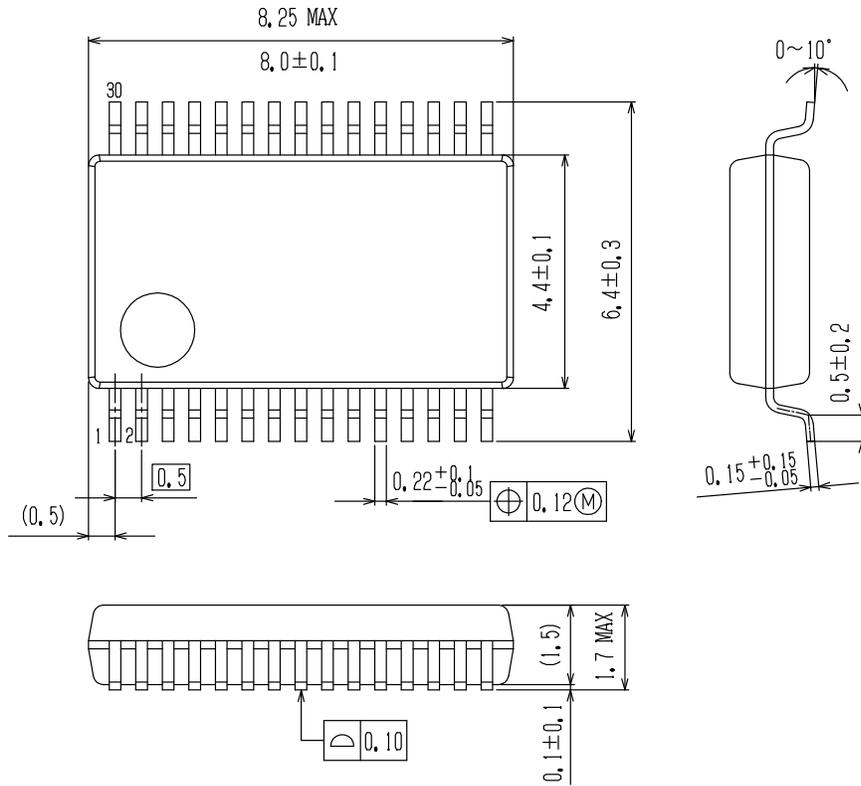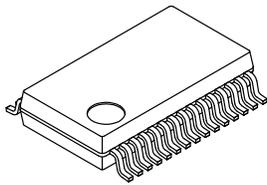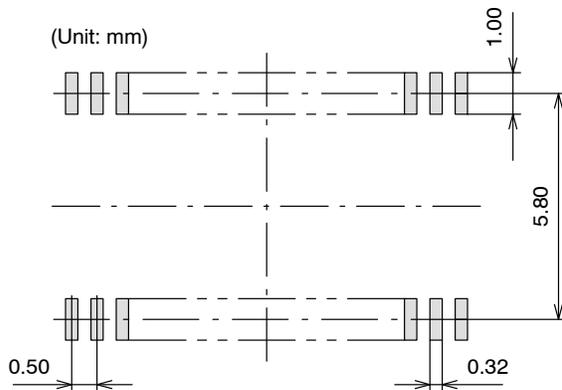
GENERIC
MARKING DIAGRAM*
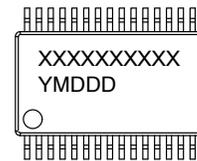
XXXXXXXXXX
YMDDD

XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

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