LPA2010S

3W Filter-free Mono Class-D Audio Power Amplifier

Features

- 2.5-5.5V Operation Voltage
- 4.5mA Quiescent Current
- <1μA Shutdown Current
- Maximum Battery Life and Minimum Heat:
  - up to 87% efficiency at 1.7W
- 500kHz fixed frequency switching
- Optimized PWM Output Stage Eliminates LC Output Filter
- Low EMI
- Output Power (P_O) at 10% THD+N:

  VDD=5V, 4Ω load, 2.8W
- Output Power (P_O) at 1% THD+N:

  VDD=5V, 4Ω load, 2.3W
- External Gain Configuration Capability
- Short Circuit Protection
- RoHS Compliant and 100% Lead(Pb)-Free
- Package: MSOP8/DFN-8（2*2mm）

Applications

- GPS Tracker
- PSP
- BT Speaker
- Portable Electronic Devices

General Description

The LPA2010S is a 3-W high efficiency filter-free mono class-D audio power amplifier (class-D amp) that requires only few external components. Its low THD+N feature offers high-quality sound reproduction. The new filterless architecture allows the device to drive speakers directly instead of using low-pass output filters thus saving PCB area and system cost.

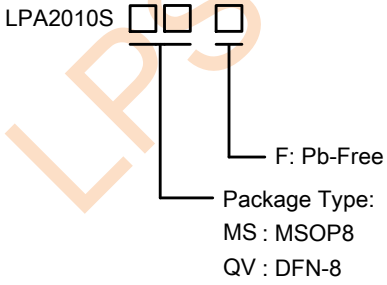
The LPA2010S contains circuitry to prevent “pop and click” noise that would occur during turn-on and turn-off transitions. For maximum flexibility, the LPA2010S provides an externally controlled gain (with resistors), as well as an externally controlled turn-on and turn-off times (with the bypass capacitor).

The LPA2010S is capable of delivering 2.8W of continuous average power to a 4Ω load from a 5V power supply with less than 10% distortion (THD+N). The device utilizes a fully differential architecture, a full-bridged output, and a low-EMI modulation scheme.

The LPA2010S is designed specifically to provide high quality output audio power with a minimal number of external components. The LPA2010S does not require output coupling capacitors or bootstrap capacitors, and therefore is ideally suited where minimal board or solution size is a primary requirement. It features a low-power shutdown mode, which is achieved by driving the SD pin with logic low. Additionally, the LPA2010S features output short-circuit protection and internal thermal-overload protection.

The LPA2010S is available in a MSOP8&DFN-8 package.

Marking Information



Ordering and Package Information

Part Number	Top Mark	Package	T&R
LPA2010SMSF	LPS LPA2010S YWXXX	MSOP8	3K/REEL
LPA2010SQVF	LPS CAYWX	DFN-8	4K/REEL
Marking indication: Y: Production Year, W: Production week, X: Series Number			

Typical Application Circuits

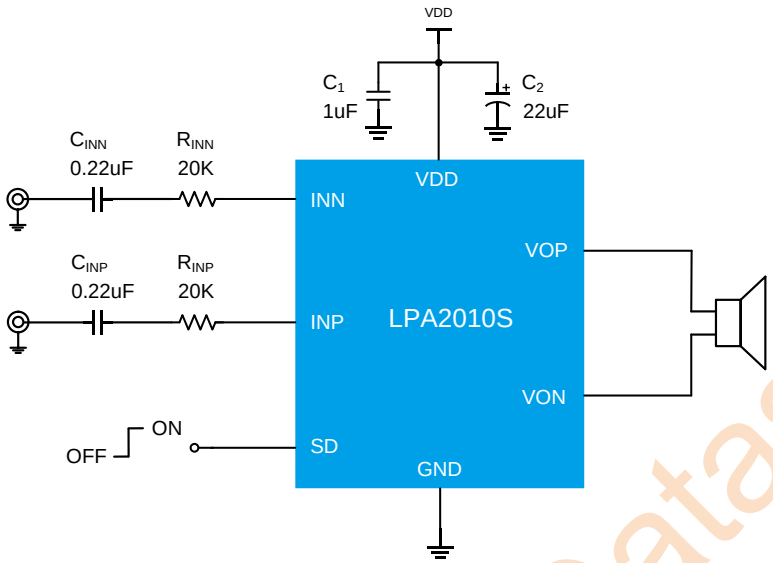


Figure 1-1. Typical Application Circuits with Differential Input

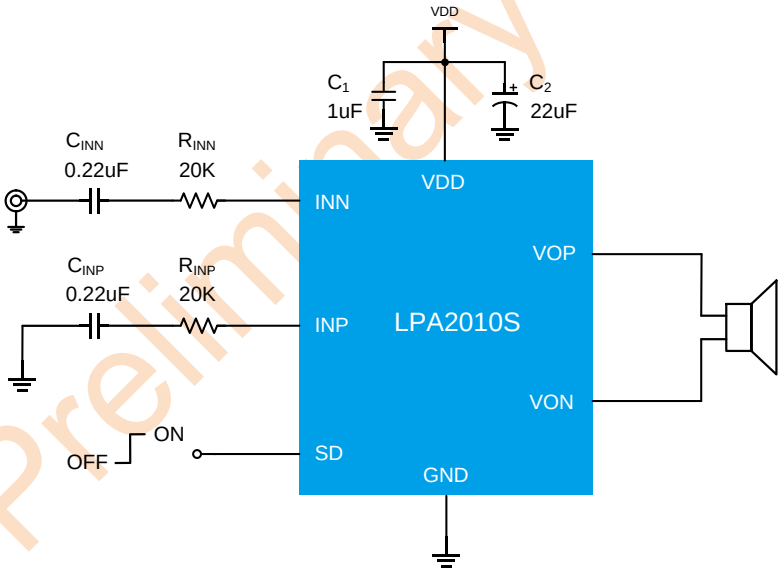
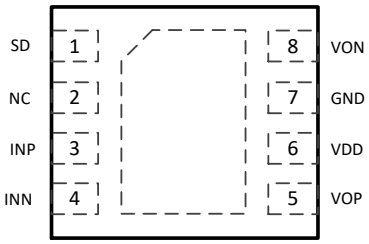
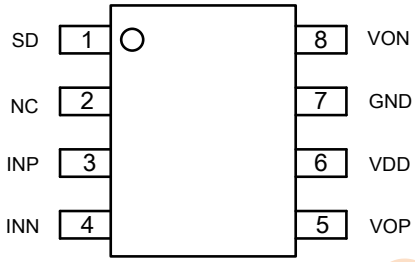


Figure 1-2. Typical Application Circuits with Single Input

Pin Configuration



DFN-8 (Top View)



MSOP8 (Top View)

Pin Description

Pin	Name	Description
1	SD	Shutdown input pin. The device is enabled with this pin pulled high. The device enters the shutdown mode if this pin is floating or pulled low. This pin is internally pulled down to ground through the R_{PD} resistor (refer to Electrical Characteristics Table).
2	NC	No connection.
3	INP	Positive input of the first amplifier. This pin receives the common mode voltage.
4	INN	Negative input of the first amplifier. This pin receives the audio input signal. Connect this pin to the feedback resistor R_F and to the input resistor R_{IN} (refer to Figure 2).
5	VOP	Positive output.
6	VDD	VDD power supply input. Connect at least 1μF ceramic capacitor as close as possible to this pin.
7	GND	Ground.
8	VON	Negative output.

Functional Block Diagram

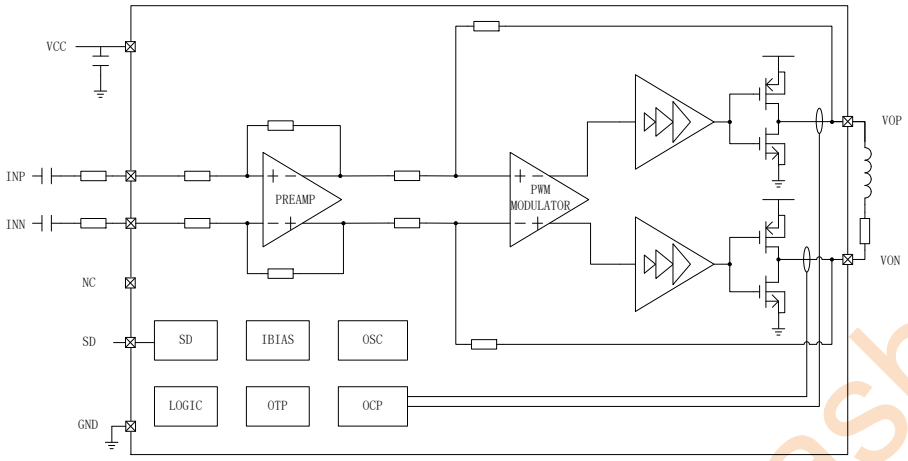


Figure 2. Internal Block Diagram

Absolute Maximum Ratings (Note 1)

- VDD/VON/VOP to GND ---------- -0.3V to + 6V
- Other pins to GND ---------- -0.3V to + 5.5V
- Maximum Junction Temperature (T_{JMAX}) ---------- -40°C to 162°C
- Operating Ambient Temperature Range(Ta) ---------- -40°C to 85°C
- Storage Temperature Range, T_{stg} ---------- -65°C to 150°C
- Maximum Soldering Temperature (at leads, 10 seconds) ---------- 260°C

***Note 1: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, instead of functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.**

Thermal Information

- Maximum Power Dissipation (MSOP8 , T_A = 25℃) ---------- 1.1W
- Thermal Resistance (MSOP8, θJA) (Note 2) ---------- 127°C/W
- Maximum Power Dissipation (DFN-8 ,T_A = 25℃) ---------- 1.3W
- Thermal Resistance (DFN-8 , θJA) (Note 2) ---------- 107°C/W

***Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX}= (T_{JMAX}–T_A)/ \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LPA2010S, T_{JMAX}= 162˚C. For the θ_{JA}, it is based on 2S2P JEDEC standard PCB.**

ESD Information

- HBM(Human Body Mode) ---------- 4kV
- MM(Machine Mode) ---------- 200V

Recommended Operating Conditions

- Input Voltage ---------- 2.5V to 5.5V
- Ambient Temperature ---------- -20°C to 80°C
- Junction Temperature---------- -20°C to 125°C

Electrical Characteristics

The following parameters are guaranteed under condition V_{DD} =5V, T_A = -40°C to 85°C unless otherwise noted. T_A = 25°C for typical value.

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
V_{OS}	Output offset voltage (Measured differentially)	V_i=0V, RINN=RINP=20K, V_{SD}=V_{DD}=2.5V to 5.5V			5		mV
I_Q	Quiescent current	V_{DD}=5V, no load			4.5		mA
I_{SD}	Shutdown Current	V_{SD}=0.35V, V_{DD}=2.5V to 5.5V			0.15		μA
Po	Output power	f=1kHz, R_L=4Ω, THD=10%	V_{DD}=5V		2.8		W
			V_{DD}=4.2V		1.9		
			V_{DD}=3.6V		1.4		
		f=1kHz, R_L=4Ω, THD=1%	V_{DD}=5V		2.3		
			V_{DD}=4.2V		1.6		
			V_{DD}=3.6V		1.1		
		f=1kHz, R_L=8Ω, THD=10%	V_{DD}=5V		1.7		
			V_{DD}=4.2V		1.2		
			V_{DD}=3.6V		0.85		
		f=1kHz, R_L=8Ω, THD=1%	V_{DD}=5V		1.36		
			V_{DD}=4.2V		0.95		
			V_{DD}=3.6V		0.65		
THD+N	Total harmonic distortion plus noise	V_{DD}=5V, Po=1.8W, R_L=4Ω			0.06		%
		V_{DD}=5V, Po=1W, R_L=8Ω			0.05		
PSRR	Supply ripple rejection ratio	V_{DD}=5V, inputs ac-grounded with C_i= 0.47uF, f=217Hz			75		dB
V_n	Output noise voltage	Inputs ac-grounded with Ci=0.47μF, V_{DD}=5V			100		uV
SNR	Signal-to-noise ratio	V_{DD}=5V, f=1kHz, R_L=4Ω, THD=1%			80		dB
F_{SW}	Switching frequency	V_{DD}=5V			500		kHz
V_{SD_H}	SD pin logic High	V_{DD}=5V		1.2			V
V_{SD_L}	SD pin logic Low	V_{DD}=5V				0.4	V

t_{WU}	Device wake up time	V_{DD}=5V, C_{BYP}=1uF		92		ms
R_{PD}	SD pin internal pull-down resistor	V_{DD}=2.5V to 5.5V	160	290	1460	kΩ
R_F	Amplifier internal resistor	V_{DD}=2.5V to 5.5V		160		kΩ
R_S	Amplifier internal resistor	V_{DD}=2.5V to 5.5V		5.4		kΩ
T_{SD}	OTSD			162		°C
T_{SD_HYS}	OTSD Hysteresis			33		°C

Typical Performance Characteristics (T_A = 25°C, RINN=RINP=100K)

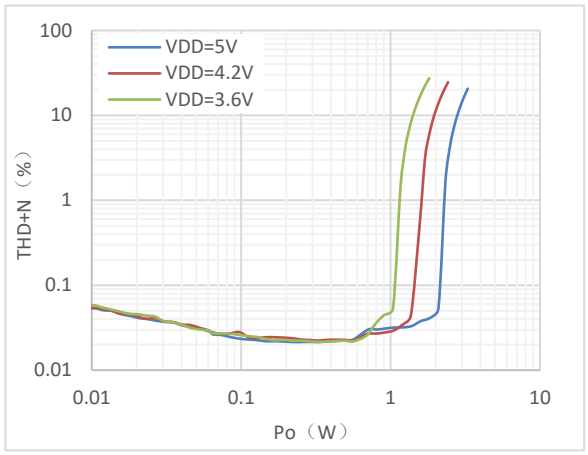


Figure 3. P_o VS THD, R_L=4Ω

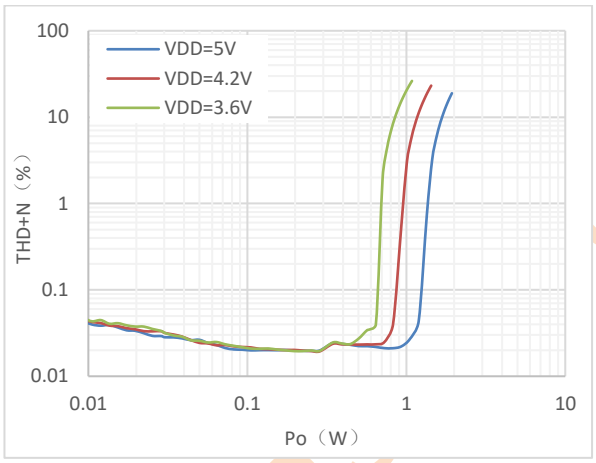


Figure 4. P_o VS THD, R_L=8Ω

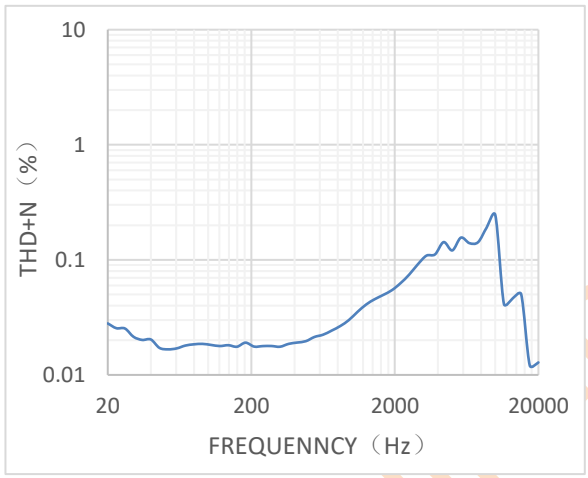


Figure 5. THD+N at VDD=5V, P_o=1W, R_L=4Ω

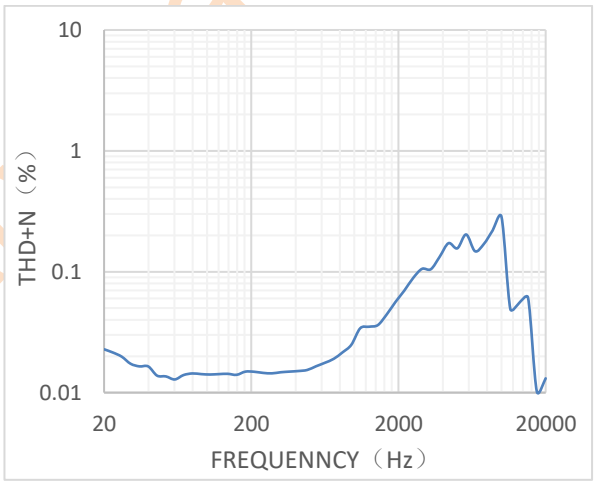


Figure 6. THD+N at VDD=5V, P_o=1W, R_L=8Ω

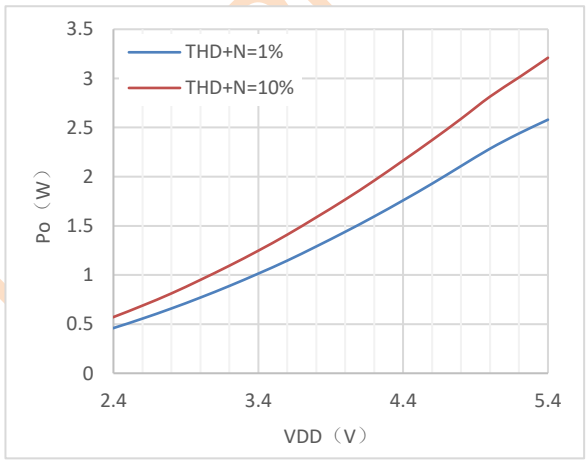


Figure 7. P_O VS VDD, R_L=4Ω

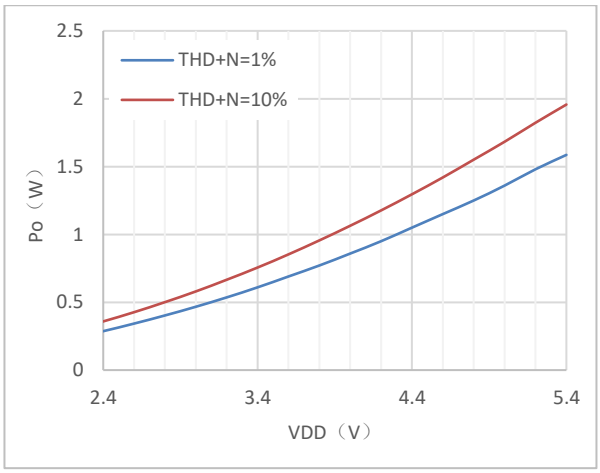


Figure 8. P_O VS VDD, R_L=8Ω

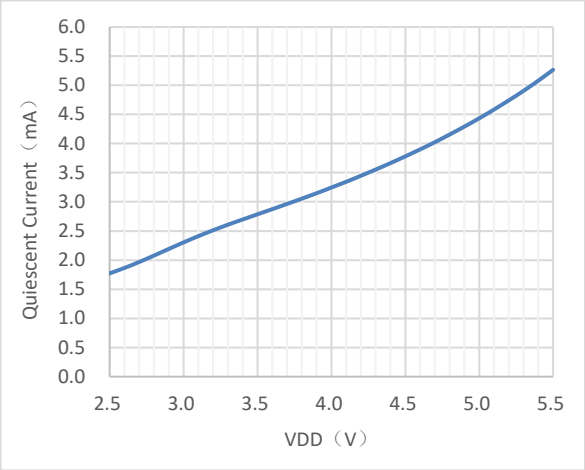


Figure 9. I_Q VS VDD, No input , R_L=8Ω

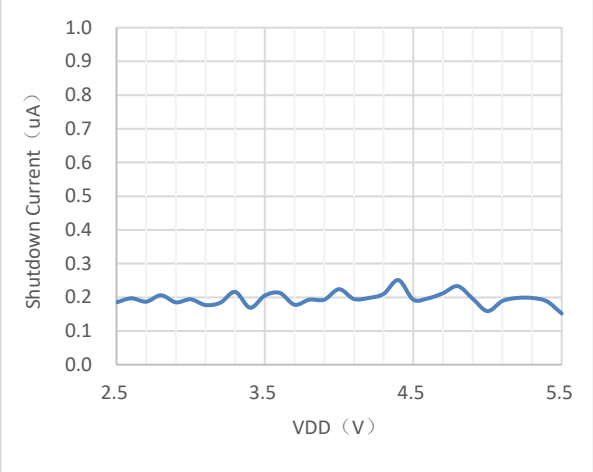


Figure 10. I_{SD} VS VDD, No input , R_L=8Ω

Functional Description

General Description

The LPA2010S is a high-efficiency filter-free Class-D audio amplifier capable of delivering up to 2.8 W into 4-Ω loads with 5-V power supply. The fully differential design of this amplifier avoids the usage of bypass capacitors and the improved CMRR eliminates the usage of input-coupling capacitors. This makes the device size a perfect choice for small, portable applications because only three external components are required. The advanced modulation used in the LPA2010S PWM output stage eliminates the need for an output filter.

Fully Differential Amplifier

As shown in Figure 2, the LPA2010S has two operational amplifiers internally, allowing for a few different amplifier configurations. The first amplifier's gain is externally configurable, while the second amplifier is internally fixed in a unity-gain 2V/V. The close loop gain of the first amplifier is set by selecting the ratio of R_F to R_{IN} + R_{IN1} while the R_{IN1} is the external input resistor. Figure 2 shows the output of the amplifier one serves as the input to amplifier two, which results in both amplifiers producing signals identical in magnitude, but out of phase by 180°. Consequently, the differential gain A_{VD} for the IC is

$$A_{VD} = 2 \times \frac{R_F}{R_{IN} + R_S}$$

By driving the load differentially through outputs VOP and VON, an amplifier configuration commonly referred to as “BTL mode” is established. The BTL mode operation is different from the classical single-ended amplifier configuration where one side of the load is connected to ground.

The LPA2010S uses a modulation scheme that still has each output switching from 0 to the supply voltage. However, VOP and VON are now in phase with each other with no input. The duty cycle of VOP is greater than 50% and VON is less than 50% for positive voltages. The duty cycle of VOP is less than 50% and VON is greater than 50% for negative voltages. The voltage across the load sits at 0 volts throughout most of the switching period greatly reducing the switching current, which reduces any I^2R losses in the load.

Power Supply Bypassing

The LPA2010S is a high-performance class-D audio amplifier that requires adequate power supply decoupling to ensure the efficiency is high and total harmonic distortion (THD) is low. The capacitor location on power supply pin should be as close to the device as possible. Typical applications employ a 5V regulator with 10 µF tantalum or electrolytic capacitor and a ceramic bypass capacitor that aid in supply stability. This does not eliminate the need for bypassing the supply nodes of the LPA2010S. The selection of a bypass capacitor is dependent upon PSRR requirements, click and pop performance, system cost, and size constraints.

Shutdown Mode

The LPA2010S contains a SD pin, it can put the device into shutdown mode when asserting SD pin to a logic LOW. While in shutdown mode, the device output stage is turned off and set into high impedance, making the current consumption very low. The device exits shutdown mode when a HIGH logic level is applied to the /SD pin. The LPA2010S has an internal pull-down resistor (R_{PD}) on the SD pin, if SD pin is floating, the device will shut down. By switching the SD pin to logic LOW or connect it to ground directly, the LPA2010S supply current draw will be minimized to shutdown current (I_{SD}), which is 0.15uA in typical.

Short Circuit Protection

The LPA2010S has short circuit protection circuitry on the outputs to prevent damage to the device when output-to-output or output-to-GND short occurs. When a short circuit is detected on the outputs, the outputs are disabled immediately. If the short was removed, the device activates again.

Thermal Shutdown

The LPA2010S has thermal shutdown protection to fully protect the device from internally or externally generated excessive temperatures. This protection scheme prevents the device from damage when the die temperature is too high. The thermal shutdown circuit is activated when the die temperature exceeds a safe temperature (typ 162°C) and the amplifier is turned off. The device automatically turns on again if the temperature drops below the threshold temperature.

Application Information

Typical Applications

Figure 1-1 shows the LPA2010S typical schematic with differential inputs and input capacitors, and Figure 1-2 shows the LPA2010S with single-ended inputs. Differential inputs should be used whenever possible because the single-ended inputs are more susceptible to noise.

Decoupling Capacitor

As with any amplifier, proper supply bypassing is critical for low noise performance and high-power supply rejection. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1 μF for C_{VDD} at least, placed as close as possible to the device VDD lead works best. Placing this decoupling capacitor close to the LPA2010S is very important for the efficiency of the class-D amplifier, because any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency. For filtering lower-frequency noise signals, a 10 μF or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

Input Capacitor

The LPA2010S does not require input coupling capacitors if the design uses a differential source that is biased from 0.5V to V_{DD}-0.8V. If the input signal is not biased within the recommended common-mode input range, if needing to use the input as a high pass filter (shown in Figure 1-2), or if using a single-ended source (shown in Figure 1-1), input coupling capacitors are required. The input capacitors and input resistors form a high-pass filter with the corner frequency, f_c, determined in below Equation:

$$f_C = \frac{1}{2\pi * (R_S + R_{IN}) * C_{IN}}$$

The value of the input capacitor is important to consider as it directly affects the bass (low frequency) performance of the circuit. Speakers in wireless phones cannot usually respond well to low frequencies, so the corner frequency can be set to block low frequencies in this application.

If the corner frequency is within the audio band, the capacitors should have a tolerance of ±10% or better, because any mismatch in capacitance causes an impedance mismatch at the corner frequency and below. For a flat low-frequency response, use large input coupling capacitors (1 μF). However, in a GSM phone the ground signal is fluctuating at 217 Hz, but the signal from the codec does not have the same 217 Hz fluctuation. The difference between the two signals is amplified, sent to the speaker, and heard as a 217 Hz hum.

Shutdown Mode

The device contains a SD pin to externally turn off the amplifier. In many applications, a microcontroller or microprocessor output is used to control the shutdown circuitry to provide a quick, smooth transition into shutdown. Another solution is to use a switch, When the switch is closed, the SD pin is connected to VDD and turn-on the amplifier. If the switch is open, the internal pull-down resistor will disable the LPA2010S. This scheme ensures that the SD pin will not float thus preventing unwanted state changes.

Output filter

Design the LPA2010S without an Inductor/Capacitor(LC) output filter if the traces from the amplifier to the speaker are short. Wireless handsets and PDAs are great applications for this class-D amplifier to be used without an output filter.

The LPA2010S does not require an LC output filter for short speaker connections (approximately 100mm long or less). A ferrite bead can often be used in the design if failing radiated emissions testing without an LC filter; And the frequency-sensitive circuit is greater than 1MHz. If choosing a ferrite bead, choose one with high impedance at high frequencies, but very low impedance at low frequencies. The selection must also take into account the currents flowing through the ferrite bead. Ferrites will begin to lose effectiveness when the current beyond its rated current values.

Power Dissipation

Power dissipation is a major concern when designing a successful amplifier, it is critical that the maximum junction temperature T_{JMAX} of 150°C is not exceeded. T_{JMAX} can be determined from the power derating curves by using P_{DMAX} and the PC board foil area. By adding additional copper foil, the thermal resistance of the application can be reduced, resulting in higher P_D. Additional copper foil can be added to any of the leads connected to the LPA2010S. If T_{JMAX} still exceeds 150°C, additional changes must be made. These changes can include reduced supply voltage, higher load impedance, or reduced ambient temperature.

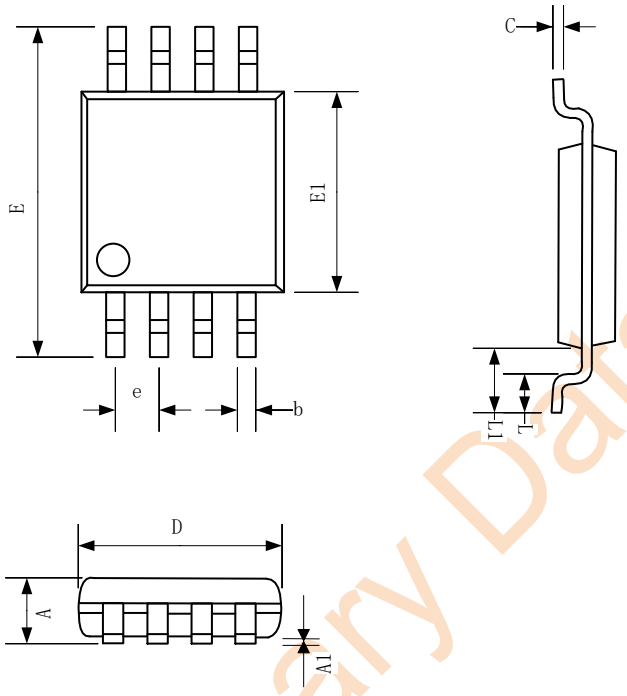
PCB Layout Guidelines

The PCB layout is critical to the optimal performance of an audio amplifier, some general mixed signal layout recommendations for LPA2010S as below:

1. Place the C_{VDD} capacitor as close as possible to the device with short, wide traces to the VDD and GND pins.
2. The power ground should be connected to the analog ground through a single point. It is further recommended to put analog and power traces over the corresponding analog and power ground traces to minimize noise coupling.
3. The PCB traces that connect the output pins to the load and the supply pins to the power supply should be as wide as possible to minimize trace resistance, this is helpful to maintain the highest output voltage swing and corresponding peak output power.
4. Avoid ground loops or running digital and analog traces parallel to each other (side-by-side) on the same PCB layer. Running digital and analog traces at 90 degrees to each other from the top to the bottom side as much as possible will minimize capacitive noise coupling and cross talk.
5. Use wide and thick trace for the high current pins like VDD, VOP, VON and GND, and ensure enough copper area is used for heat dissipation.

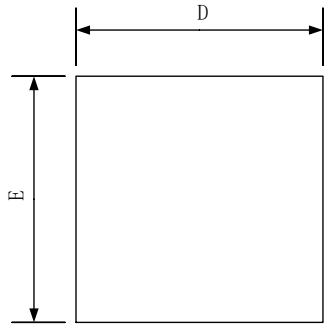
Package Information

MSOP8

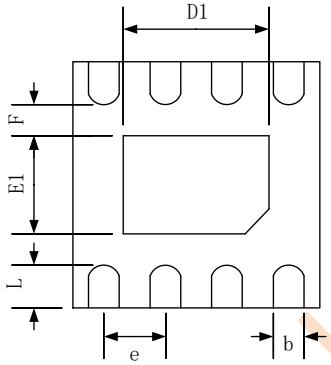


SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.10
A1	0.00	-	0.15
b	0.22	0.30	0.38
c		0.17REF	
D	2.90	3.00	3.10
E	4.70	4.90	5.10
E1	2.90	3.00	3.10
e		0.65BSC	
L	0.40	0.60	0.80
L1		0.95 REF	

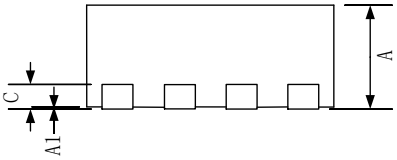
DFN-8



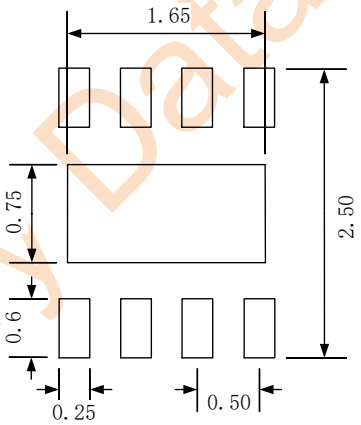
TOP VIEW



BOTTOM VIEW



SIDE VIEW

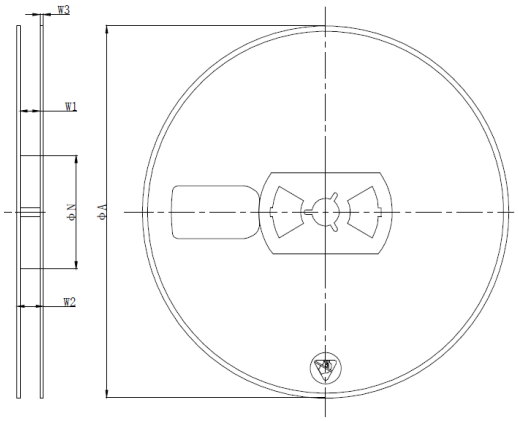


Recommended Land Pattern

SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
c		0.20 REF	
D	1.90	2.00	2.10
D1	1.10	1.30	1.65
E	1.90	2.00	2.10
E1	0.60	0.75	0.85
e		0.50 BSC	
L	0.25	0.35	0.40
F	0.25	0.30	0.35

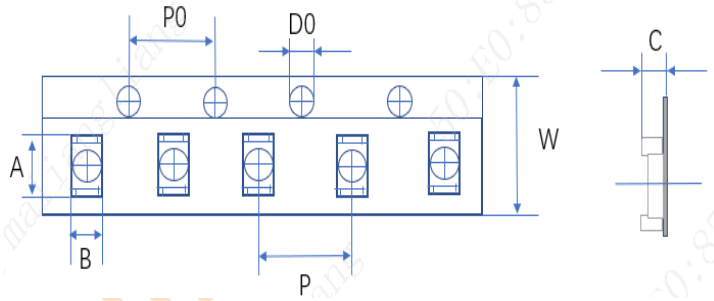
Tape and Reel information

REEL DIMENSIONS（Unit:mm）



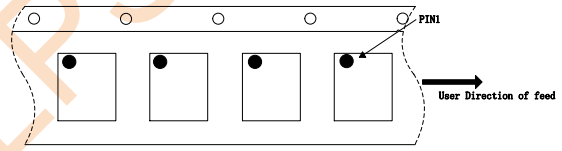
Device	ΦA	W2
LPA2010SMSF	330±4	16±4
LPA2010SQVF	180±4	12±2

TAPE DIMENSIONS（Unit:mm）

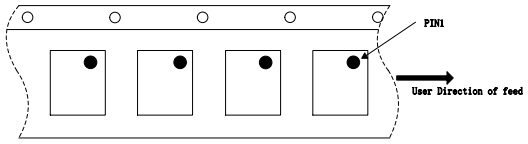


Device	A	B	P0	P	D0	W	C
LPA2010SMSF	5.33±0.2	3.4±0.2	4.0±0.2	8.0±0.2	1.5±0.2	12.0±0.3	1.53±0.2
LPA2010SQVF	2.15±0.15	2.15±0.15	4.0±0.1	4.0±0.1	1.5±0.1	8.0±0.3	1.0±0.2

PIN1 AND TAPE FEEDING DIRECTION



MSOP8



DFN-8

Classification of IR Reflow Profile

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak		
Temperature Min(T_{SMIN})	100℃	150℃
Temperature Max(T_{SMAX})	150℃	200℃
Time(T_S) from (T_{SMIN} to T_{SMAX})	60~120 seconds	60~120 seconds
Ramp-up rate (T_L to T_P)	3℃/second max	3℃/second max
Liquidous temperature(T_L)	183℃	217℃
Time(t_L) maintained above T_L	60~150 seconds	60~150 seconds
Peak package body temperature (T_P)	For users T_P must not exceed theClassification temp in Table 1. For suppliers T_P must equal or exceedthe Classification temp in Table 1.	For users T_P must not exceed theClassification temp in Table 2. For suppliers T_P must equal or exceedthe Classification temp in Table 2.
Time(t_P)* within 5℃ of the specified classification temperature(T_C), see Figure1	20* seconds	30* seconds
Ramp-down rate (T_P to T_L)	6℃/second max	6℃/second max
Time 25℃ to peak temperature	6 minutes max	8minutes max
* Tolerance for peak profile temperature (T_P) is defined as a supplier minimum and a user maximum.		

Table 1Sn-Pb Eutectic Process - Classification Temperatures (T_C)

Package Thickness	Volume mm^3 <350	Volume mm^3 ≥350
<2.5mm	235℃	220℃
≥2.5mm	220℃	220℃

Table 2 Pb-Free Process - Classification Temperatures (T_C)

Package Thickness	Volume mm^3 <350	Volume mm^3 350~2000	Volume mm^3 ≥350
<1.6mm	260℃	260℃	260℃
1.6mm~2.5mm	260℃	250℃	245℃
>2.5mm	250℃	245℃	245℃

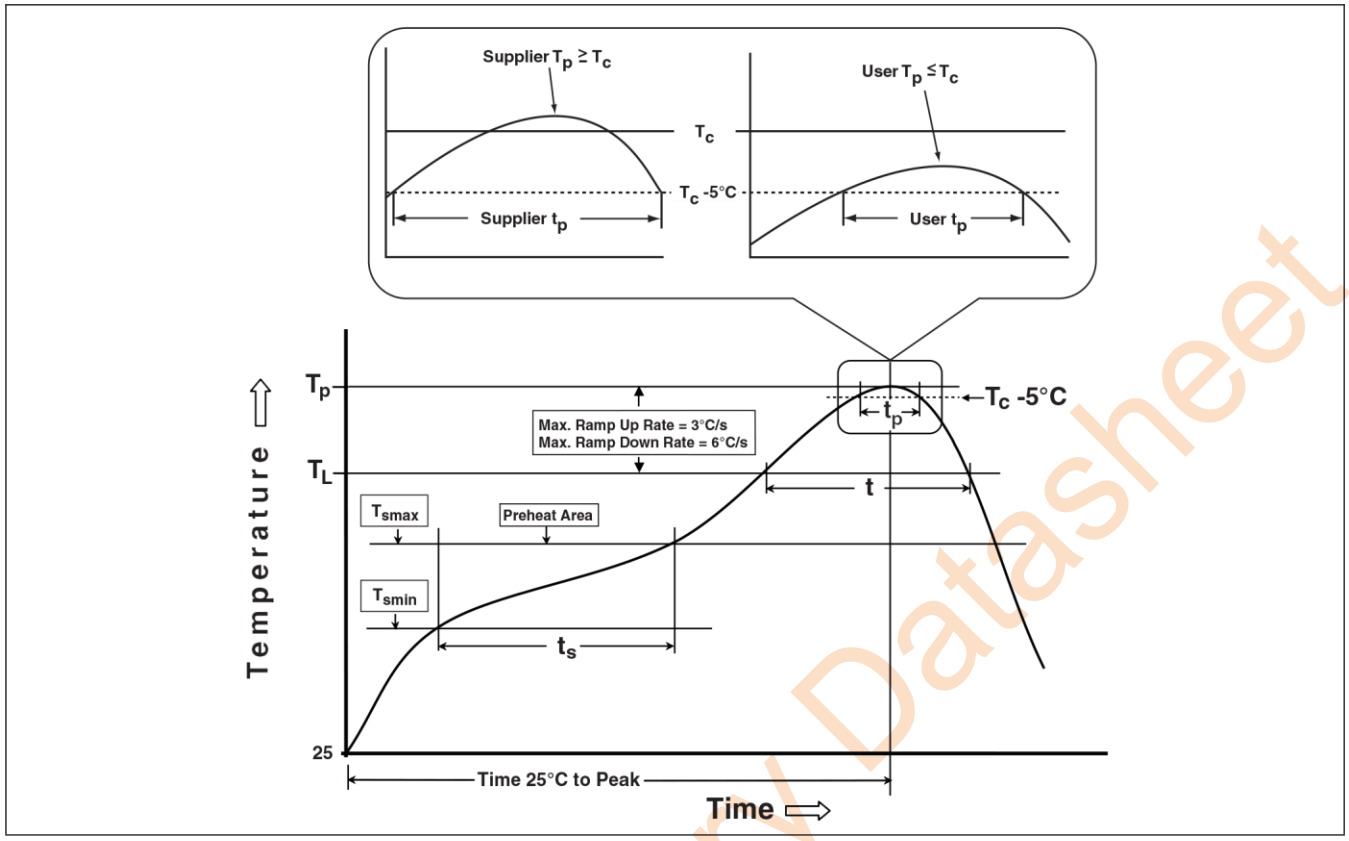


Figure1Classification Profile (Not to scale)

Products conform to "JEDEC J-STD-020C"standards;

Products shipped conform to "Rohs"standards;

Moisture Sensitivity Level：MSL3（CONDITION：≦30 °C/60%RH、Time control:168 hours）;