

1A Single Chip Li-Ion and Li-Polymer Charger

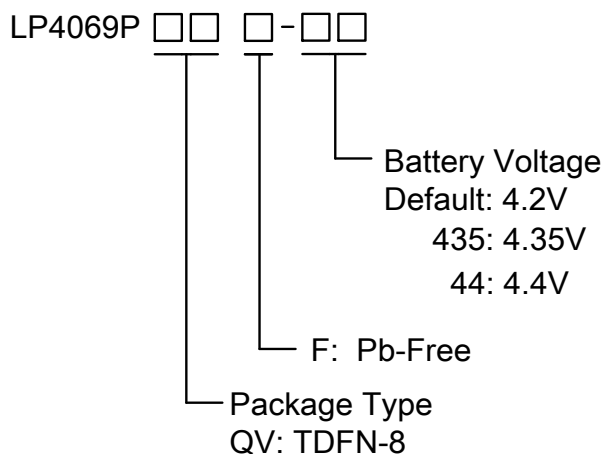
General Description

The LP4069P is a complete constant-current/constant voltage linear charger for single cell lithium-ion battery. No external sense resistor is needed, and no blocking diode is required due to the internal MOSFET architecture. Thermal feedback regulates the charge current to limit the die temperature during high power operation or high ambient temperature. The charge voltage is fixed at V_{FLOAT} , and the charge current can be programmed externally by ISET pin with a single resistor.

The LP4069P automatically terminates the charge cycle when the charge current drops to 1/10 setting current value after the final float voltage is reached.

Other features include charge current monitor, under voltage lockout, automatic recharge, status pins.

Order Information



Features

- ◆ Input Over Voltage Protection : 6.3V
- ◆ Short-circuit protection
- ◆ Programmable Charge Current up to 1A
- ◆ 1 μ A Battery Reverse Current
- ◆ Protection of Reverse Connection of Battery
- ◆ No MOSFET, Sense Resistor or Blocking Diode Required
- ◆ Constant-Current/Constant-Voltage Operation with Thermal Regulation
- ◆ TDFN-8 Package
- ◆ RoHS Compliant and 100% Lead (Pb)-Free

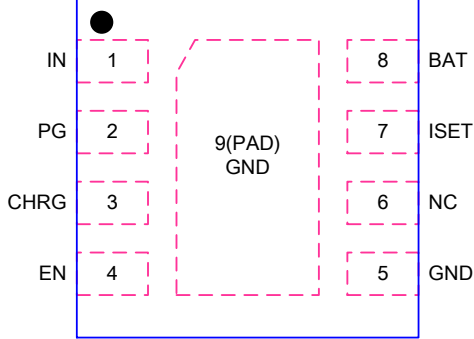
Applications

- ◇ Portable Media Players/Game
- ◇ Power Bank
- ◇ Bluetooth Applications
- ◇ PDA/MID

Marking Information

Device	Marking	Package	Shipping
LP4069PQVF	LP4069 PYWX	TDFN-8	4K/REEL
LP4069PQVF-435	LP4069 P435YW	TDFN-8	4K/REEL
LP4069PQVF-44	LP4069 P44YW	TDFN-8	4K/REEL
Marking indication: Y: Production year W: Production week X: Series Number			

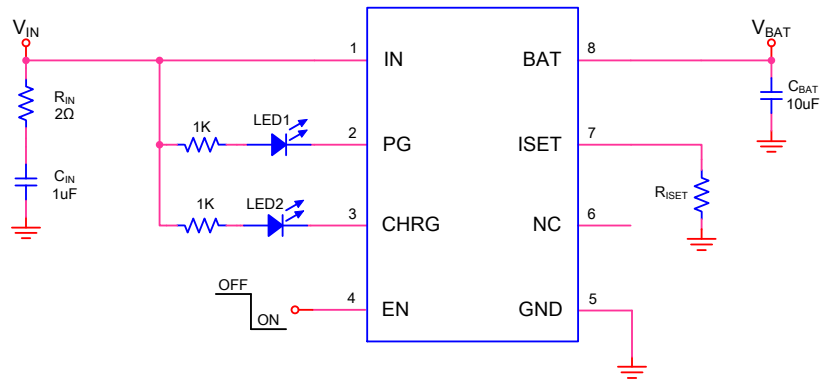
Functional Pin Description

Package Type	Pin Configurations
TDFN-8	 <p>TDFN-8 (Top View)</p>

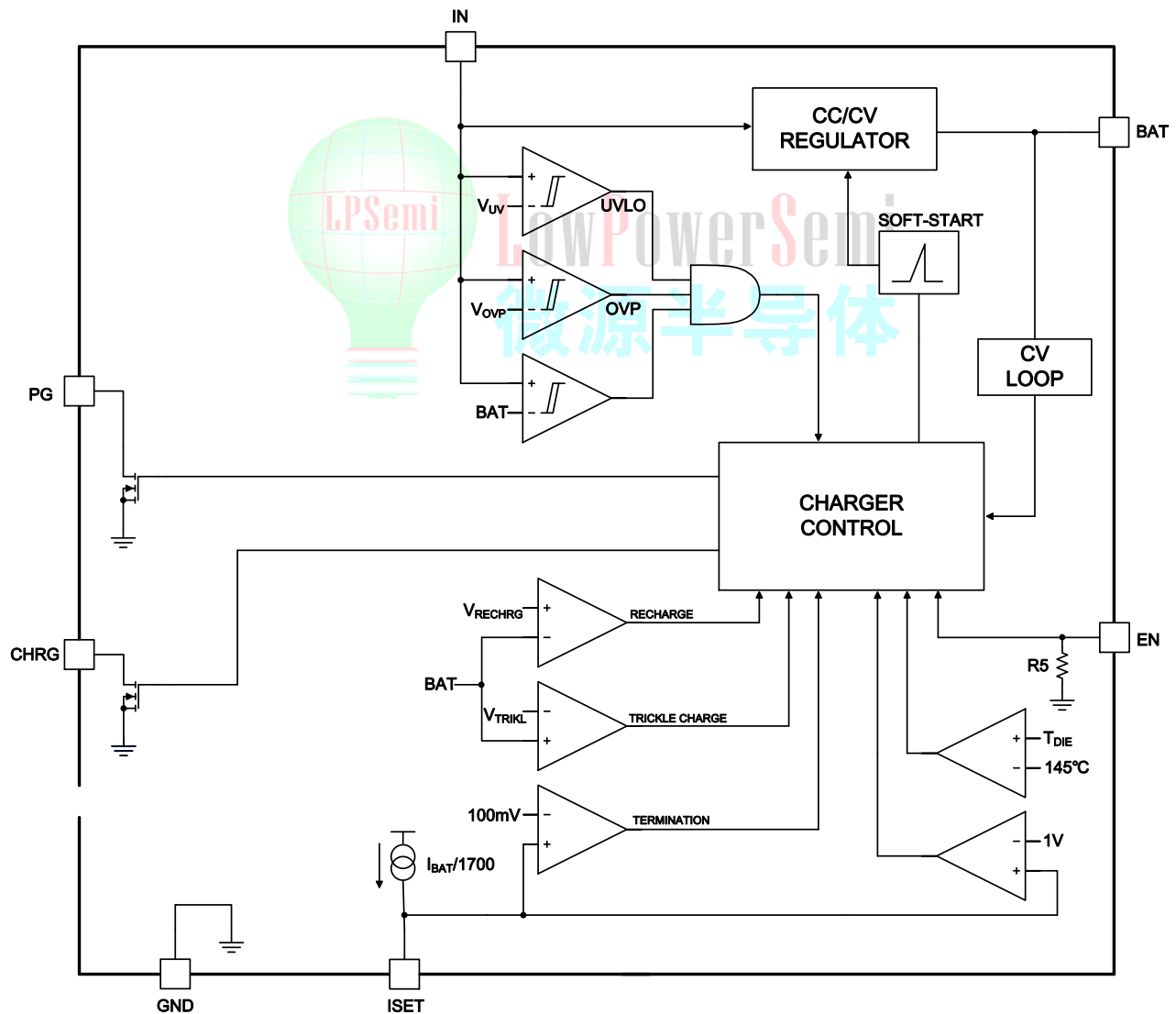
Pin Description

No.	NAME	DESCRIPTION
1	IN	IN is the input power source. Connect to a wall adapter.
2	PG	Open-Drain Status Output. Low indicates the input voltage is above the input UVLO voltage and the OUT (battery)+150mV voltage, and lower than OVP threshold.
3	CHRG	Open-Drain Charge Status Output. When the battery is charging, the CHRG pin is pulled low by an internal N-MOS. When the charge cycle is completed, the pin could be pulled High by an external pull high resistor.
4	EN	Charge Enable Input (active low).
5	GND	GND is the connection to system ground.
6	NC	No Connector.
7	ISET	Charge Current Program. The charge current is programmed by connecting a 1% resistor(R_{ISET}) to ground. $I_{BAT} = \frac{1700 \times V_{ISET}}{R_{ISET}}$
8	BAT	BAT is the connection to the battery. Typically a 10μF Tantalum capacitor is needed for stability when there is no battery attached.
9	PAD	Exposed Pad, use to strengthen dissipation of heat. It usually connect to GND.

Typical Application Circuit



Functional Block Diagram



Absolute Maximum Ratings ^{Note 1}

✧ Input Voltage to GND	-----	-0.3V to 28V
✧ BAT Voltage GND	-----	- 5V to 15V
✧ Other pin to GND	-----	-0.3V to 6.5V
✧ Maximum Junction Temperature(T_J)	-----	150°C
✧ Maximum Soldering Temperature (at leads, 10 sec)	-----	260°C
✧ Operating Junction Temperature Range	-----	-20°C to 85°C
✧ Storage Temperature	-----	-60°C to 125°C

Thermal Information

✧ Maximum Power Dissipation ($P_D, T_A=25^{\circ}\text{C}$)	-----	1.2W
✧ Thermal Resistance (θ_{JA})	-----	95°C/W

ESD Susceptibility

✧ HBM(Human Body Model)	-----	2KV
✧ MM(Machine Model)	-----	200V

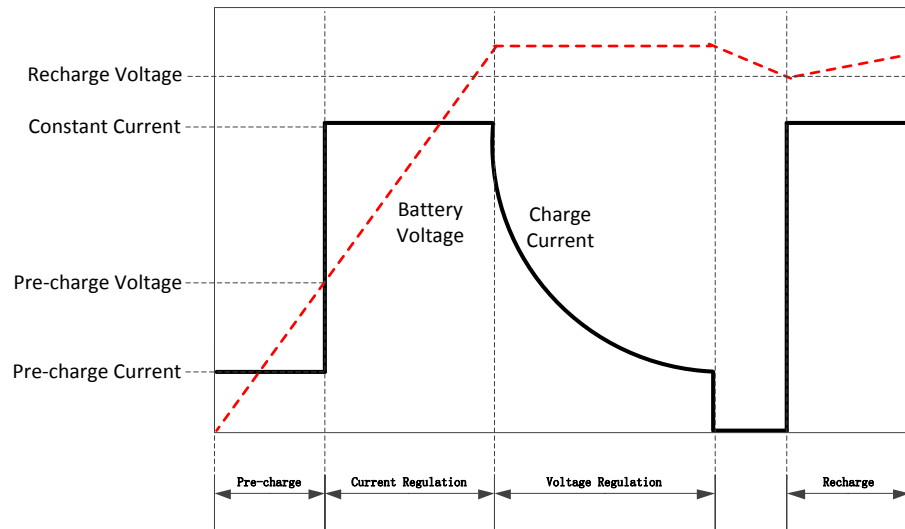
Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(T_A=25°C, V_{IN}=5V, unless otherwise noted.)

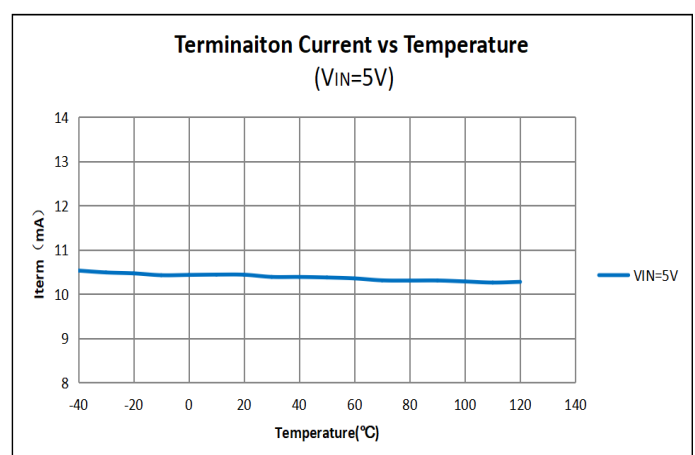
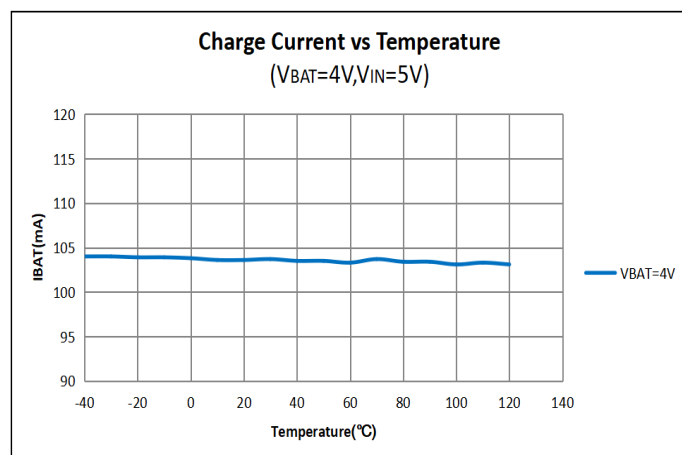
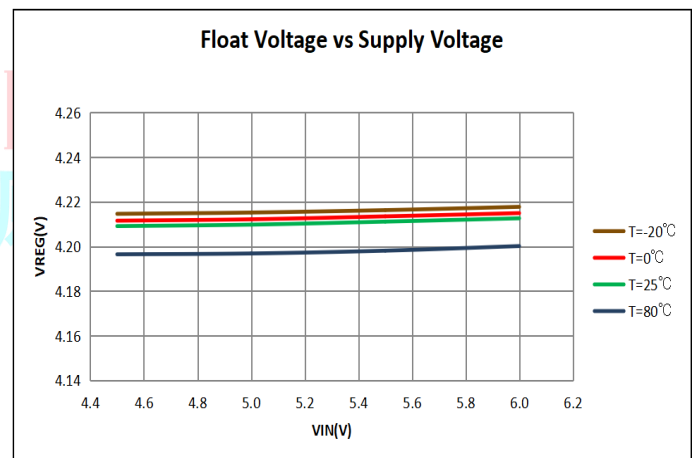
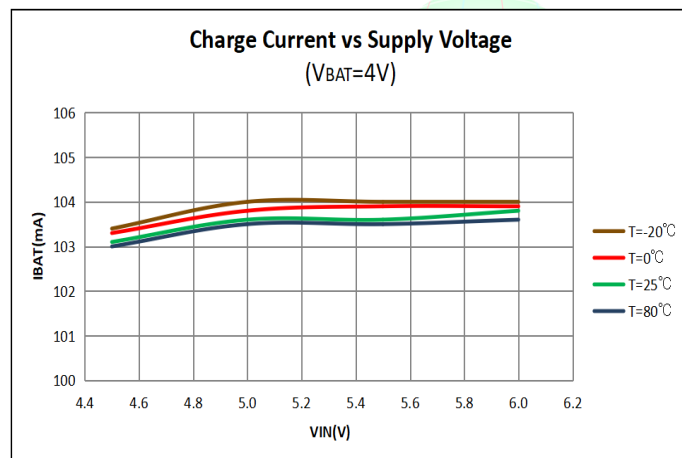
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
V _{IN}	Input Voltage		4.5	5	5.5	V
I _{IN}	Input Supply Current	R _{IS} ET=17K, Charge Mode		300		μA
		V _{BAT} =4.4V, Charge Terminated		160		μA
		R _{IS} ET=NC, Shutdown Mode		200		μA
V _{FLOAT}	Regulated Output (Float) Voltage	LP4069PQVF, I _{BAT} =40mA	4.158	4.2	4.242	V
		LP4069PQVF-435, I _{BAT} =40mA	4.307	4.35	4.394	V
		LP4069PQVF-44, I _{BAT} =40mA	4.356	4.4	4.444	V
V _{UV}	V _{IN} Under Voltage Lockout Threshold	V _{IN} Rising		3.5		V
V _{UV_HYS}	Under Voltage Lockout Hysteresis			140		mV
V _{OVP}	Input Voltage OVP	V _{IN} Rising	6	6.3	7.5	V
V _{OVP_HYS}	OVP Hysteresis			150		mV
I _{BAT}	BAT Pin Current	R _{IS} ET=3.4k, Current Mode	450	500	550	mA
		R _{IS} ET=17k, Current Mode	90	100	110	mA
		V _{BAT} =4.2V (V _{IN} =Float or 0V)		-1		μA
I _{TRIKL}	Trickle Charge Current	V _{BAT} <V _{TRIKL} , R _{IS} ET=10k, Charge Mode		40		%I _{BAT}
V _{TRIKL}	Trickle Charge Threshold Voltage	V _{BAT} Rising		2.6		V
V _{TRIKL-HYS}	Trickle Charge Hysteresis Voltage			150		mV
I _{TERM}	Termination Current Threshold			10		%I _{BAT}
V _{IS} ET	ISET Pin Voltage	R _{IS} ET=10k, Current Mode	0.9	1	1.1	V
I _{STAT}	CHRG Pin Sink Current	V _{CHRG} =5V			5	μA
V _{STAT}	CHRG Pin Output Low Voltage	I _{CHRG} =5mA			0.5	V
I _{PG}	PG Pin Sink Current	V _{CHRG} =5V			5	μA
V _{PG}	PG Pin Output Low Voltage	I _{CHRG} =5mA			0.5	V
ΔV _{RECHRG}	Recharge Battery Threshold Voltage	V _{FLOAT} -V _{RECHRG}		150		mV
V _{ASD}	V _{IN} - V _{BAT} Lockout Threshold Voltage	V _{BAT} =3.5V, V _{IN} Rising		150		mV
V _{EN_ON}	EN Logic-Low Voltage Threshold				0.4	V
V _{EN_OFF}	EN Logic-High Voltage Threshold		1.4			V
T _{LIM}	Junction Temperature in Constant Temperature Mode		145			°C

Typical Charging Profile



Typical Performance Characteristics

($C_{IN}=C_{OUT}=10\mu F$, $R_{ISET}=16.5K$, unless otherwise noted)



Application Information

The LP4069P has built-in input voltage surge protection as high as +28V. The charger IC will be automatically disabled when the input voltage is higher than 7V. A charge cycle begins when EN is high, the voltage at the IN pin rises above the UVLO threshold level and a program resistor is connected from the ISET pin to ground. If the BAT pin is less than 2.6V, the charger enters trickle charge mode. In this mode, the LP4069P supplies approximately 4/10 the ISET programmed charge current to bring the battery voltage up to a safe level for full current charging. When the BAT pin voltage rises above 2.6V, the charger enters constant-current mode(CC), where the ISET programmed charge current is supplied to the battery. When the Battery Voltage approaches the final float voltage, It enters constant-voltage mode(CV) and the charge current begins to decrease, and the battery full indication is set when the charge current in the CV mode is reduced to the programmed full battery current (1/10).

Charge Termination

A charge cycle is terminated when the charge current falls to 1/10th the ISET programmed value after the final float voltage is reached. This condition is detected by using an internal, filtered comparator to monitor the ISET pin. When the ISET pin voltage falls below 100mV for longer than t_{TERM} (typically 1ms), charging is terminated.

Charge Current Program

The charge current (I_{BAT}) is set by a resistor (R_{ISET}) connecting from the ISET pin to GND. The relationship of the charge current and the programming resistance is established by the following equations ($V_{ISET}=1V$).

$$I_{BAT} = \frac{1700 \times V_{ISET}}{R_{ISET}}$$

Automatic Recharge

Once the charge cycle is terminated, the LP4069P continuously monitors the voltage on the BAT pin. A charge cycle restarts when the battery voltage falls below 4.05V (which corresponds to approximately 80% to 90% battery capacity). This ensures that the battery is kept at or near a fully charged condition and eliminates the need for periodic charge cycle initiations.

Charge Status Indicator (CHRG/PG)

When the input voltage is above the UVLO and above the battery voltage +150mV($V_{IN}>V_{BAT}+150mV$), and lower than OVP ($V_{IN}<V_{OVP}$), the PG internal NMOS turns on and provides a low impedance path to ground.

Function	PG
$V_{IN}<V_{UVLO}$	Hi-Z
$V_{UVLO}<V_{IN}<V_{OVP}$	Low
$V_{OVP}<V_{IN}$	Hi-Z

CHRG has two different states: pull-down ~5mA maximum sink current) to GND and high impedance. The pull-down state indicates that the LP4069P is in a charge cycle. when the charge current decreases to the battery termination charge current threshold (IBF) ,the CHRG pin will become high impedance. After application of a 5V source, the input

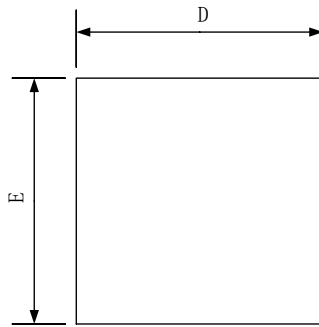
Function	CHRG	FULL
Charging	Low	Hi-Z
Charge Finish	Hi-Z	Low

Thermal Limit

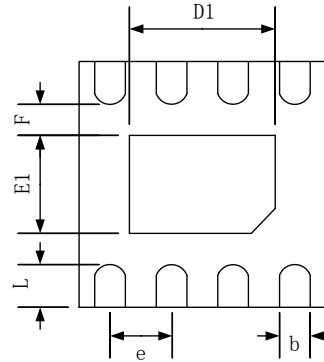
An internal thermal feedback loop reduces charge current if junction temperature attempts to rise above a preset value of approximately 145°C. This feature protects the device from excessive temperature and allows the user to push the limits of the power handling capability of a given circuit board without risk of damaging the device. The charge current can be set according to typical (not worst-case) ambient temperature with the assurance that the charger will automatically reduce the current in worst-case conditions.

Packaging Information

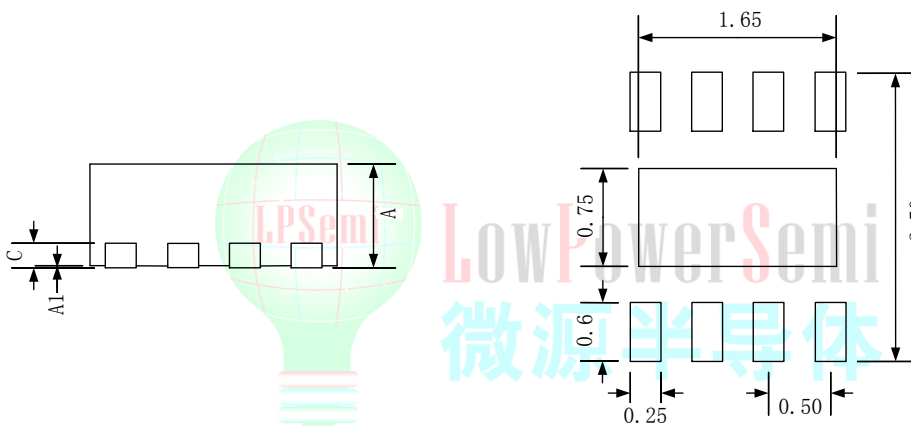
TDFN-8



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Recommended Land Pattern

SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
c	0.20 REF		
D	1.90	2.00	2.10
D1	1.10	1.30	1.65
E	1.90	2.00	2.10
E1	0.60	0.75	0.85
e	0.50 BSC		
L	0.25	0.35	0.40
F	0.25	0.30	0.35