

Features

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

B_{vds}

30V

R_{dson}

1.4mΩ

I_D

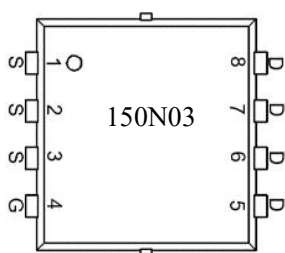
150A

Application

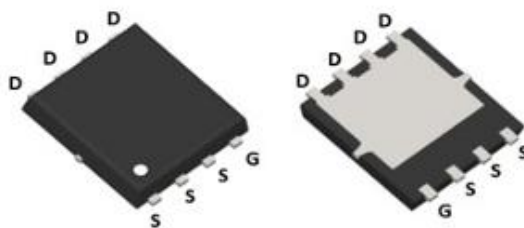
- DC-DC Converters
- Power management functions
- Synchronous-rectification applications

RoHS

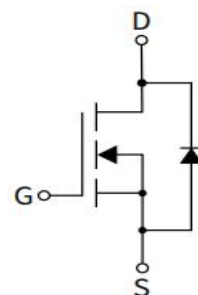
Package



Marking and pin assignment



PDFN3x3-8L top view



Schematic diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Quantity
150N03	S150N03D	PDFN3x3-8L	5000

Absolute Maximum Ratings ($T_J=25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	$T_C=25^{\circ}\text{C}$ I_D	150	A
	$T_C=100^{\circ}\text{C}$ I_D	95	A
Pulsed Drain Current ¹	I_{DM}	600	A
Single Pulsed Avalanche Energy ²	EAS	180	mJ
Avalanche Current	I_{AS}	-	A
Total Power Dissipation	$P_D@T_C=25^{\circ}\text{C}$	66	W
Operating Junction Temperature Range	T_J	$-55 \sim +150$	$^{\circ}\text{C}$
Storage Temperature Range	T_{STG}	$-55 \sim +150$	$^{\circ}\text{C}$



Thermal Resistance Ratings

Parameter	Symbol	Typ.	Max.	Unit
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	--	1.9	$^{\circ}\text{C/W}$
Thermal Resistance Junction-to-Ambient ³	$R_{\theta JA}$	--	60	$^{\circ}\text{C/W}$

Ordering Information

Ordering Number	Package	Pin Assignment			Packing
Halogen Free		G	D	S	
HL150N03D	PDFN3x3-8L	4	5,6,7,8	1,2,3	Tape Reel

Electrical Characteristics ($T_J=25^{\circ}\text{C}$, unless otherwise specified)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	30	-	-	V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=30V, V_{GS}=0V, T_J=25^{\circ}\text{C}$	-	-	1	μA
		$V_{DS}=30V, V_{GS}=0V, T_J=100^{\circ}\text{C}$	-	-	100	μA
Gate-Source Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$	-	-	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.2	1.7	2.2	V
Static Drain-Source On-Resistance ⁴	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$	-	1.4	1.9	m Ω
		$V_{GS}=4.5V, I_D=15A$	-	2.1	2.8	
Forward Transconductance ⁴	g_{fs}	$V_{DS}=10V, I_D=20A$	-	85	-	S
Gate Resistance	R_g	$f=1\text{MHz}$	-	0.98	-	Ω
Input Capacitance	C_{iss}	$V_{DS}=15V, V_{GS}=0V,$ $f=1\text{MHz}$	-	2554	-	pF
Output Capacitance	C_{oss}		-	924	-	
Reverse Transfer Capacitance	C_{rss}		-	73.5	-	
Total Gate Charge	Q_g	$V_{DS}=15V, V_{GS}=10V,$ $I_D=20A$	-	39.1	-	nC
Gate-Source Charge	Q_{gs}		-	6.7	-	
Gate-Drain Charge	Q_{gd}		-	5.9	-	
Turn-on Delay Time	$T_{d(on)}$	$V_{GS}=10V, V_{DD}=15V,$ $R_G=3\Omega, I_D=20A$	-	10	-	nS
Turn-on Rise Time	T_r		-	7.3	-	
Turn-Off Delay Time	$T_{d(off)}$		-	38.6	-	
Turn-Off Fall Time	T_f		-	16.4	-	
Continuous Source Current	I_S	-	-	-	150	A
Pulsed Source Current	I_{SM}		-	-	-	A
Diode Forward Voltage ⁴	V_{SD}	$V_{GS}=0V, I_S=20A$	-	-	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F=20A, dI/dt=100A/\mu s$	-	54	-	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	27	-	nC

Notes:

1. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=150^{\circ}\text{C}$.
2. The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.4\text{mH}, I_{AS}=30A$.

3. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
5. This value is guaranteed by design hence it is not included in the production test.

Typical Performance Characteristics

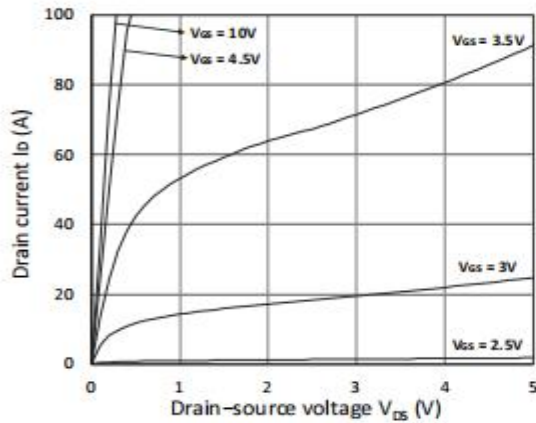


Figure 1. Output Characteristics

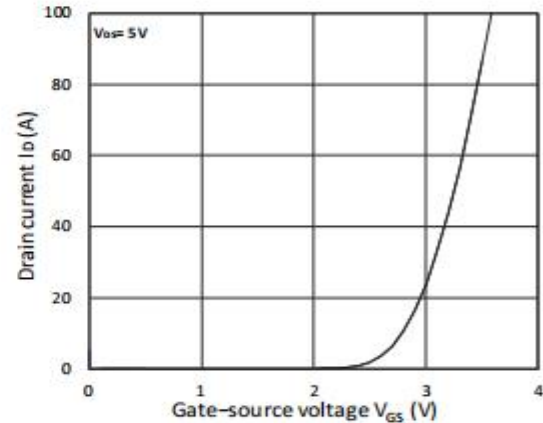


Figure 2. Transfer Characteristics

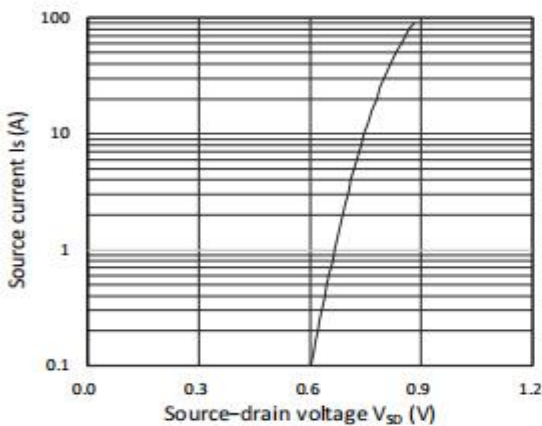


Figure 3. Forward Characteristics of Reverse

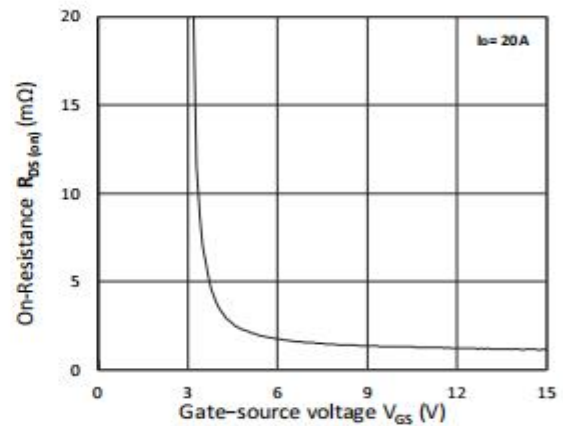


Figure 4. $R_{DS(ON)}$ vs. V_{GS}

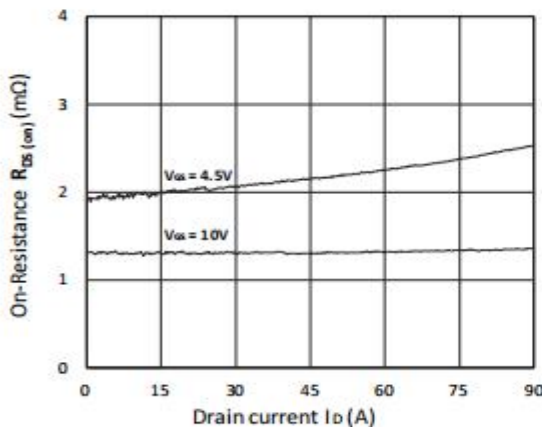


Figure 5. $R_{DS(ON)}$ vs. I_D

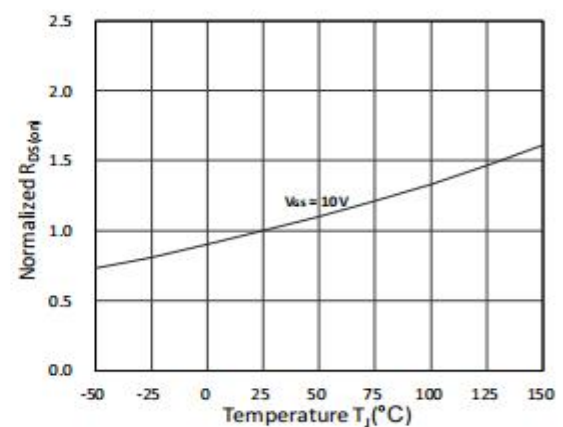


Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

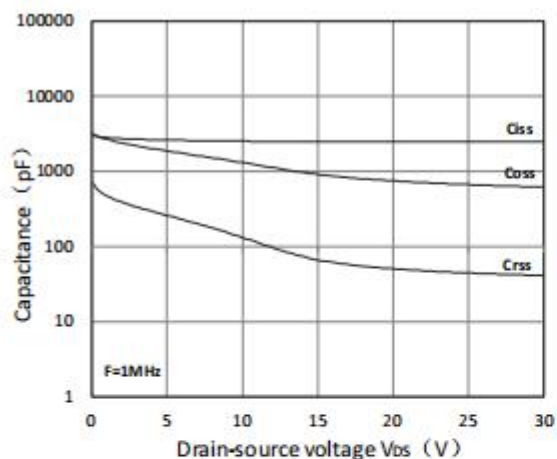


Figure 7. Capacitance Characteristics

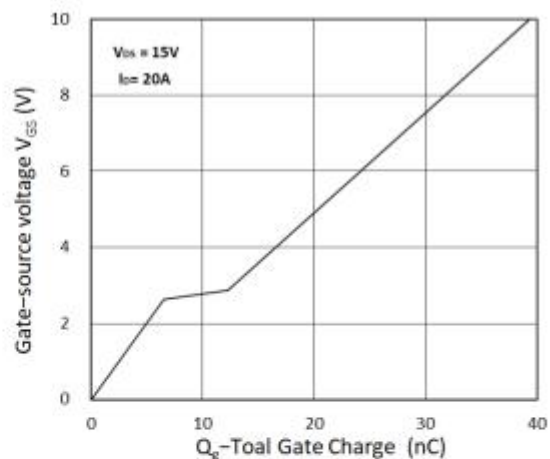


Figure 8. Gate Charge Characteristics

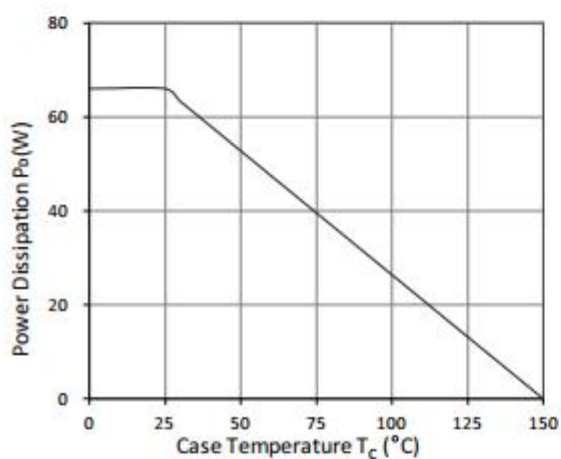


Figure 9. Power Dissipation

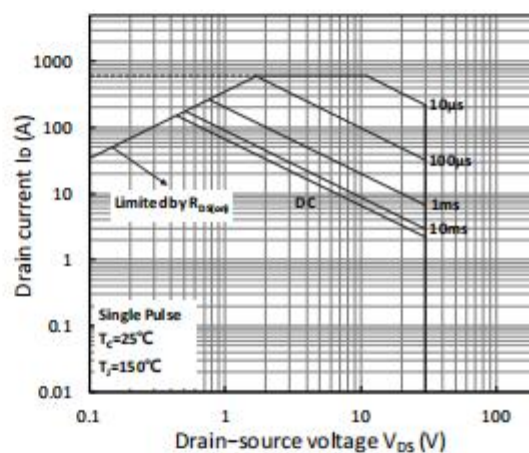


Figure 10. Safe Operating Area

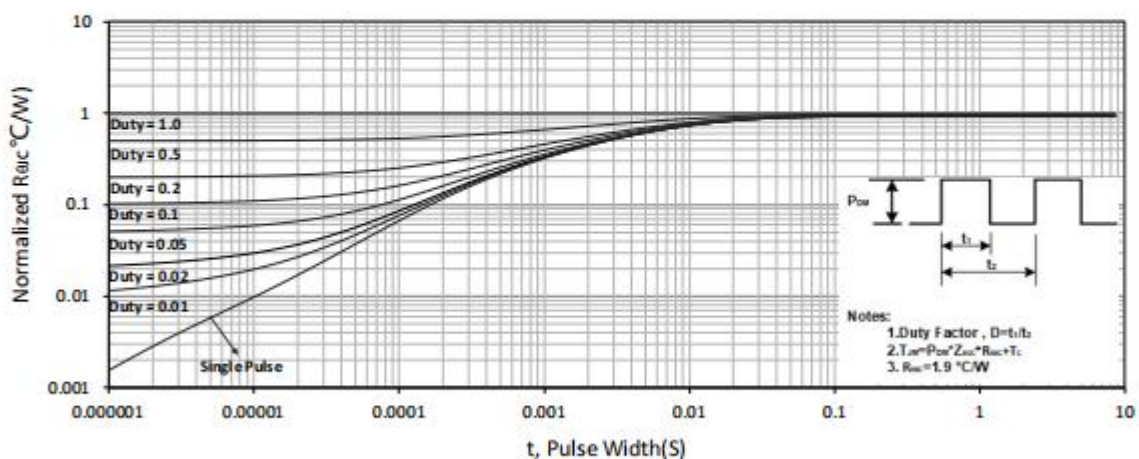


Figure 11. Normalized Maximum Transient Thermal Impedance

Test Circuit

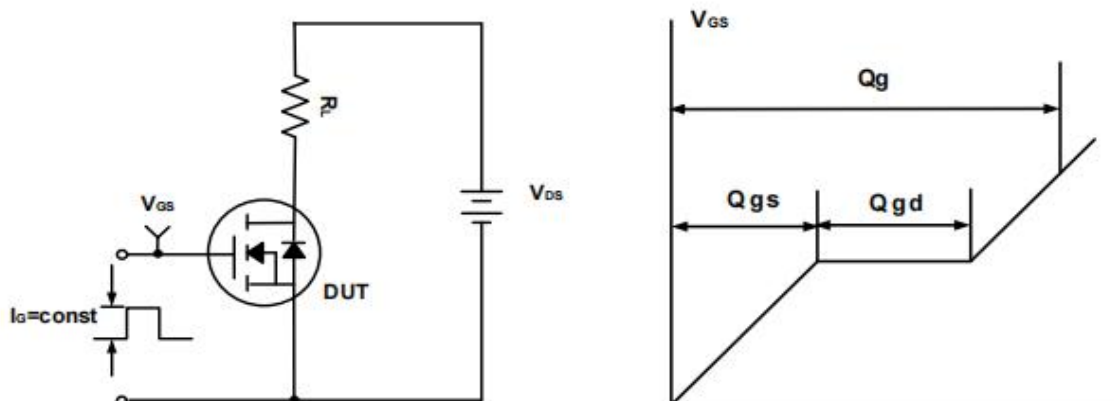


Figure A. Gate Charge Test Circuit & Waveforms

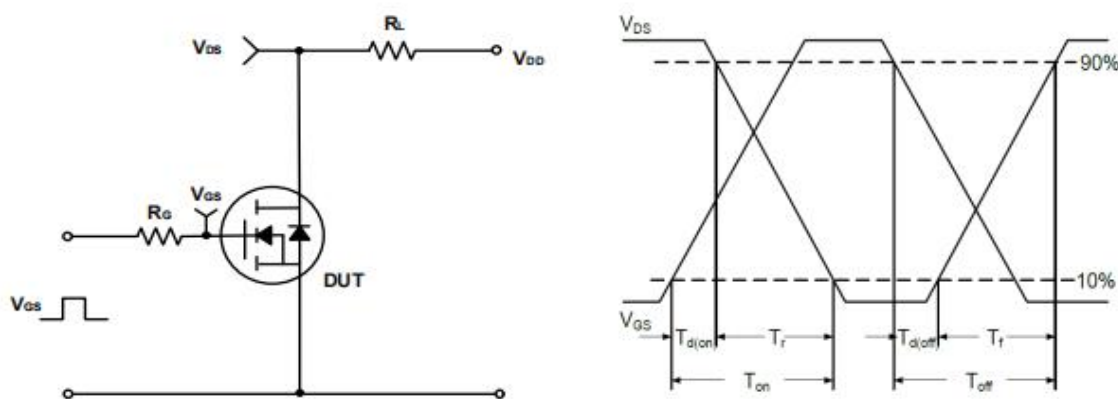


Figure B. Switching Test Circuit & Waveforms

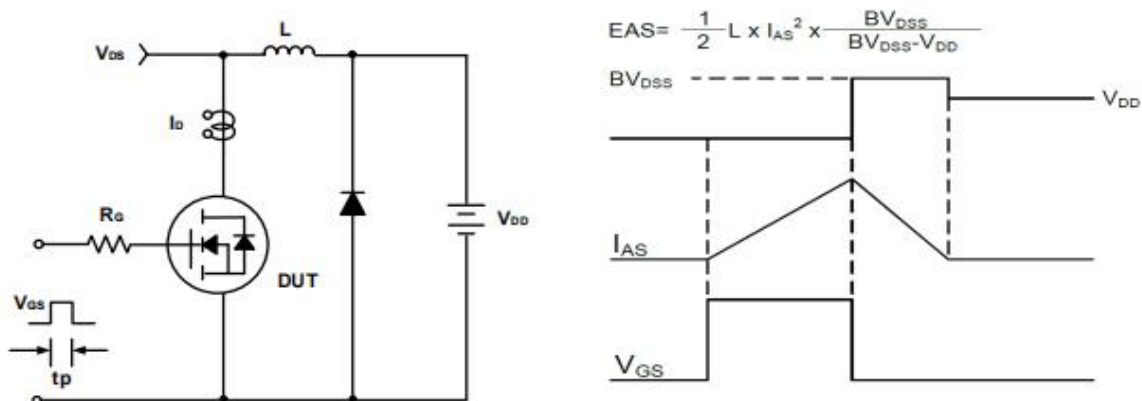
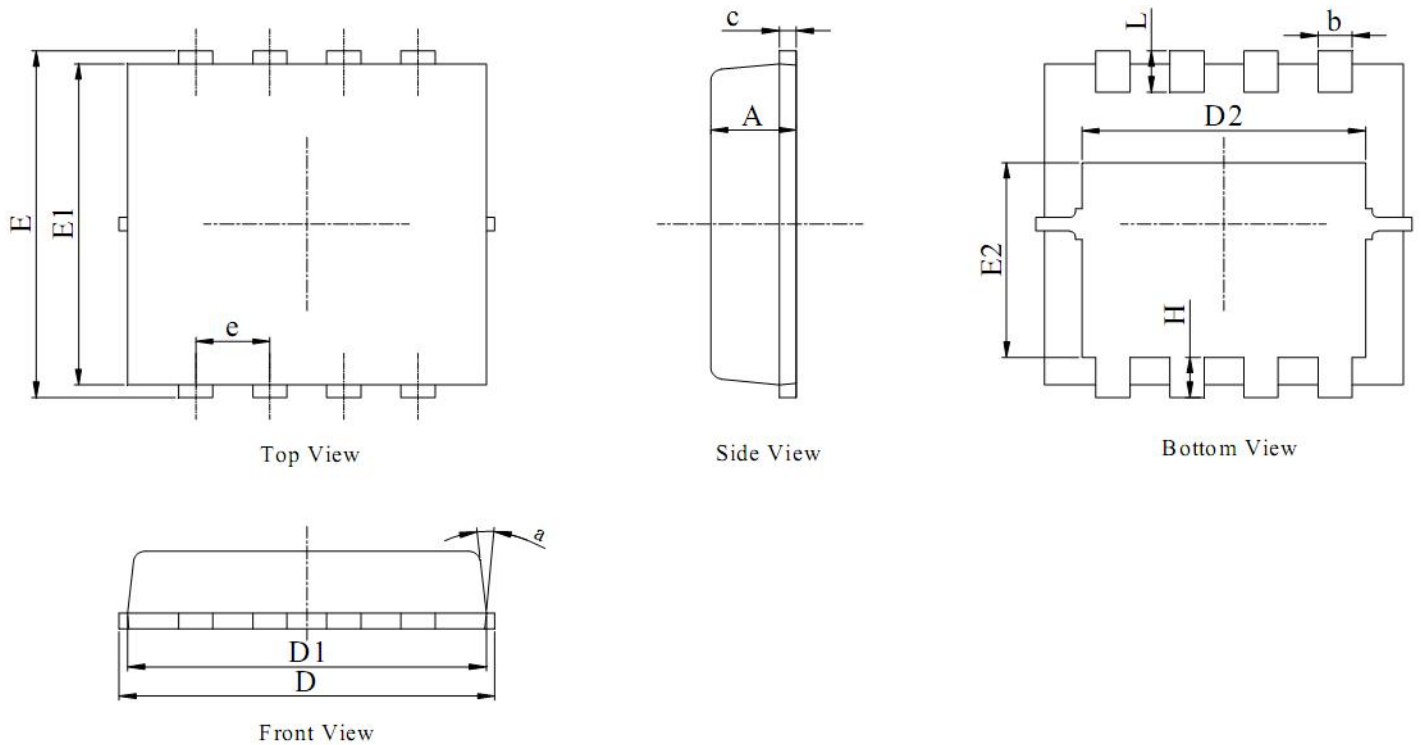


Figure C. Unclamped Inductive Switching Circuit & Waveforms



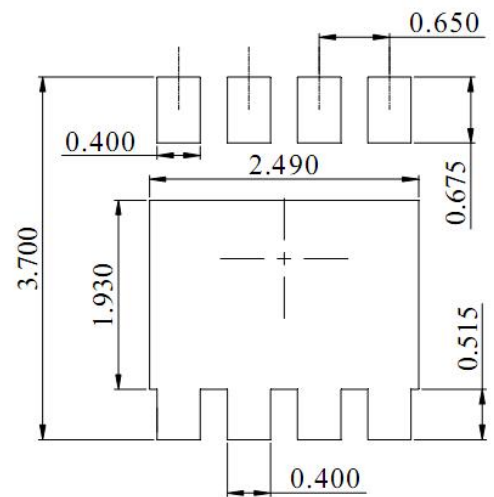
Package Mechanical Data PDFN3x3-8L



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. ALL DIMNESIONS IN MILLIMETER (ANNGLE IN DEGREE).
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM.	MILLIMETER		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.20	0.25
D	3.00	3.15	3.25
D1	2.95	3.05	3.15
D2	2.39	2.49	2.59
E	3.20	3.30	3.40
E1	2.95	3.05	3.15
E2	1.70	1.80	1.90
e	0.65 BSC		
H	0.30	0.40	0.50
L	0.25	0.40	0.50
a	---	---	15°



DIMENSIONS:MILLIMETERS



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