Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

Applications

- Power management in half bridge and inverters
- DC-DC Converter
- Load Switch

General Description

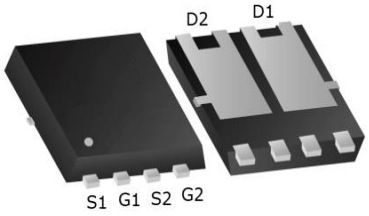
The XR30G15D is the highest performance trenchN-ch and P-ch MOSFETs with extreme high cell density , which provide excellent RDSON and gate charge for most of the synchronous buck converter applications .

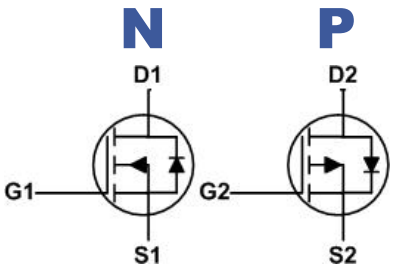
The XR30G15D meet the RoHS and Green Product requirement , 100% EAS guaranteedwith full function reliability approved.

Product Summary

BVDSS	RDSON	ID
30V	16mΩ	15A
-30V	33mΩ	-12A

PDFN3333-8L Pin Configuration





Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-Channel	P-Channel	
V_{DS}	Drain-Source Voltage	30	-30	V
V_{GS}	Gate-Source Voltage	±20	±20	V
I_D@T_C=25℃	Continuous Drain Current, V_{GS} @ 10V[1]	15	-12	A
I_D@T_C=100℃	Continuous Drain Current, V_{GS} @ 10V[1]	12	-8	A
I_{DM}	Pulsed Drain Current[2]	42	-24	A
EAS	Single Pulse Avalanche Energy[3]	72	59	mJ
I_{AS}	Avalanche Current	21	-19	A
P_D@T_C=25℃	Total Power Dissipation[4]	2.5	2.08	W
T_{STG}	Storage Temperature Range	-55 to 150	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	-55 to 150	℃

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient [1]	---	85	℃/W
$R_{\theta JC}$	Thermal Resistance Junction-Case[1]	---	50	℃/W

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250uA	30	---	---	V
$\triangle BV_{DSS}/\triangle T_J$	BVDSS Temperature Coefficient	Reference to 25℃ , I_D=1mA	---	0.034	---	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V , I_D=13A	---	16	23	mΩ
		V_{GS}=4.5V , I_D=10A	---	23	32	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =250uA	1.0	1.5	2.5	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-5.8	---	mV/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=30V , V_{GS}=0V , T_J=25℃	---	---	1	uA
		V_{DS}=30V , V_{GS}=0V , T_J=55℃	---	---	5	
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=15V , I_D=10A	---	10	---	S
R_g	Gate Resistance	V_{DS}=24V , V_{GS}=0V , f=1MHz	---	2.5	---	Ω
Q_g	Total Gate Charge (4.5V)	V_{DS}=20V , V_{GS}=4.5V , I_D=13A	---	7.2	---	nC
Q_{gs}	Gate-Source Charge		---	1.4	---	
Q_{gd}	Gate-Drain Charge		---	2.2	---	
$T_{d(on)}$	Turn-On Delay Time	V_{DD}=12V , V_{GS}=10V , R_G=3.3Ω I_D=10A	---	3.9	---	ns
T_r	Rise Time		---	9.2	---	
$T_{d(off)}$	Turn-Off Delay Time		---	14.5	---	
T_f	Fall Time		---	6.0	---	
C_{iss}	Input Capacitance	V_{DS}=25V , V_{GS}=0V , f=1MHz	---	370	---	pF
C_{oss}	Output Capacitance		---	54	---	
C_{rss}	Reverse Transfer Capacitance		---	40	---	

Guaranteed Avalanche Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
EAS	Single Pulse Avalanche Energy[5]	V_{DD}=25V , L=0.1mH , I_{AS}=21A	16	---	---	mJ

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current[1,6]	V_G=V_D=0V , Force Current	---	---	15	A
I_{SM}	Pulsed Source Current[2,6]		---	---	40	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V , I_S=10A , T_J=25℃	---	---	1.2	V

Note :
1. The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper,t<10sec.
2. The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3. The EAS data shows Max. rating . The test condition is V_{DD}=25V,V_{GS}=10V,L=0.1mH,I_{AS}=21A
4. The power dissipation is limited by 150℃ junction temperature
5. The Min. value is 100% EAS tested guarantee.
6. The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Static Characteristics						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}= 0V, I_D= -250μA	-30	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}= -30V, V_{GS}= 0V	-	-	-1	μA
Gate-Source Leakage	I_{GSS}	V_{DS}= 0V, V_{GS}= ±20V	-	-	±100	nA
Gate-Source Threshold voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D= -250μA	-1	-1.5	-2.5	V
Drain-Source on-State Resistance[3]	$R_{DS(on)}$	V_{GS}= -10V, I_D= -8.2A	-	33	44	mΩ
		V_{GS}= -4.5V, I_D= -6A	-	46	64	
Dynamic Characteristics[4]						
Input Capacitance	C_{iss}	V_{GS} = 0V , V_{DS} = -15V, f = 1.0MHz	-	530	-	pF
Output Capacitance	C_{oss}		-	70	-	
Reverse Transfer Capacitance	C_{rss}		-	56	-	
Switching Characteristics[4]						
Total Gate Charge	Q_g	V_{GS} = -10V, V_{DS} = -15V, I_D = -8.2A	-	6.8	-	nC
Gate−Source Charge	Q_{gs}		-	1.0	-	
Gate−Drain Charge	Q_{gd}		-	1.4	-	
Turn-on Delay Time	$t_{d(on)}$	V_{GS}= -10V, V_{DS}= -15V , R_L= 15Ω,R_{GEN}= 2.5Ω	-	14	-	ns
Rise Time	t_r		-	61	-	
Turn-off Delay time	$t_{d(off)}$		-	19	-	
Fall Time	t_f		-	10	-	
Source-Drain Body Diode Characteristics						
Diode Forward Voltage[3]	V_{SD}	I_S = -1A, V_{GS} = 0V	-	-	-1.2	V
Continuous Source Current	I_S		-	-	-12	A

Notes:

1. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C.
2. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
3. Pulse Test: Pulse width≤300μs, duty cycle≤2%.
4. This value is guaranteed by design hence it is not included in the production test.

N-Channel Typical Characteristics

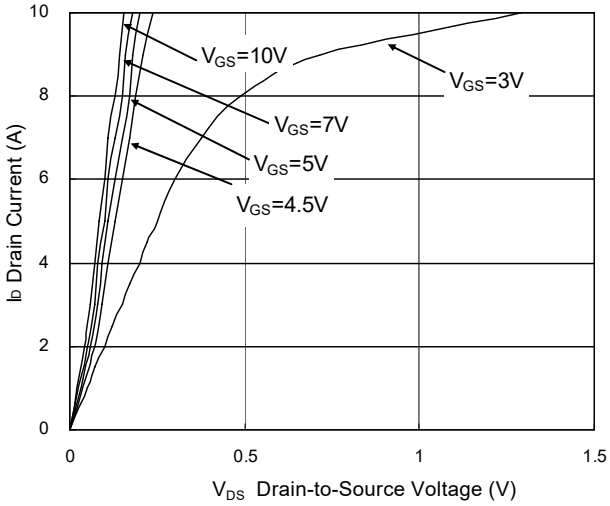


Fig.1 Typical Output Characteristics

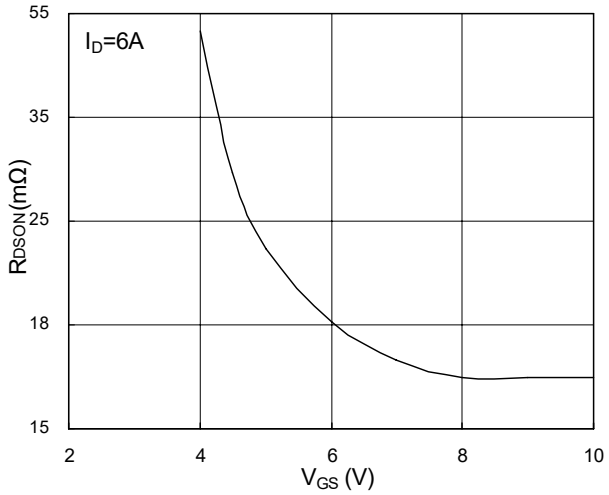


Fig.2 On-Resistance vs. G-S Voltage

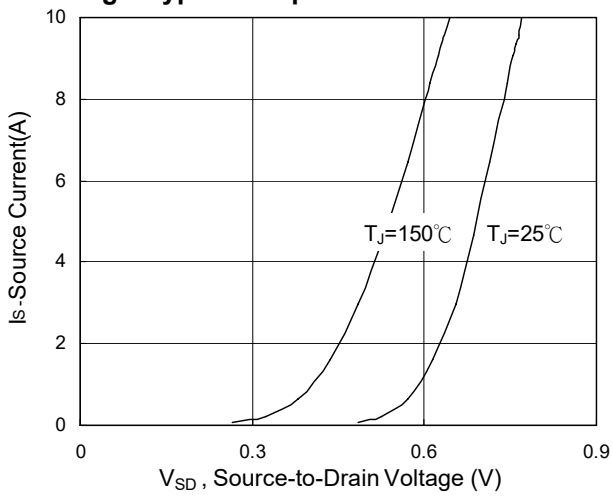


Fig.3 Forward Characteristics of Reverse

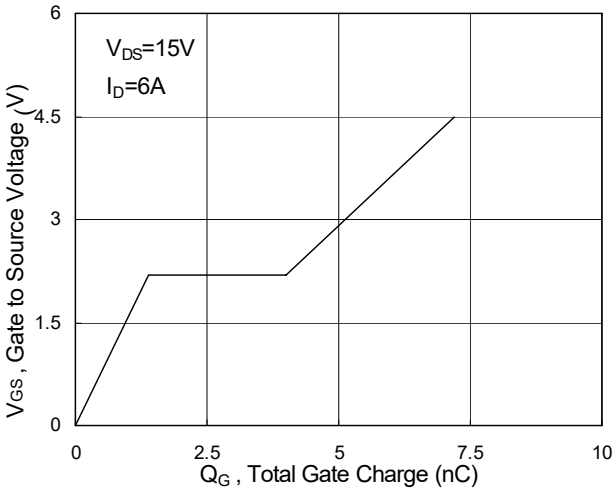
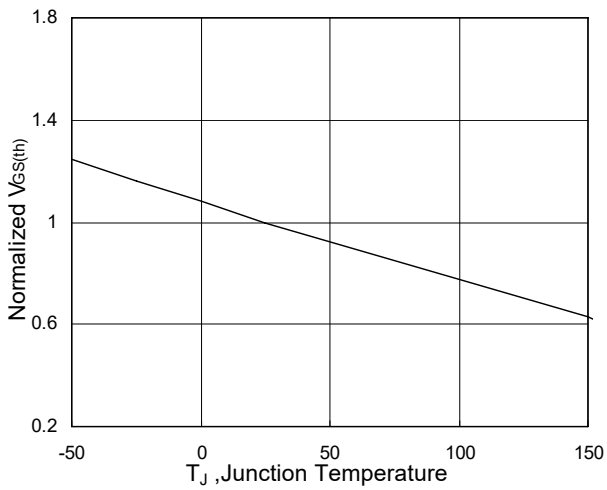


Fig.4 Gate-charge Characteristics



(℃) Fig.5 $V_{GS(th)}$ vs. T_J

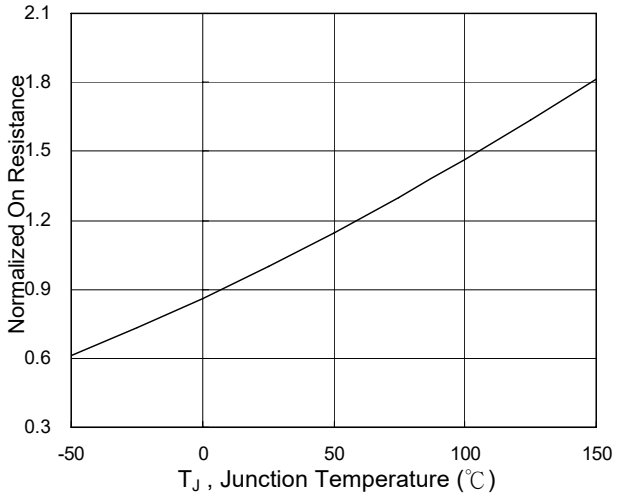


Fig.6 Normalized R_{DSON} vs. T_J

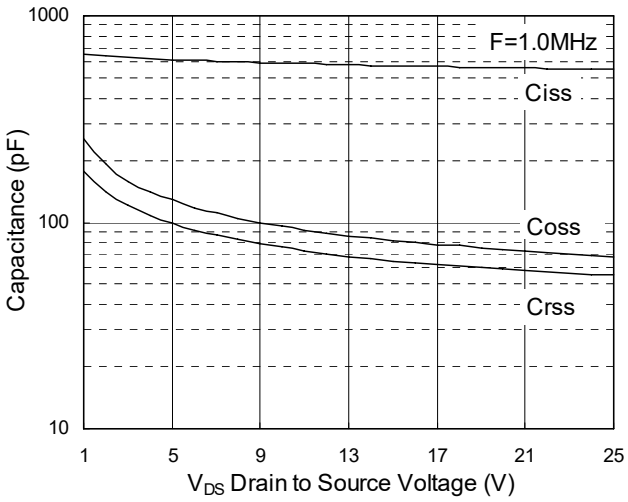


Fig.7 Capacitance

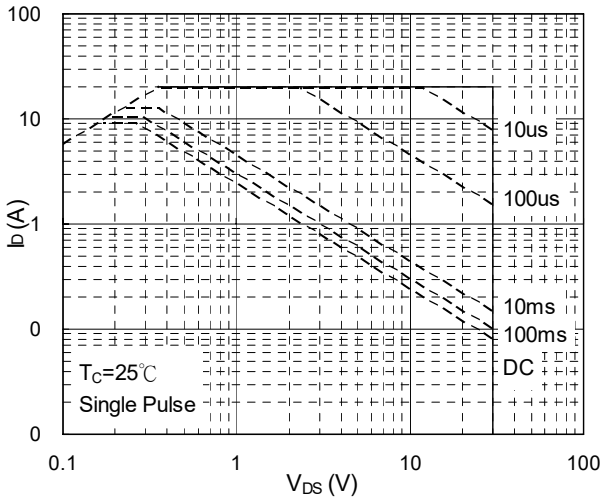


Fig.8 Safe Operating Area

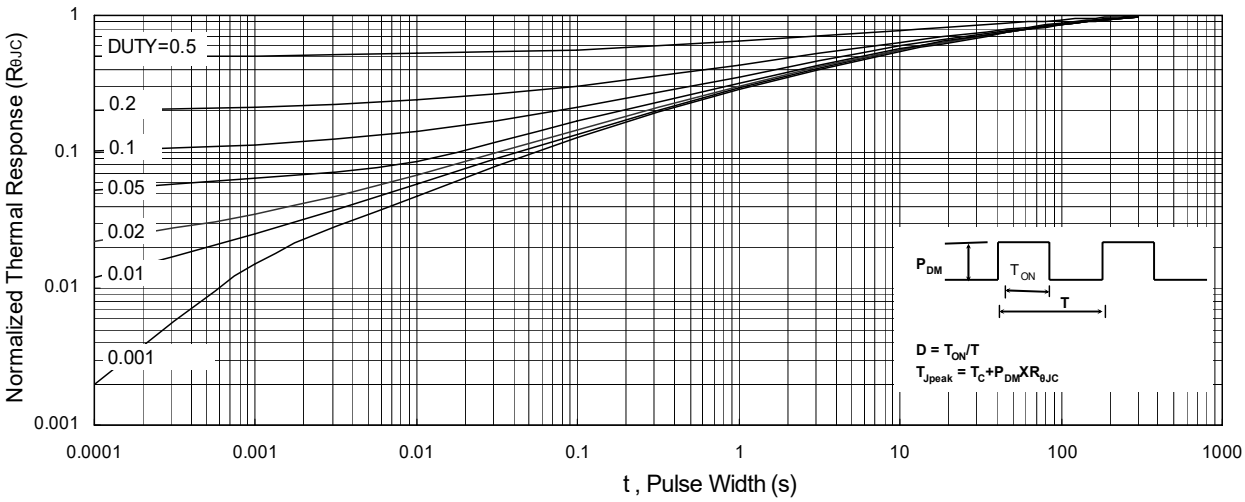


Fig.9 Normalized Maximum Transient Thermal Impedance

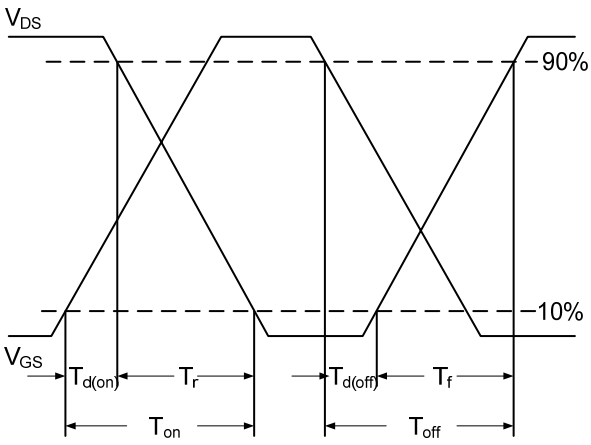


Fig.10 Switching Time Waveform

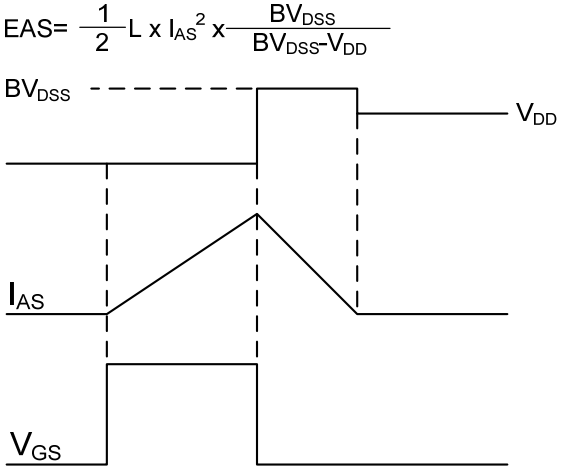


Fig.11 Unclamped Inductive Waveform

P-Channel Typical Characteristics

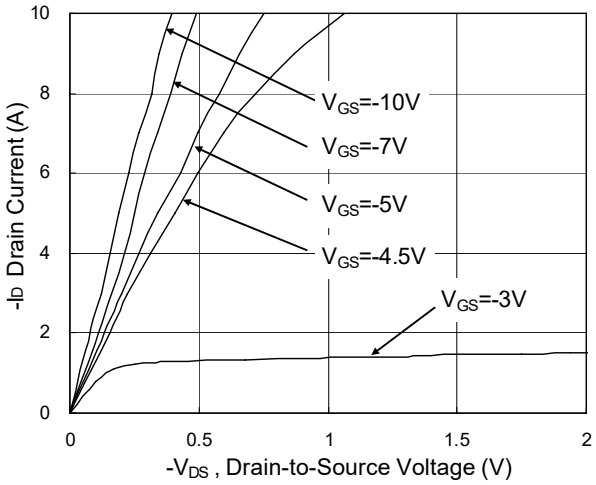


Fig.1 Typical Output Characteristics

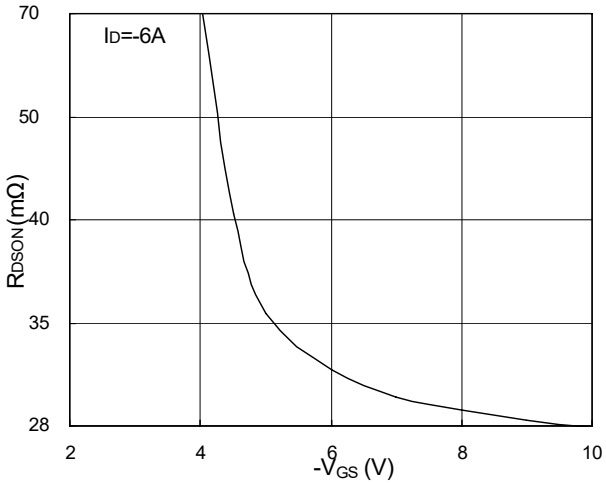


Fig.2 On-Resistance vs. Gate-Source

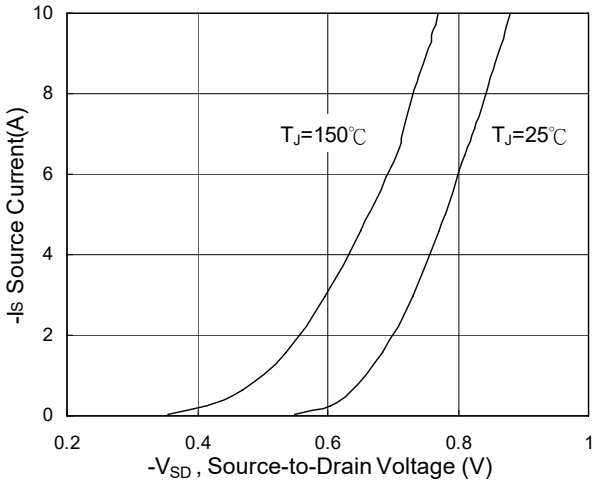


Fig.3 Forward Characteristics of Reverse

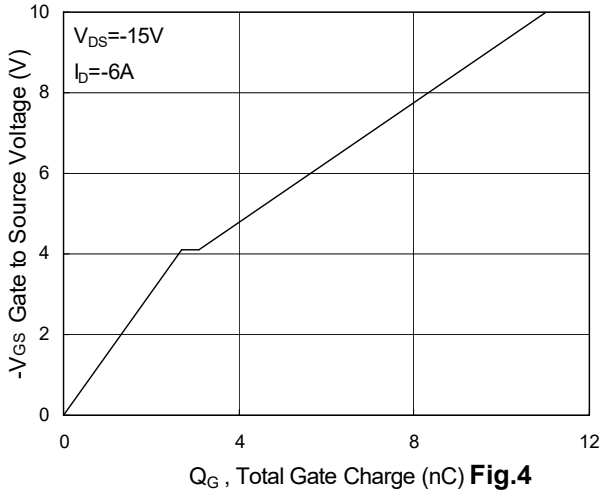


Fig.4 Gate-charge Characteristics

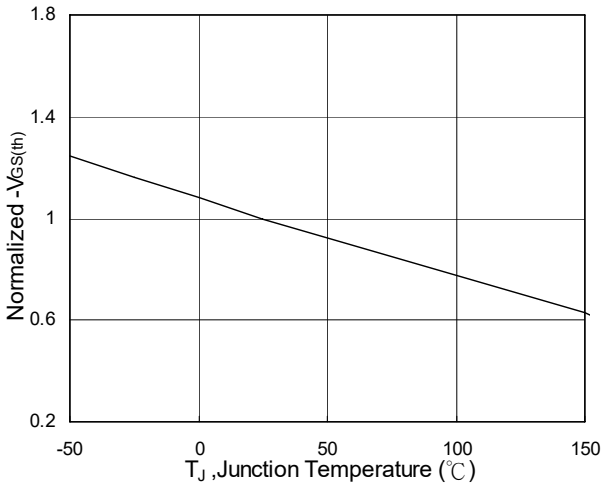


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

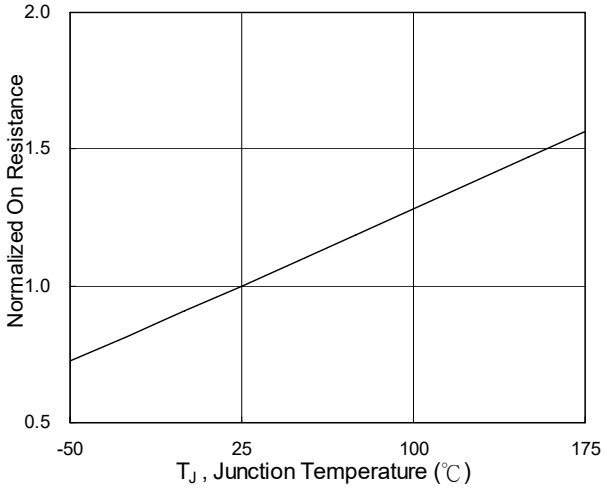


Fig.6 Normalized R_{DSON} vs. T_J

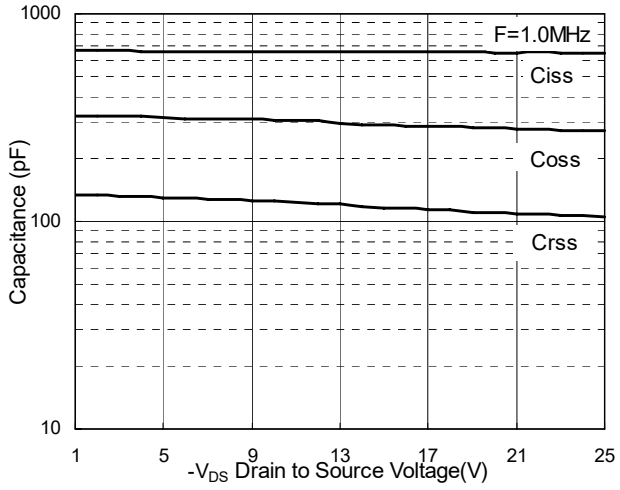


Fig.7 Capacitance

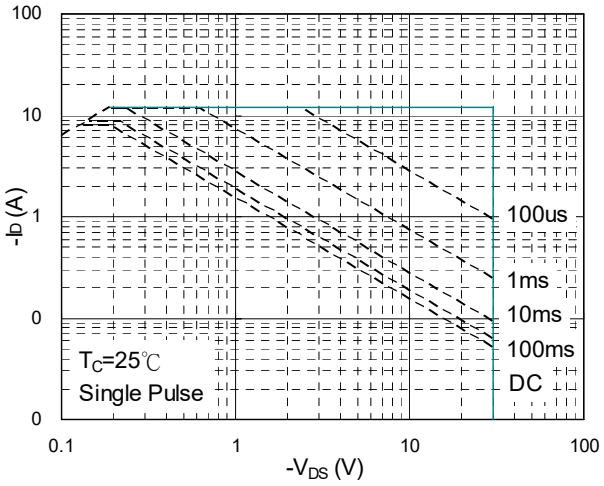


Fig.8 Safe Operating Area

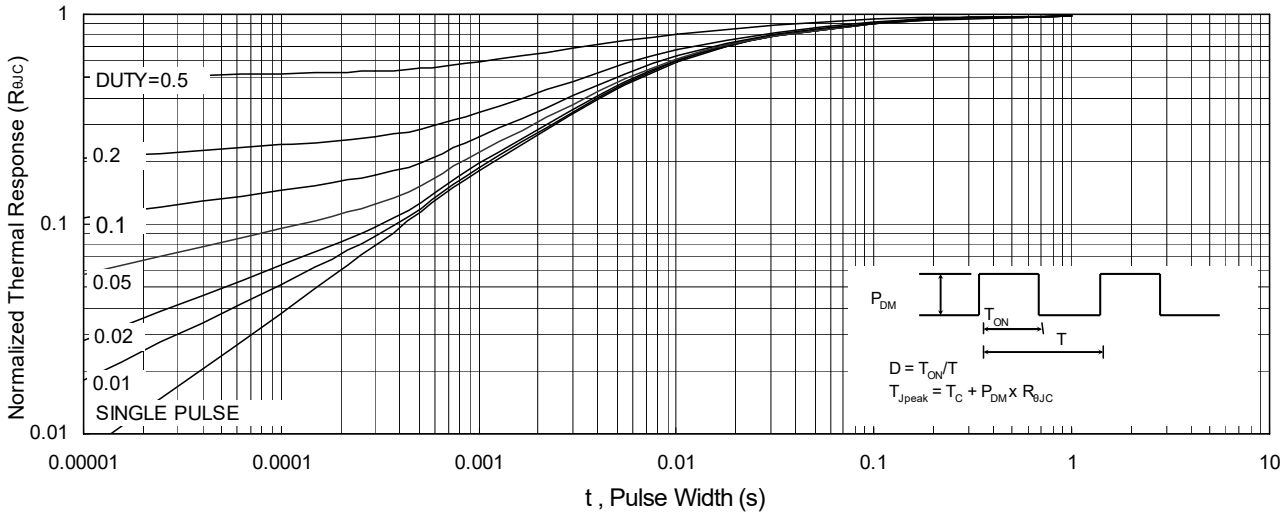


Fig.9 Normalized Maximum Transient Thermal Impedance

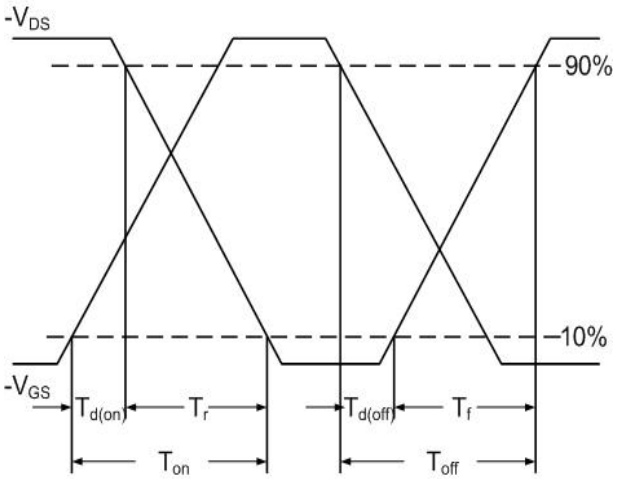


Fig.10 Switching Time Waveform

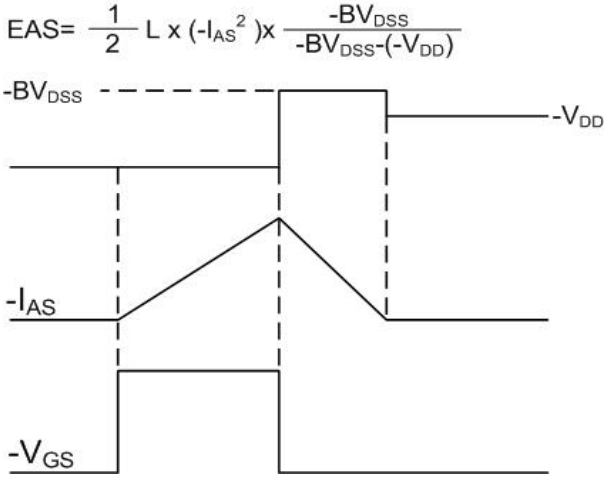
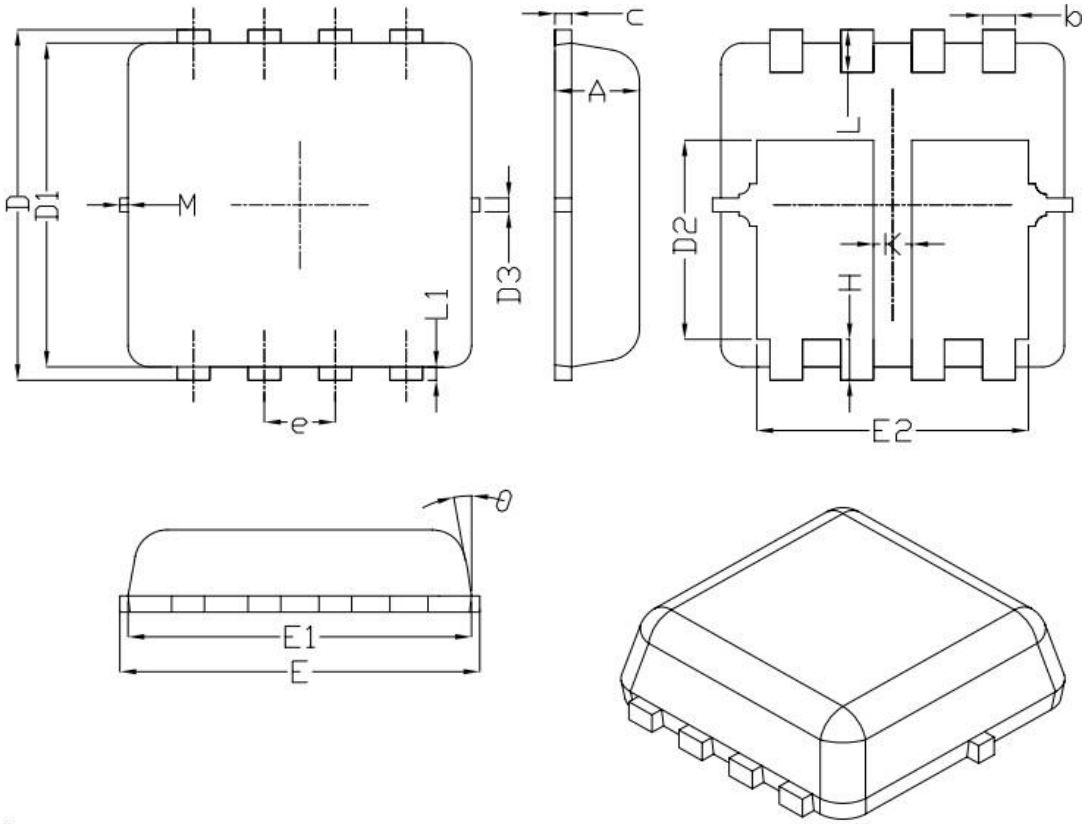


Fig.11 Unclamped Inductive Waveform

Dual PDFN3333-8L Package Outline Data



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.78	1.88	1.98
D3	--	0.13	--
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65 BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	--	0.13	--
K	0.30	--	--
θ	--	10°	12°
M	*	*	0.15
* Not Specified			

Notes:
1. Refer to JEDEC MO-240 variation CA.
2. Dimensions "D1" and "E1" do NOT include mold flash protrusions or gate burrs.
3. Dimensions "D1" and "E1" include interterminal flash or protrusion.