Low-power Configurable Multiple Function Gate

General Description

The SN74LVC1G57 is a configurable multiple function gate with Schmitt-trigger inputs. The device can be configured as any of the following logic functions AND, OR, NAND, NOR, XNOR, inverter and buffer; using the 3-bit input. All inputs can be connected directly to V_{CC} or GND. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging back-flow current through the device when it is powered down.

Features

- Wide Supply Voltage Range from 1.65 V to 5.5 V
- Over-voltage Tolerant Inputs to 5.5 V
- High Noise Immunity
- ±24 mA Output Drive (V_{CC} = 3.0 V)
- CMOS Low Power Dissipation
- Latch-up Performance Exceeds 250 mA
- Direct Interface with TTL Levels
- I_{OFF} Circuitry Provides Partial Power-down Mode Operation
- Complies with JEDEC Standard:
  - --JESD8-7 (1.65 V to 1.95 V)
  - --JESD8-5 (2.3 V to 2.7 V)
  - --JESD8B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - --HBM JESD22-A114 exceeds 2000 V
  - --CDM JESD22-C101 exceeds 200 V
- Multiple Package Options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

Applications

- Active Noise Cancellation (ANC)
- Bar-code Scanners
- Blood Pressure Monitors
- CPAP Machines
- Cable Solutions
- Embedded PCs
- Field Transmitter: Temperature or Pressure Sensors
- HVAC: Heating, Ventilating and Air Conditioning
- TVs: High-Definition (HDTV), LCD and Digital
- Video Communications Systems

Pin Configuration

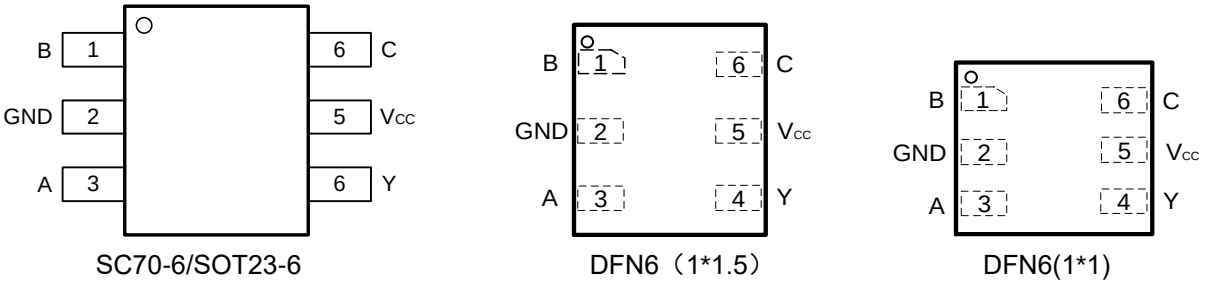


Fig1. Top View

Pin Function

Pin No. 74LVC1G57DCK /DBV/DSF/DRY	Pin Name	Pin Function
1	B	Data Input
2	GND	Ground (0 V)
3	A	Data Input
4	Y	Data Input
5	V_{CC}	Supply Voltage
6	C	Data Input

Block Diagram

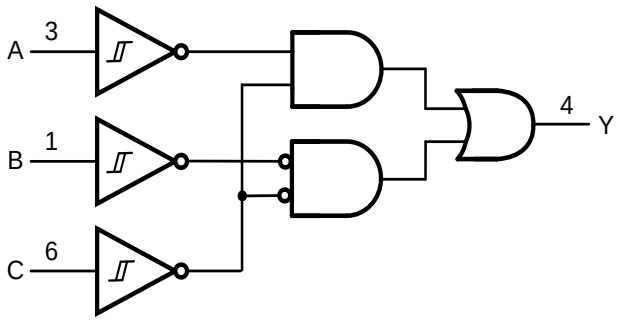


Fig 2. Logic Symbol

Functional Description

Function Table

H = HIGH voltage level; L = LOW voltage level.

Input			Output
C	**B**	**A**	**Y**
L	L	L	H
L	L	H	L
L	H	L	H
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	H
H	H	H	H

Function Selection Table

Logic function	Figure
2-input AND	See Fig 3.
2-input AND with both Inputs Inverted	See Fig 6.
2-input NAND with Inverted Input	See Fig 4. and Fig 5.
2-input OR with Inverted Input	See Fig 4. and Fig 5.
2-input NOR	See Fig 6.
2-input NOR with both Inputs Inverted	See Fig 3.
2-input XNOR	See Fig 7.
Inverter	See Fig 8.
Buffer	See Fig 9.

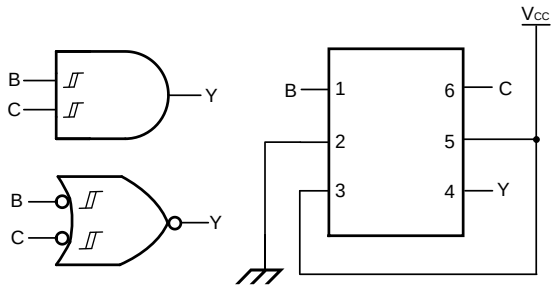


Fig3. 2-input AND gate or
2-input NOR gate with both inputs inverted

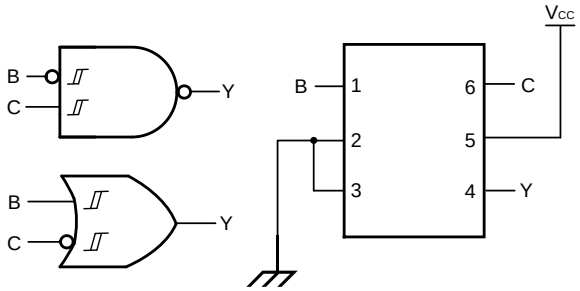


Fig4. 2-input NAND gate with input B inverted or
2-input OR gate with inverted C input

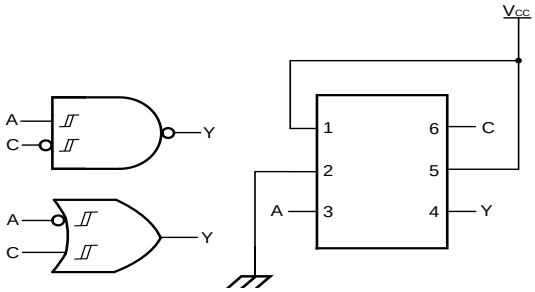


Fig5. 2-input NAND gate with input C inverted or
2-input OR gate with inverted A input

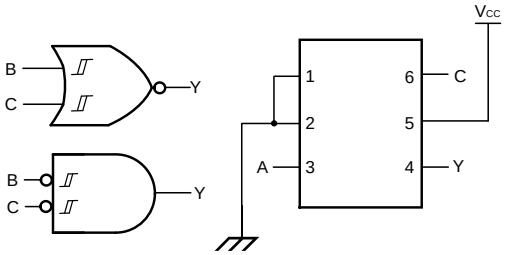


Fig6. 2-input NOR gate or
2-input AND gate with both inputs inverted

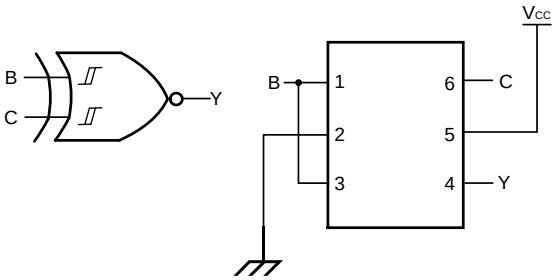


Fig7. 2-input XNOR gate

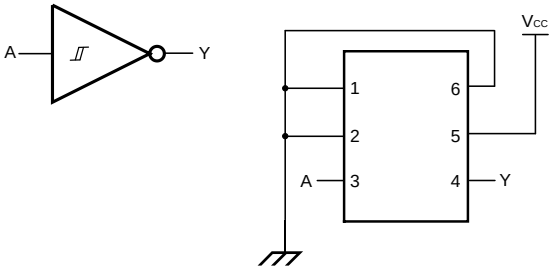
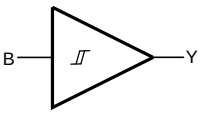


Fig8. Inverter



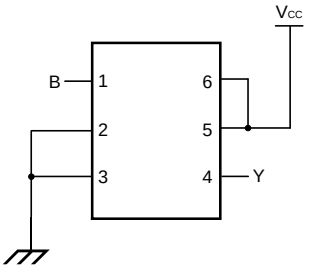


Fig 9. Buffer

Absolute Maximum Ratings

Symbol	Parameters	Conditions	Value	Unit
V_{CC}	DC Supply Voltage		-0.5 to 6.5	V
I_{IK}	Input Clamping Current		-50	mA
V_I	Input Voltage(1)	V_I < 0 V	-0.5 to 6.5	V
I_{OK}	Output Clamping Current	V_O > V_{CC} or V_O < 0 V	±50	mA
V_O	Output Voltage(1)	V_O > V_{CC} or V_O < 0 V	-0.5 to 6.5	V
		Power-down mode; V_{CC} = 0 V	-0.5 to 6.5	V
I_O	Output Current	V_O = 0 V to V_{CC}	±50	mA
I_{CC}	Supply Current		100	mA
I_{GND}	Ground Current		-100	mA
T_J	Max Junction Temperature		150	°C
T_{STG}	Storage Temperature Range		−65 to 150	°C
ESD	HBM(JESD22-A114)		±4000	V
	CDM(JESD22-C101)		±1500	V

Stresses exceeding those listed in this table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note1:The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Thermal Characteristics

Symbol	Package	Ratings	Value	Unit
$R_{\theta JA}$	SC70-6	Thermal Characteristics, Thermal Resistance, Junction-to-Air	TBD	°C/W
	SOT23-6		TBD	
	DFN6(1.50×1.00)		TBD	
	DFN6(1.00×1.00)		TBD	
P_D @25°C	SC70-6	Power Dissipation in Still Air at 25°C	TBD	mW
	SOT23-6		TBD	
	DFN6(1.50×1.00)		TBD	
	DFN6(1.00×1.00)		TBD	

Recommended Operating Conditions

Symbol	Parameters	Min	Max	Unit
V_{CC}	Supply Voltage Range	1.65	5.5	V
V_I	Input Voltage	0	5.5	V
V_O	Output Voltage	0	V_{CC}	V
T_A	Ambient Temperature	-40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied.

Electrical Characteristics

Static Characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameters	Conditions	V_{CC}(V)	-40°C≤T_A≤85°C			-40°C≤T_A≤125°C		Unit
				Min	Typ(2)	Max	Min	Max	
V_{OL}	LOW-level Output Voltage	V_I = V_{T+} or V_{T-}							
		I_O = 100μA	1.65V to 5.5V			0.1		0.1	V
		I_O = 4mA	1.65V			0.45		0.7	V
		I_O = 8mA	2.3V			0.3		0.45	V
		I_O = 12mA	2.7V			0.4		0.6	V
		I_O = 24mA	3.0V			0.55		0.8	V
		I_O = 32mA	4.5V			0.55		0.8	V
V_{OH}	HIGH-level Output Voltage	V_I = V_{T+} or V_{T-}							
		I_O = -100μA	1.65V to 5.5V	V_{CC} - 0.1			V_{CC} - 0.1		V
		I_O = -4mA	1.65V	1.2			0.95		V
		I_O = -8mA	2.3V	1.9			1.7		V
		I_O = -12mA	2.7V	2.2			1.9		V
		I_O = -24mA	3.0V	2.3			2.0		V
		I_O = -32mA	4.5V	3.8			3.4		V
I_I	Input Leakage Current	V_I = 5.5V or GND	0V to 5.5V		±0.1	±1		±1	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O =5.5V	0V		±0.1	±2		±2	μA
I_{CC}	Supply Current	V_I=5.5V or GND; I_O = 0A	1.65V to 5.5V		0.1	4		4	μA
ΔI_{CC}	Additional Supply Current	V_I=V_{CC} - 0.6V; I_O = 0A	2.3V to 5.5V		5	500		500	μA
C_I	Input Capacitance	Input Capacitance			2.5				pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Note2: Typical values are measured at maximum V_{CC} and T_A = 25 °C.

Electrical Characteristics(Continued)

Dynamic Characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig 10.

Symbol	Parameters	Conditions	V_{CC}(V)	-40°C≤T_A≤85°C			-40°C≤T_A≤125°C		Unit
				Min	Typ(2)	Max	Min	Max	
T_{PD}	Propagation Delay	A, B, C to Y; See Fig.10(3)	tPHL						
			1.65 V to 1.95V	2.0	10.0	15.0	2.0	18	ns
			2.3V to 2.7V	1.5	7.0	11.0	1.5	14.0	ns
			2.7V	1.5	6.7	10.5	1.5	13.0	ns
			3.0V to 3.6V	1.5	7.0	10.0	1.5	12.0	ns
			4.5V to 5.5V	1.5	5.5	9.5	1.5	11.0	ns
			tPLH						
			1.65 V to 1.95V	4.0	20.0	29.0	4.0	32.0	ns
			2.3V to 2.7V	3.0	17.6	25.0	3.0	28.0	ns
			2.7V	3.0	19.2	24.0	3.0	27.0	ns
			3.0V to 3.6V	3.0	15.5	23.0	3.0	26.0	ns
			4.5V to 5.5V	3.0	13.5	21.0	3.0	24.0	ns
C_{PD}	Power Dissipation Capacitance	V_I=GND to V_{CC}(4)	3.3V		22				pF

Note3: T_{pd} is the same as T_{PLH} and T_{PHL}.

Note4: C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

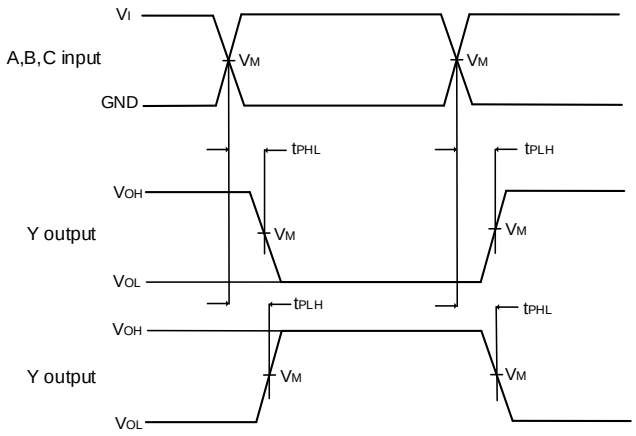
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

Test Circuit



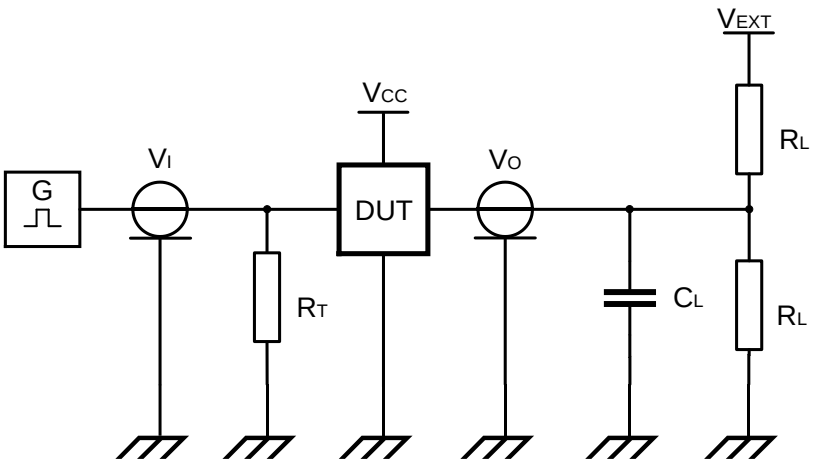
Measurement points are given in Table 1.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig.10 Input A, B and C to output Y propagation delay times

Table 1.Measurement Points

Supply Voltage	Input		Output
V_{CC}	V_M	V_I	V_M
1.65 V to 1.95 V	0.5 × V_{CC}	V_{CC}	0.5 × V_{CC}
2.3 V to 2.7 V	0.5 × V_{CC}	V_{CC}	0.5 × V_{CC}
2.7 V	1.5 V	2.7 V	1.5 V
3.0 V to 3.6 V	1.5 V	2.7 V	1.5 V
4.5 V to 5.5 V	0.5 × V_{CC}	V_{CC}	0.5 × V_{CC}



Measurement points are given in Table 2.

Definitions test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_O of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

Fig.11 Test circuit for measuring switching times

Table 2.Test Data

Supply Voltage	**Input**		**Load**		**V_{EXT}**
V_{CC}	**V_I**	**$t_r = t_f$**	**C_L**	**R_L**	**t_{PLH} , t_{PHL}**
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 kΩ	open
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open

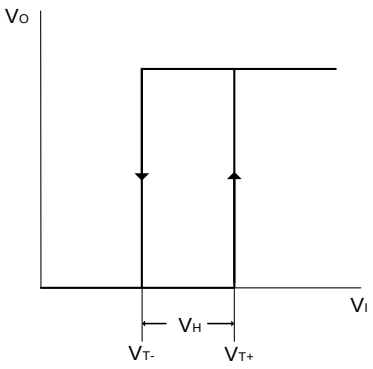
Electrical Characteristics

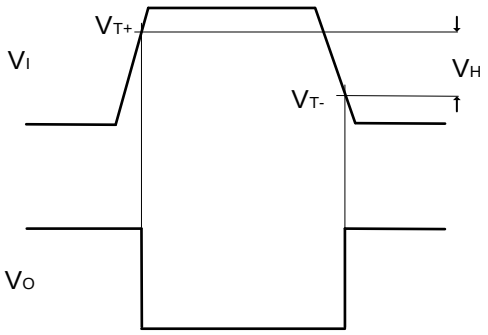
Transfer Characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

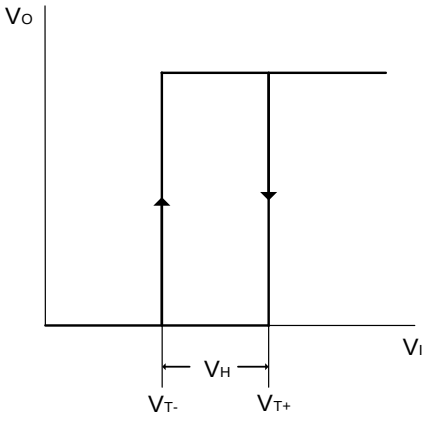
Symbol	Parameters	Conditions	-40°C≤T_A≤85°C			-40°C≤T_A≤125°C		Unit
			Min	Typ(2)	Max	Min	Max	
V_{T+}	Positive-going Threshold Voltage	See Fig. 12, Fig. 13, Fig. 14 and Fig. 15						
		V_{CC} = 1.8V	0.95	1.20	1.45	0.90	1.40	V
		V_{CC} = 2.3V	1.25	1.50	1.75	1.15	1.70	V
		V_{CC} = 3.0V	1.60	1.90	2.15	1.50	2.10	V
		V_{CC} = 4.5V	2.45	2.70	2.95	2.40	2.90	V
		V_{CC} = 5.5V	2.85	3.10	3.35	2.80	3.30	V
V_{T-}	Negative-going Threshold Voltage	See Fig. 12, Fig. 13, Fig. 14 and Fig. 15						
		V_{CC} = 1.8V	0.40	0.60	0.80	0.40	0.83	V
		V_{CC} = 2.3V	0.58	0.77	1.00	0.58	1.03	V
		V_{CC} = 3.0V	0.80	1.04	1.30	0.80	1.33	V
		V_{CC} = 4.5V	1.21	1.55	1.90	1.21	1.93	V
		V_{CC} = 5.5V	1.50	1.92	2.34	1.50	2.36	V
V_H	Hysteresis Voltage	(V_{T+} - V_{T-}) See Fig. 12, Fig. 13, Fig. 14 and Fig. 15						
		V_{CC} = 1.8V	0.40	0.60	0.95	0.33	0.95	V
		V_{CC} = 2.3V	0.50	0.73	0.97	0.43	0.97	V
		V_{CC} = 3.0V	0.60	0.82	1.05	0.54	1.05	V
		V_{CC} = 4.5V	0.70	1.05	1.30	0.64	1.30	V
		V_{CC} = 5.5V	0.75	1.20	1.55	0.69	1.55	V

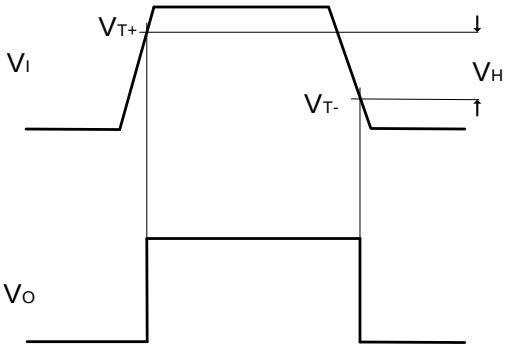
Wave-forms Transfer Characteristics





V_{T+} and V_{T-} limits are at 70 % and 20 %





V_{T+} and V_{T-} limits are at 70 % and 20 %

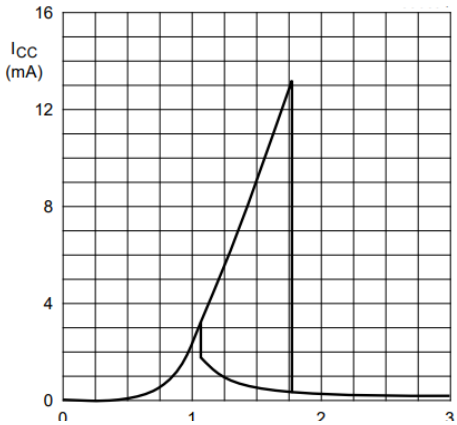


Fig 16. Typical SN74LVC1G57 transfer characteristic; V_{CC} = 3.0 V

Application Circuits

This application shows the SN74LVC1G57 configured as an OR gate with an inverted input. This particular configuration is helpful for dual sensor or switch applications where one of the inputs is normally closed or a logic high 1. Normally this application would require two external gates, but because the SN74LVC1G57 can be configured to meet this function the application can be implemented with a single chip solution.

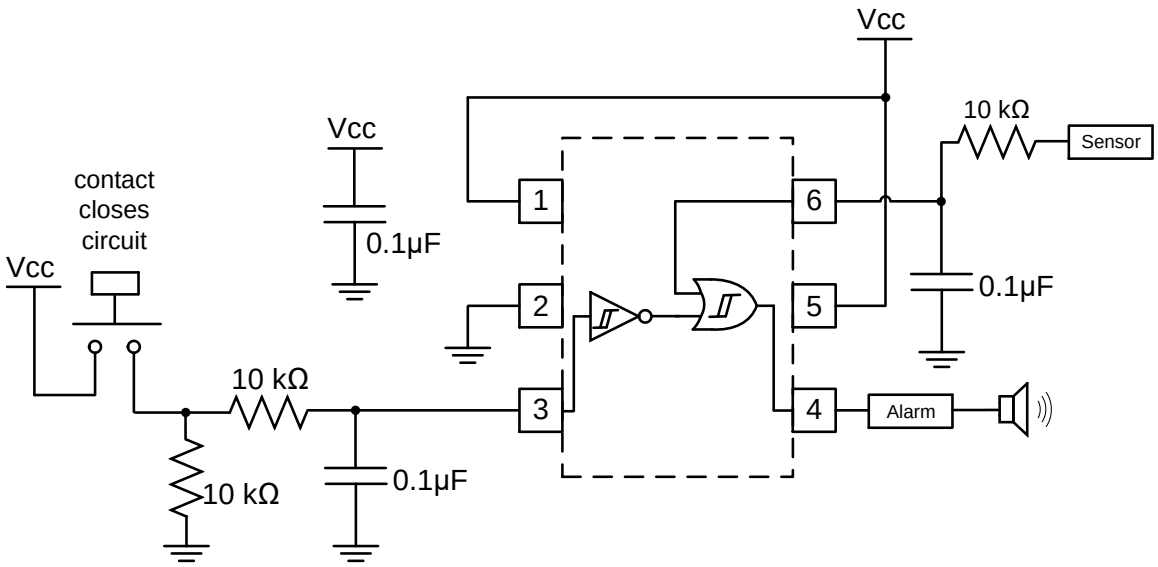
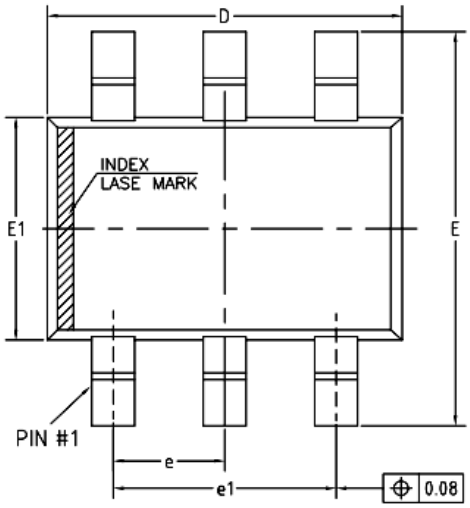


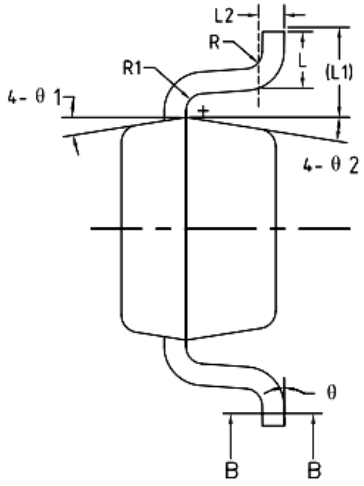
Fig 19. Dual-Sensor Alarm Trigger [5]

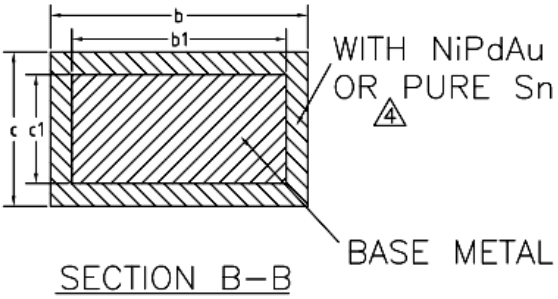
Note5: This application circuit is for reference only.

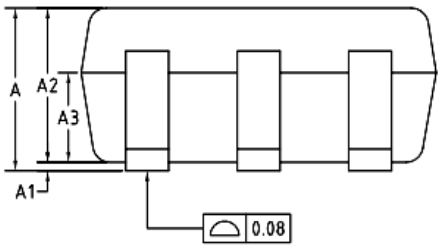
Package Dimension

SC70-6





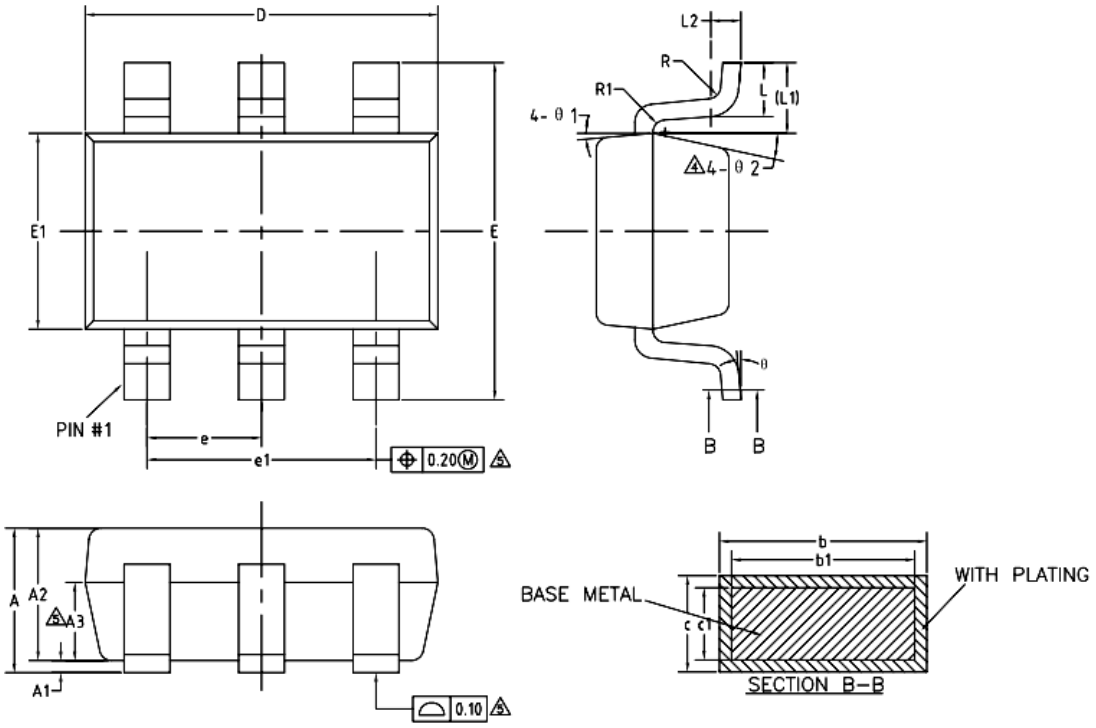




COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL		MIN	NOM	MAX
A		0.85	–	1.05
A1		0	–	0.10
A2		0.80	0.90	1.00
A3		0.47	0.52	0.57
b	NiPdAu	0.22	–	0.29
	PURE Sn	0.23	–	0.33
b1		0.22	0.25	0.28
c	NiPdAu	0.115	–	0.15
	PURE Sn	0.12	–	0.18
c1		0.115	0.13	0.14
D		2.02	2.07	2.12
E		2.20	2.30	2.40
E1		1.25	1.30	1.35
e		0.60	0.65	0.70
e1		1.20	1.30	1.40
L		0.28	0.33	0.38
L1		0.50REF		
L2		0.15BSC		
R		0.10	–	–
R1		0.10	–	0.25
θ		0°	–	8°
θ 1		6°	9°	12°
θ 2		6°	9°	12°

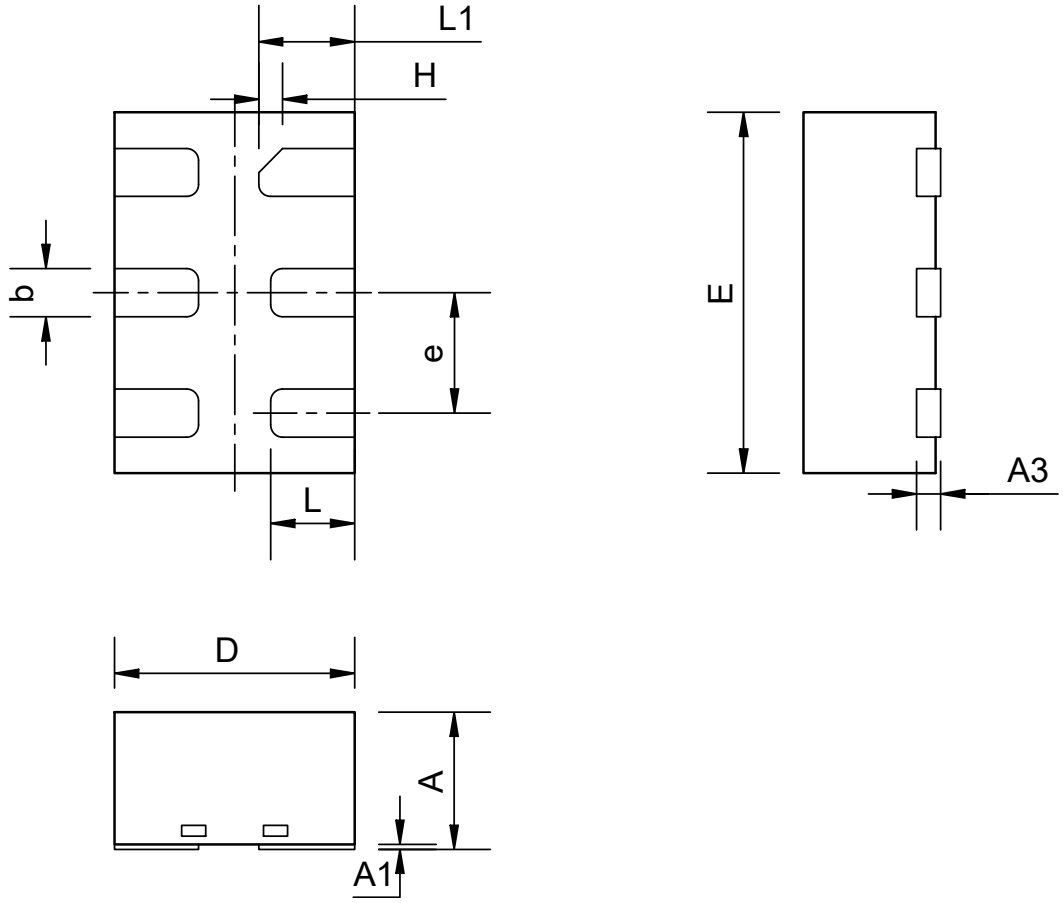
SOT23-6



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

	SYMBOL	MIN	NOM	MAX
	A	–	–	1.25
	A1	0	–	0.15
	A2	1.00	1.10	1.20
	A3	0.60	0.65	0.70
	b	0.36	–	0.50
	b1	0.36	0.38	0.45
	c	0.14	–	0.20
	c1	0.14	0.15	0.16
	D	2.826	2.926	3.026
	E	2.60	2.80	3.00
	E1	1.526	1.626	1.726
4	e	0.90	0.95	1.00
4	e1	1.80	1.90	2.00
	L	0.35	0.45	0.60
	L1	0.59REF		
	L2	0.25BSC		
5	R	0.10	–	–
5	R1	0.10	–	0.20
	θ	0°	–	8°
	θ1	3°	5°	7°
4	θ2	6°	–	14°

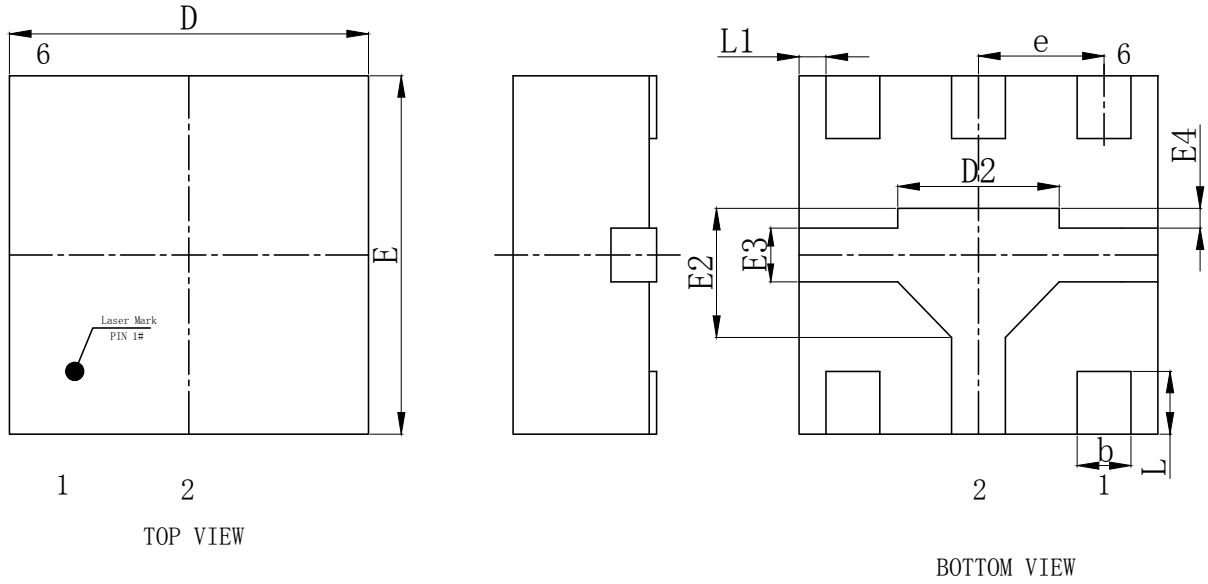
DFN6(1.0×1.5)

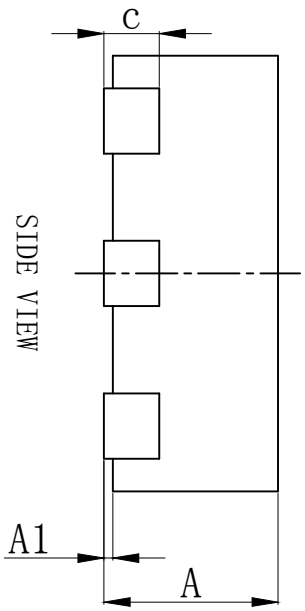


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.50	--	0.60
A1	0	0.02	0.05
A3		0.10REF	
b	0.15	0.20	0.25
D	0.90	1.00	1.10
E	1.40	1.50	1.60
e	0.40	0.50	0.60
H		0.10REF	
L	0.30	0.35	0.40
L1	0.35	0.40	0.45

DFN6(1.0×1.0)





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0. 36	-	0. 40
A1	0. 00	0.02	0. 05
b	0. 10	0. 15	0. 20
c	0. 127REF		
D	0. 95	1. 00	1. 05
D2	0. 40	0. 45	0. 50
e	0. 35BSC		
E	0. 95	1. 00	1. 05
E2	0. 31	0. 36	0. 41
E3	0. 10	0. 15	0. 20
E4	0. 005	0. 055	0. 105
L	0. 125	0.175	0. 225
L1	0.075REF		

Ordering information

Order code	Package	Baseqty	Deliverymode	Marking code
UMW SN74LVC1G57DBVR	SOT23-6	3000	Tape and reel	CA7RU
UMW SN74LVC1G57DCKR	SC70-6	3000	Tape and reel	CLRU
UMW SN74LVC1G57DRYR	DFN6(1*1.5)	5000	Tape and reel	CL U
UMW SN74LVC1G57DSFR	DFN6(1*1)	5000	Tape and reel	CL U