

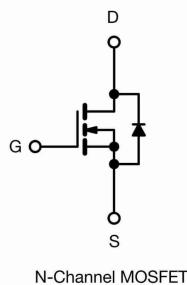
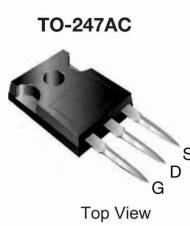
FCHD190N65S3R0-F155-VB Datasheet

650V Single-N SJ_Multi-EPI TO247 MOSFET

PRODUCT SUMMARY		
V_{DS} (V) at T_J max.	650	
$R_{DS(on)}$ (Ω) at 25 °C	$V_{GS} = 10$ V	0.19
Q_g max. (nC)		106
Q_{gs} (nC)		14
Q_{gd} (nC)		33
Configuration	Single	

FEATURES

- Reduced t_{rr} , Q_{rr} , and I_{RRM}
- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low input capacitance (C_{iss})
- Low switching losses due to reduced Q_{rr}
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)



APPLICATIONS

- Telecommunications
 - Server and telecom power supplies
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Consumer and computing
 - ATX power supplies
- Industrial
 - Welding
 - Battery chargers
- Renewable energy
 - Solar (PV inverters)
- Switch mode power supplies (SMPS)

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	650	V
Gate-Source Voltage		V_{GS}	± 30	
Continuous Drain Current ($T_J = 150$ °C)	V_{GS} at 10 V	I_D	20	A
			13	
Pulsed Drain Current ^a		I_{DM}	53	
Linear Derating Factor			1.7	W/°C
Single Pulse Avalanche Energy ^b		E_{AS}	367	mJ
Maximum Power Dissipation		P_D	208	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +150	°C
Drain-Source Voltage Slope	$T_J = 125$ °C	dV/dt	37	V/ns
Reverse Diode dV/dt ^d			31	
Soldering Recommendations (Peak Temperature) ^c	for 10 s		300	°C

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature.

b. $V_{DD} = 50$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω, $I_{AS} = 5.1$ A.

c. 1.6 mm from case.

d. $I_{SD} \leq I_D$, $dI/dt = 100$ A/μs, starting $T_J = 25$ °C.

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	$^{\circ}\text{C}/\text{W}$
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.5	

 SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$		650	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, $I_D = 1 \text{ mA}$		-	0.67	-	$\text{V}/^{\circ}\text{C}$
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$		2	-	4	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA
		$V_{GS} = \pm 30 \text{ V}$		-	-	± 1	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 520 \text{ V}$, $V_{GS} = 0 \text{ V}$		-	-	1	μA
		$V_{DS} = 520 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 125 \text{ }^{\circ}\text{C}$		-	-	500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$	$I_D = 11 \text{ A}$	-	0.19	-	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 30 \text{ V}$, $I_D = 11 \text{ A}$		-	7.0	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0 \text{ V}$, $V_{DS} = 100 \text{ V}$, $f = 1 \text{ MHz}$		-	2322	-	pF
Output Capacitance	C_{oss}			-	105	-	
Reverse Transfer Capacitance	C_{rss}			-	4	-	
Effective Output Capacitance, Energy Related ^a	$C_{o(er)}$			-	84	-	
Effective Output Capacitance, Time Related ^b	$C_{o(tr)}$			-	293	-	
Total Gate Charge	Q_g	$V_{GS} = 10 \text{ V}$	$I_D = 11 \text{ A}$, $V_{DS} = 520 \text{ V}$	-	71	106	nC
Gate-Source Charge	Q_{gs}			-	14	-	
Gate-Drain Charge	Q_{gd}			-	33	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 520 \text{ V}$, $I_D = 11 \text{ A}$, $V_{GS} = 10 \text{ V}$, $R_g = 9.1 \Omega$		-	22	44	ns
Rise Time	t_r		-	34	68		
Turn-Off Delay Time	$t_{d(off)}$		-	68	102		
Fall Time	t_f		-	42	84		
Gate Input Resistance	R_g	$f = 1 \text{ MHz}$, open drain		-	0.78	-	Ω
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	21	A
Pulsed Diode Forward Current	I_{SM}			-	-	53	
Diode Forward Voltage	V_{SD}	$T_J = 25 \text{ }^{\circ}\text{C}$, $I_S = 11 \text{ A}$, $V_{GS} = 0 \text{ V}$		-	0.9	1.2	V
Reverse Recovery Time	t_{rr}		-	160	-	ns	
Reverse Recovery Charge	Q_{rr}		-	1.2	-	μC	
Reverse Recovery Current	I_{RRM}		-	14	-	A	

Notes

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .
 b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .

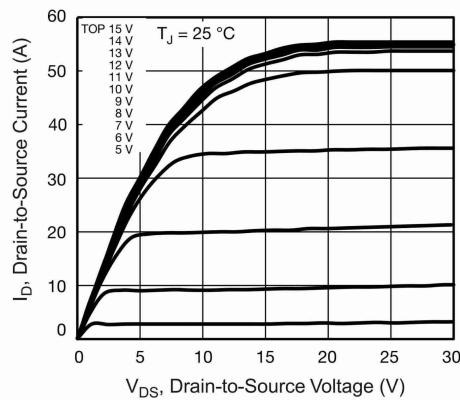
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


Fig. 1 - Typical Output Characteristics

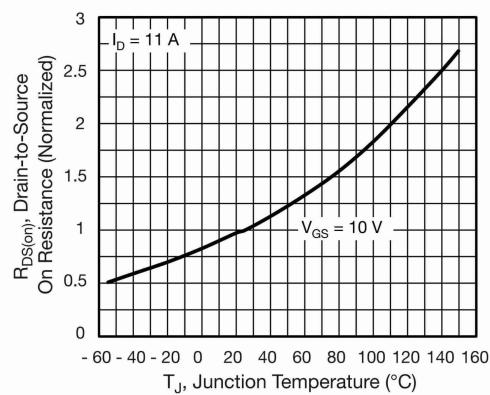


Fig. 4 - Normalized On-Resistance vs. Temperature

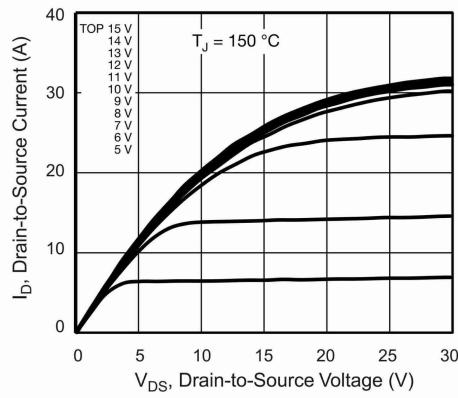


Fig. 2 - Typical Output Characteristics

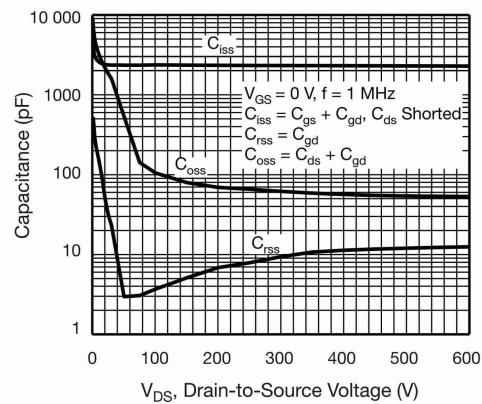


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

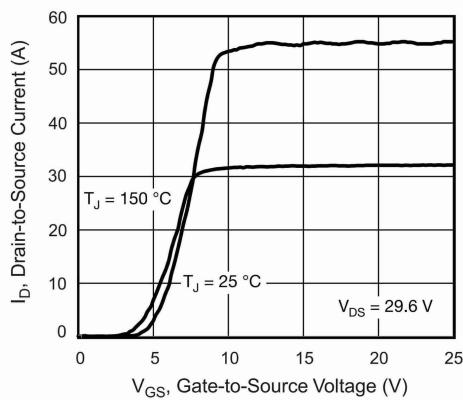
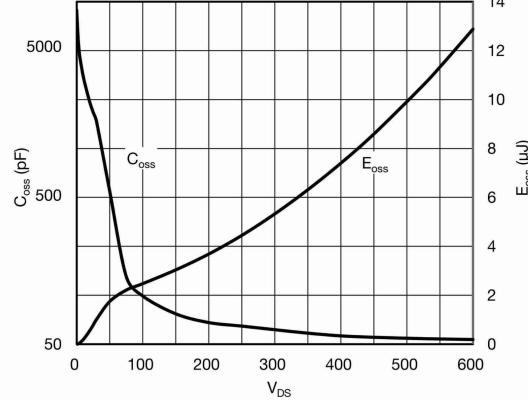


Fig. 3 - Typical Transfer Characteristics

Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}

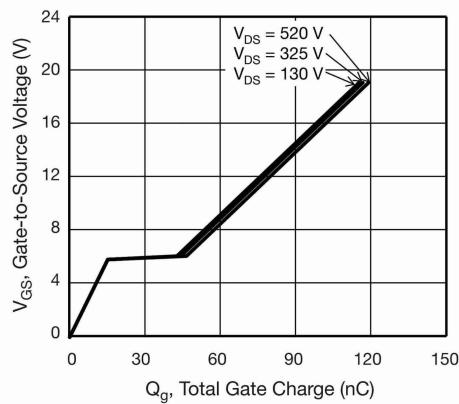


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

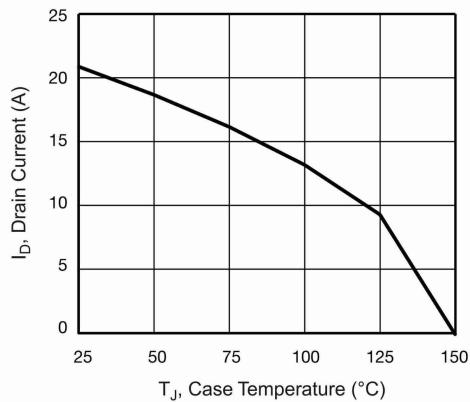


Fig. 10 - Maximum Drain Current vs. Case Temperature

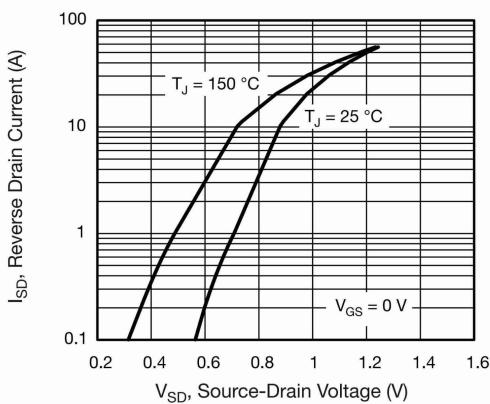


Fig. 8 - Typical Source-Drain Diode Forward Voltage

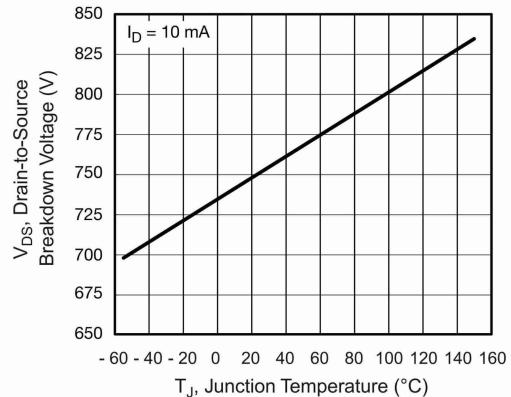


Fig. 11 - Temperature vs. Drain-to-Source Voltage

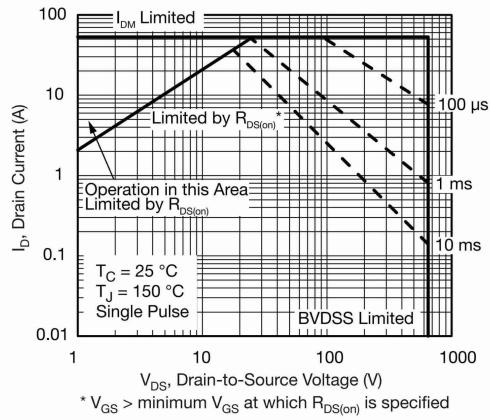


Fig. 9 - Maximum Safe Operating Area

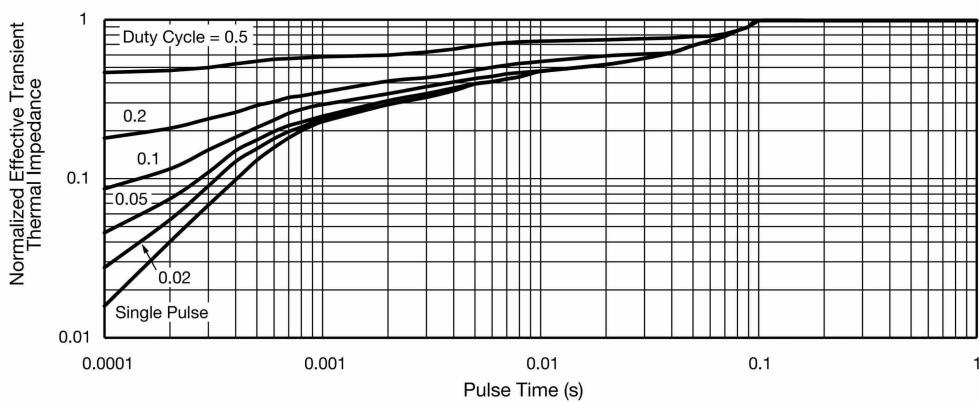


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

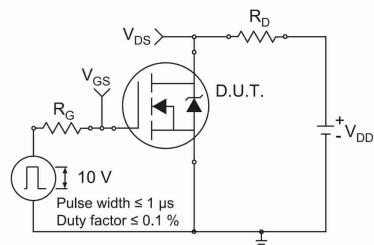


Fig. 13 - Switching Time Test Circuit

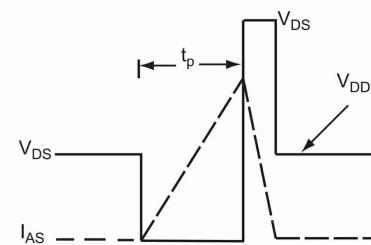


Fig. 16 - Unclamped Inductive Waveforms

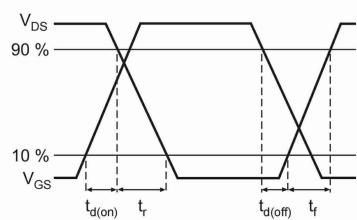


Fig. 14 - Switching Time Waveforms

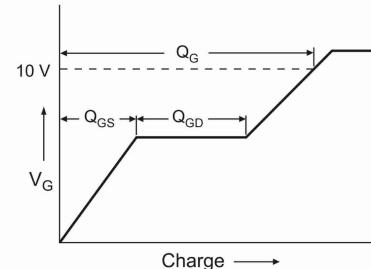


Fig. 17 - Basic Gate Charge Waveform

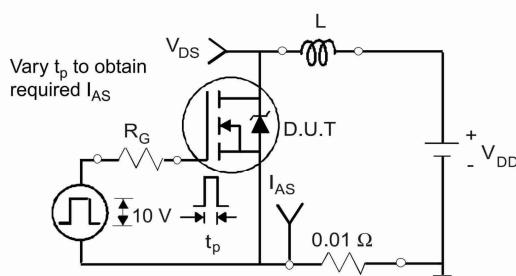


Fig. 15 - Unclamped Inductive Test Circuit

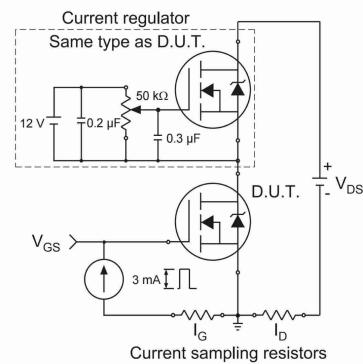
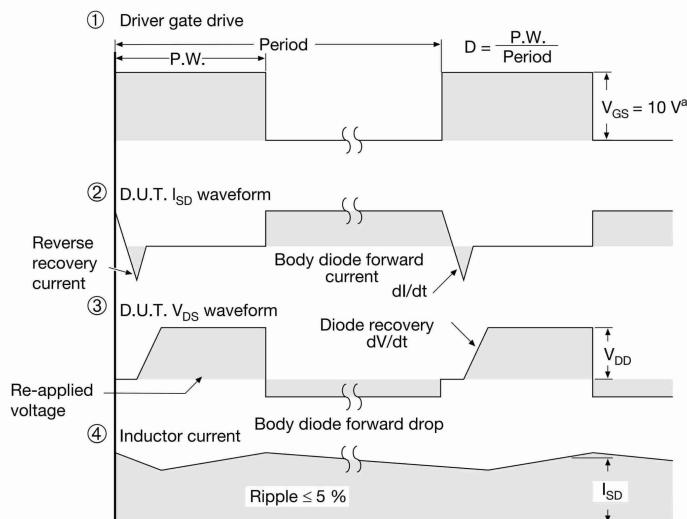
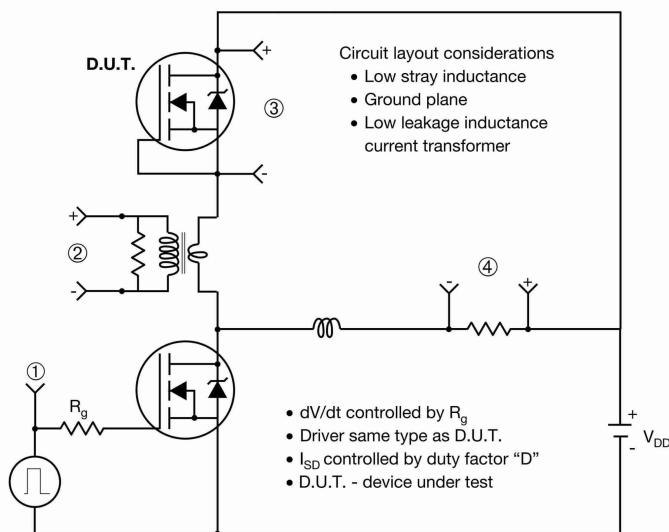


Fig. 18 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

Fig. 19 - For N-Channel

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