Mediatek MT7531 Datasheet

Version: 2.2
Release date: 2020-12-11

Overview

Applications:
- Standalone Switch
- Switch in Wired router
- Switch in Access pointer

MT7531 is a highly integrated wired Ethernet switch with high performance and non-blocking forwarding. It includes a 7-port Gigabit Ethernet MAC and a 5-port Gigabit Ethernet PHY for home entertainment, home automation and so on. It also integrated 2-port high speed SGMII interface for 2.5Gbps backbone or the external 2.5Gbps PHY.

MT7531 enables an advanced power-saving feature to meet the market requirement. It complies with IEEE803.3az for Energy Efficient Ethernet and cable-length/link-down power saving mode. MT7531 is also designed for cost-sensitive applications in retail and Telecom market. MediaTek's industry-leading techniques provide customers with the most cost-competitive and lowest power consumption Ethernet product in the industry.

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With the advanced technology and abundant features, MT7531 is well positioned to be the core of next-generation router, and home gateway systems.

Key Features

- 5-port 10/100/1000Mbps UTP + 7-port MAC
  - 2-port SGMII@2.5Gbps (7531AE)
  - 1-port SGMII@2.5Gbps + 1-port MII/RGMII (7531BE)
- 5-port 10/100/1000Mbps UTP + 5-port MAC (7531DE)
- Accessible MAC/IGMP address table
  - 2048 entries learned in 4-way hash
  - Extra 64 entries for collision pool
  - Shared with IGMP table
- Full 4K VLAN entries and double VLAN tag recognition
- Support 2 LED pins on per UTP port
- Support one Interrupt pin to MCU
- External 32K-bytes EEPROM space for configuration
- Green Ethernet
  - Link-down power saving
  - IEEE 802.3az Energy Efficient Ethernet
- Supports 25MHz clock source
  - 25MHz DIP XTAL
- Package
  - 128-pin LQFP 14mm x 14mm

Document Revision History

Revision	Date	Description
Preliminary	2019-02-12	Initial Draft
1.0	2019-05-31	Formal release
1.1	2019-06-14	Update 4.1 dimension
1.2	2019-07-01	1. Update 2.3 Pin Sharing 2. Add note on PFC
1.3	2020-01-08	1. Update 2.4 Strapping options 2. Remove one clock source
2.0	2020-04-29	1. Recommend 4.7k ohm pull resistance value 2. Pin#60 AVDD33_MISC changed to N.C. 3. Add WOL, PFC support and MDIO timing diagram
2.1	2020-10-06	Title change
2.2	2020-12-10	Add DC electrical characteristics

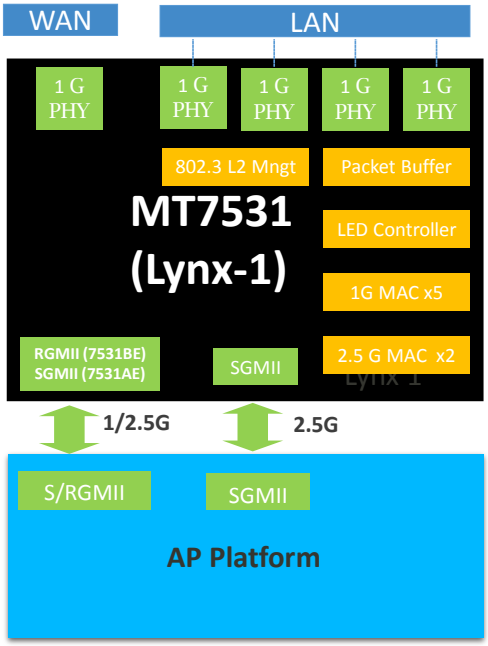
Function Block Diagram

MT7531 Release 1Gbps between LAN and WLAN

- 5-port 10/100/1000Mbps MDI transceivers
- 1-port SGMII MAC(P6), and 1-port RGMII/SGMII MAC(P5)
- Supports 2.5Gbps SGMII+ mode

- 802.1x,
- 802.3i, 3u, 3z, 3ab
- 256 sets of ACL rules
- Compliant with IEEE 802.3 Auto-Negotiation
- Integrated switch regulator for single 3.3V external power source
- 2 pins LED per port

- 128-pin, LQFP, 14mm x 14mm



- 2K MAC address table programmable aging
- Up to 15K Jumbo frame length
- 25MHz clock source

- RSTP and MSTP
- Supports 4K VLAN entries
- 8 priority queues per port

- 256 sets of ACL rules
- IGMPv1/v2/v3 and MLDv1/v2 snooping
- Supports Loop detection indicator
- Broadcast/Multicast/Unknown frames storm suppression
- Supports link-down power saving

Glossary

Abbreviation	Description
AP	Access Point
ASIC	Application-Specific Integrated Circuit
ASYNC	Asynchronous
BIST	Built-in Self-Test
CLK	Clock
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
EEPROM	Electrically Erasable Programmable Read-Only Memory
EFUSE	Electrical Fuse
FC	Flow Control
FIFO	First In First Out
FSM	Finite State Machine
GND	Ground
GPIO	General Purpose Input/output
GPO	General Purpose Output
I^2C	Inter-Integrated Circuit
I/O	Input/output
JEDEC	Joint Electron Devices Engineering Council
IEEE	Institute of Electrical and Electronics Engineers
Kbps	Kilo (10^3) bits per second
KB	Kilo (10^3) Bytes
Mbps	Mega (10^6) bits per second
MB	Mega (10^6) Bytes
MII	Media Independent Interface
LDO	Low-Dropout Regulator
LED	Light-Emitting Diode
LSB	Least Significant Bit
MAC	Medium Access Controller
MCU	Microcontroller Unit
MDC	Management Data Clock
MDIO	Management Data Input/output

Abbreviation	Description
MEM	Memory
MSB	Most Significant Bit
MSTP	Multiple Spanning Tree Protocol
OSC	Open Source Control
PFC	Priority Flow Control
PLL	Phase Lock Loop
PMU	Power Management Unit
PPP	Point-to-point Protocol
PPPoE	Point-to-point Protocol over Ethernet
QoS	Quality of Service
RAM	Random Access Memory
RGMII	Reduced Gigabit Media Independent Interface
RevMII	Reverse Media Independent Interface
RoHS	Restriction on Hazardous Substances
ROM	Read-Only Memory
RSTP	Rapid Spanning Tree Protocol
SRAM	Static Random Access Memory
SGMII+	SGMII plus (3.125GHz)
SMI	Serial Management Interface
STP	Spanning Tree Protocol
VoIP	Voice over IP
XTAL	External Crystal Oscillator

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1 General Description

1.1 Introduction

MT7531 is a highly integrated high performance 7-port Gigabit Ethernet switch controller. It integrates 384Kbytes embedded SRAM as the packet memory and supports up to 2K MAC address entries. Equipped with 10Gbps high bandwidth switching fabric, MT7531 provides users a 7-port wire-speed non-blocking switch platform.

MT7531 is targeted at SOHO and Small/Medium sized Business (SMB). To meet the more and more important bandwidth management and multimedia requirements in the markets, MT7531 also supports up to 4K IEEE 802.1Q port-based VLAN and 8 priority queues for advanced network management and QoS solutions. Using the VLAN feature, users can manage broadcasted traffic efficiently. Through the priority queue mechanisms, MT7531 switches the different kinds of traffics (e.g., normal data, expedited data, voice and video) according to the traffic characteristics and user's requirements, and then provides end users a multimedia environment. In all ports, the flow control functions are implemented to prevent the switch from congestion or overflow. Avoiding the broadcast storm from the abnormal network events, per port can be programmed a specific bandwidth threshold to suppress the exceeding packets. The dump switch can be configured just through EEPROM with simple control parameter.

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The MT7531 is fabricated with 28nm Low Power CMOS technology, where the inputs are 3.3V tolerant and the outputs are capable of directly interfacing to Low-Voltage TTL levels. The chip is packaged in a 128-pin LQFP.

1.2 Features

- Supports 25Mhz XTAL DIP external clock source
- 10Base-T, 10Base-Te, 100Base-TX, and 1000Base-T compliant Transceivers
- Compliant with IEEE 802.3 Auto-Negotiation
- Supports 2 LEDs per GEPHY port
- Integrated MDI resistors
- Supports IEEE 802.3az Energy Efficient Ethernet
- Build-in the best efficient Power Management Unit(PMU) for single power plan
  - 3.3V to 1.15V BUCK converter
  - High efficiency up to 86%
- Embedded 5-port 10/100/1000Mbps MDI transceivers and 2-port SGMII+ Serdes Interface

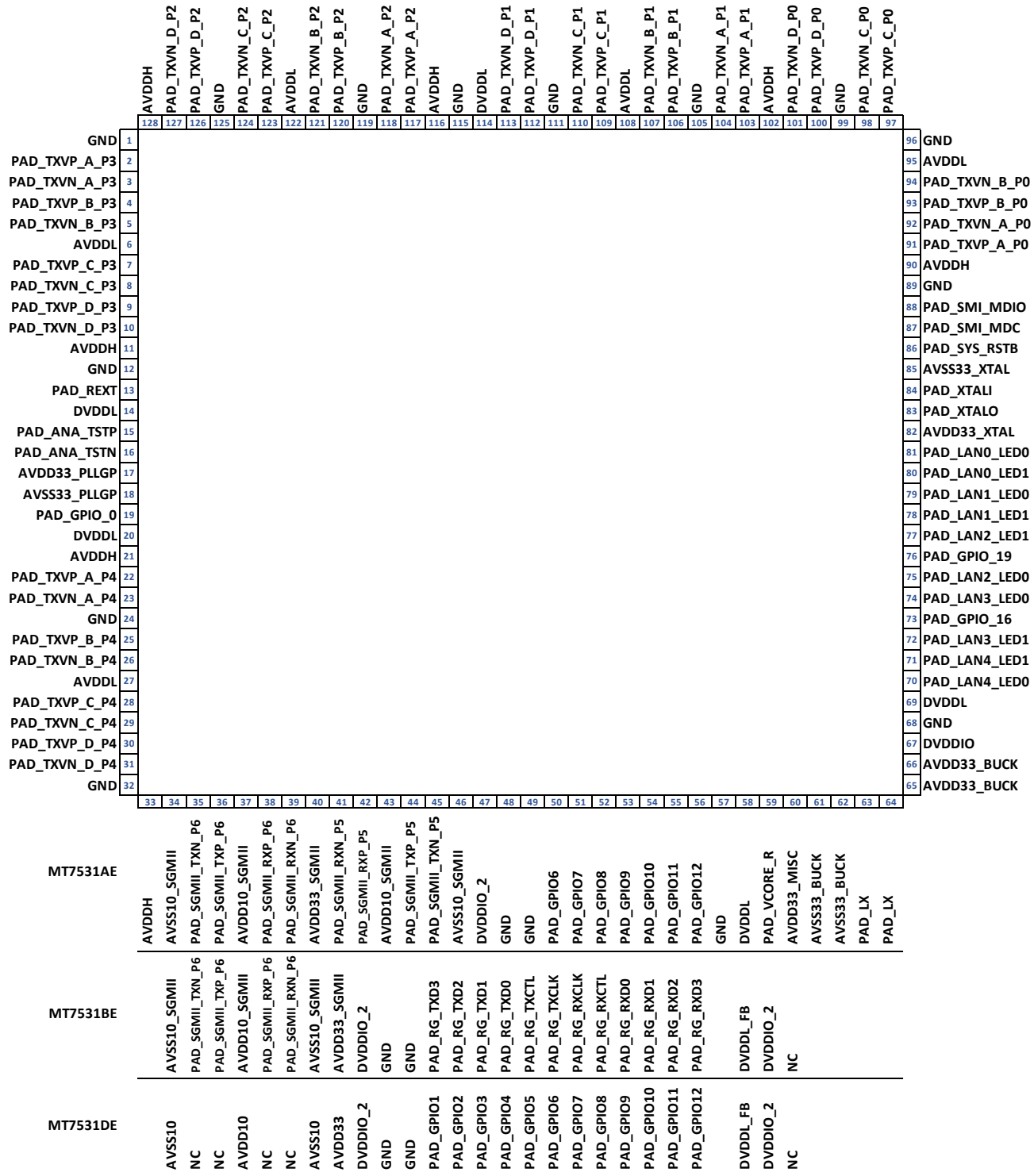
- SGMII for 1.25GHz SerDes interface
- SGMII+ for 3.125GHz SerDes interface

- Supports programmable packet length 1518/1536/1552 or up to 15K Jumbo frame
- Built-in address table with 2K MAC addresses which can support up to 8 filtering databases
  - Accessible by managing interface to keep static addresses
  - Support IVL/SVL based on FID from VLAN table
  - Programmable aging timer: no aging out, 10 ~ 1,000,000 seconds; default is 300 seconds
  - Configurable Address look-up algorithm. Address look-up based on the proprietary hashing algorithm, CRC16 or CRC32.
  - Support Collision Pool with 64 entries
- Per port MAC Address learning control to protect the system from being attacked by hackers
  - Disable learning or aging for Per-port
  - Limit SA Learning number for Per-port
- Support IEEE 802.1x access control protocol and advanced security features
  - Access policy based on Port-based, MAC-based and guest VLAN
  - Access control based on ACL rules
  - Drop unknown Source MAC or Destination MAC address for Per-port
- Support Link Aggregation (Port Trunking)
  - Support maximum 3 aggregation group. Each aggregation group has 2 ports. (P0 P1), (P3 P4), (P5 P6)
  - Configurable port setting for each aggregation group.
  - Configurable distribution scenario. Information used to assign conversations to aggregation ports is configurable. Including Source Port, MAC DA, MAC SA, Source IP Address, Destination IP Address, TCP/UDP Source Port and TCP/UDP Destination Port
- Support Spanning Tree port state HW configuration
  - IEEE 802.1w Rapid Spanning Tree
  - IEEE 802.1s Multiple Spanning Tree with up to 8 Spanning Tree instance
- Up to 4K full VLAN entries with flexible support for IEEE 802.1Q and port-based VLAN
  - Support port-based, Tag-based, and up to 4 port-and-protocol based VLAN
  - Support per-port VLAN tag addition, removal, or leave unchanged
  - Provide special tag for CPU port
  - Support Per Egress port stack VLAN (Q in Q)
  - Support Per Egress port 1:1 and N:1 VLAN Translation
- Leaky VLAN based on port attribute, MAC address and ACL
- Embedded 384K-byte packet buffer
  - Per page is 256-bytes to store the packet data
  - Total 1,536 pages to provide effective flow control mechanism
- Supports 8 priority queues per egress port and the advanced Priority Flow Control (PFC) mechanism

- Per queue MAX-MIN shapers with different schedulers – Strict Priority (SP), Weight Fair Queue (WFQ), Round-Robin (RR) and mixed ones
  - The minimum shapers can use either SP or RR
  - The maximum shapers can use either SP or WRQ
  - Per shaper is enabled/disabled
  - Per shaper threshold setting
  - Per shaper with both the leaky bucket and token bucket algorithms
- Supports ingress and egress rate control
  - Per port egress rate control with both the leaky bucket and token bucket approaches
- ACL Table includes 256 entries rule table and 128 entries rule control table
  - ACL Rule support layer 1 to layer 4. Rules include Port No., DA/SA, Ether Type, VLAN ID, IP Protocol, SIP/DIP, TCP/UDP , SP/DP and user-defined content
  - Actions support mirror, redirect, dropping, priority adjustment, and traffic rate policing
  - Optional per-port Enable/Disable of ACL function
  - Optional setting of per-port action when ACL is mismatched
- IGMP/MLD snooping
  - Support IPv4 IGMP v1/v2/v3 snooping and IPv6 MLD v1/v2 snooping
  - Trap all IGMP and MLD packets to the CPU port. CPU writes the correct multicast entry to the lookup table via management interface
  - Support hardware IGMP(v1/v2) join and fast leave
  - Support partial hardware IGMPv3 and MLDv2 - IS_EX(), TO_EX(), TO_IN(). User-defined SIP Table for IGMPv3/MLDv2, SIP Table hardware auto learning is not supported
- Broadcast/Multicast/Unknown DA storm control/alert depending on the number of the frames received during a period of time to protect the system from being attacked by hackers
- Supports 40 MIB counters per port
- Supports Wake-on-Lan(WOL) indicator and interrupt pin
- Supports Loop detection indicator

2 Pin

2.1 Pin Map



2.2 Pin Descriptions

2.2.1 Package Common Pins

Table 2-1 Common Pin Description

Pin	Name	Reset *1		After Reset *1				Pull *3,4	Voltage (V)	Driving (mA)	Description
		State *2	Pull *3	State *2	Aux *5	Pull *3	Driving				
MISC											
86	PAD_SYS_RSTB	I	PU	I	0	PU	-	PU	3.3	-	System Hardware Reset Pin
GPIO											
19	PAD_GPIO_0	I	PU	I/O	0	-	8	PU/PD	3.3	4/8/12/16	General Purpose IO / Interrupt
73	PAD_GPIO_16	I	PU	I/O	0	-	8	PU/PD	3.3	4/8/12/16	General Purpose IO
76	PAD_GPIO_19	I	PU	I/O	0	-	8	PU/PD	3.3	4/8/12/16	General Purpose IO
LED											
70	PAD_LAN4_LED0	I	PU	O	1	-	8	PU/PD	3.3	4/8/12/16	GSW Port #4 LED #0
71	PAD_LAN4_LED1	I	-	O	1	-	8	PU/PD	3.3	4/8/12/16	GSW Port #4 LED #1
74	PAD_LAN3_LED0	I	PU	O	1	-	8	PU/PD	3.3	4/8/12/16	GSW Port #3 LED #0
72	PAD_LAN3_LED1	I	-	O	1	-	8	PU/PD	3.3	4/8/12/16	GSW Port #3 LED #1
75	PAD_LAN2_LED0	I	PU	O	1	-	8	PU/PD	3.3	4/8/12/16	GSW Port #2 LED #0
77	PAD_LAN2_LED1	I	-	O	1	-	8	PU/PD	3.3	4/8/12/16	GSW Port #2 LED #1
79	PAD_LAN1_LED0	I	PU	O	1	-	8	PU/PD	3.3	4/8/12/16	GSW Port #1 LED #0
78	PAD_LAN1_LED1	I	-	O	1	-	8	PU/PD	3.3	4/8/12/16	GSW Port #1 LED #1
81	PAD_LAN0_LED0	I	PU	O	1	-	8	PU/PD	3.3	4/8/12/16	GSW Port #0 LED #0
80	PAD_LAN0_LED1	I	-	O	1	-	8	PU/PD	3.3	4/8/12/16	GSW Port #0 LED #1
SM											
87	PAD_SMI_MDC	I	PU	O	1	-	8	PU/PD	3.3	4/8/12/16	Serial management clock
88	PAD_SMI_MDIO	I		I/O	1	-	8	PU/PD	3.3	4/8/12/16	Serial management data
XTAL											
83	PAD_XTALO	A	-	A	-	-	-	-	3.3	-	
84	PAD_XTALI	A	-	A	-	-	-	-	3.3	-	
PMU											
63, 64	PAD_LX	A	-	A	-	-	-	-	3.3	-	
MDI											
13	PAD_REXT	A		A					3.3		Band gap resistor which is connected to AVSS33 through a 24kΩ (±1%) resistor

Pin	Name	Reset *1		After Reset *1				Pull *3,4	Voltage (V)	Driving (mA)	Description
		State *2	Pull *3	State *2	Aux *5	Pull *3	Driving				
91	PAD_TXVP_A_P0	A		A					3.3		Port #0 MDI Transceivers
92	PAD_TXVN_A_P0	A		A					3.3		Port #0 MDI Transceivers
93	PAD_TXVP_B_P0	A		A					3.3		Port #0 MDI Transceivers
94	PAD_TXVN_B_P0	A		A					3.3		Port #0 MDI Transceivers
97	PAD_TXVP_C_P0	A		A					3.3		Port #0 MDI Transceivers
98	PAD_TXVN_C_P0	A		A					3.3		Port #0 MDI Transceivers
100	PAD_TXVP_D_P0	A		A					3.3		Port #0 MDI Transceivers
101	PAD_TXVN_D_P0	A		A					3.3		Port #0 MDI Transceivers
103	PAD_TXVP_A_P1	A		A					3.3		Port #1 MDI Transceivers
104	PAD_TXVN_A_P1	A		A					3.3		Port #1 MDI Transceivers
106	PAD_TXVP_B_P1	A		A					3.3		Port #1 MDI Transceivers
107	PAD_TXVN_B_P1	A		A					3.3		Port #1 MDI Transceivers
109	PAD_TXVP_C_P1	A		A					3.3		Port #1 MDI Transceivers
110	PAD_TXVN_C_P1	A		A					3.3		Port #1 MDI Transceivers
112	PAD_TXVP_D_P1	A		A					3.3		Port #1 MDI Transceivers
113	PAD_TXVN_D_P1	A		A					3.3		Port #1 MDI Transceivers
117	PAD_TXVP_A_P2	A		A					3.3		Port #2 MDI Transceivers
118	PAD_TXVN_A_P2	A		A					3.3		Port #2 MDI Transceivers
120	PAD_TXVP_B_P2	A		A					3.3		Port #2 MDI Transceivers
121	PAD_TXVN_B_P2	A		A					3.3		Port #2 MDI Transceivers
123	PAD_TXVP_C_P2	A		A					3.3		Port #2 MDI Transceivers
124	PAD_TXVN_C_P2	A		A					3.3		Port #2 MDI Transceivers
126	PAD_TXVP_D_P2	A		A					3.3		Port #2 MDI Transceivers
127	PAD_TXVN_D_P2	A		A					3.3		Port #2 MDI Transceivers
2	PAD_TXVP_A_P3	A		A					3.3		Port #3 MDI Transceivers
3	PAD_TXVN_A_P3	A		A					3.3		Port #3 MDI Transceivers
4	PAD_TXVP_B_P3	A		A					3.3		Port #3 MDI Transceivers
5	PAD_TXVN_B_P3	A		A					3.3		Port #3 MDI Transceivers
7	PAD_TXVP_C_P3	A		A					3.3		Port #3 MDI Transceivers
8	PAD_TXVN_C_P3	A		A					3.3		Port #3 MDI Transceivers
9	PAD_TXVP_D_P3	A		A					3.3		Port #3 MDI Transceivers
10	PAD_TXVN_D_P3	A		A					3.3		Port #3 MDI Transceivers
22	PAD_TXVP_A_P4	A		A					3.3		Port #4 MDI Transceivers
23	PAD_TXVN_A_P4	A		A					3.3		Port #4 MDI Transceivers
25	PAD_TXVP_B_P4	A		A					3.3		Port #4 MDI Transceivers

Pin	Name	Reset *1		After Reset *1				Pull *3,4	Voltage (V)	Driving (mA)	Description
		State *2	Pull *3	State *2	Aux *5	Pull *3	Driving				
26	PAD_TXVN_B_P4	A		A					3.3		Port #4 MDI Transceivers
28	PAD_TXVP_C_P4	A		A					3.3		Port #4 MDI Transceivers
29	PAD_TXVN_C_P4	A		A					3.3		Port #4 MDI Transceivers
30	PAD_TXVP_D_P4	A		A					3.3		Port #4 MDI Transceivers
31	PAD_TXVN_D_P4	A		A					3.3		Port #4 MDI Transceivers
MISC											
15	PAD_ANA_TSTP	A		A					3.3		Analog Differential Test Pin
16	PAD_ANA_TSTN	A		A					3.3		Analog Differential Test Pin
POWER											
14 20 69 114	DVDDL	P		P					1.15		Digital core power supply
67	DVDDIO	P		P					3.3		Digital IO power supply
6, 27 95 108 122	AVDDL	P		P					1.15		GPHY analog power supply
11, 21 33, 90 102 116 128	AVDDH	P		P					3.3		GPHY analog power supply
65, 66	AVDD33_BUCK	P		P					3.3		BUCK analog power supply
17	AVDD33_PLLGP	P		P					3.3		PLLGP analog power supply
82	AVDD33_XTAL	P		P					3.3		XTAL analog power supply
60	AVDD33_MISC	P		P					3.3		POR, ELDO analog power supply
GROUND											
61, 62	AVSS33_BUCK	G		G							Ground for BUCK
18	AVSS33_PLLGP	G		G							Ground for PLL
K16	AVSS33_XTAL	G		G							Ground for XTAL

Pin	Name	Reset *1		After Reset *1				Pull *3,4	Voltage (V)	Driving (mA)	Description
		State *2	Pull *3	State *2	Aux *5	Pull *3	Driving				
1, 12 24, 32 57, 68 89, 96 99 105 111 115 119 125	GND	G		G							Ground

NOTE:

1. Section 3.9 for reset and after reset period definition.
2. I: Input
   OH: Output high
   OL: Output low
   A: Analog
   P: Power
   G: Ground
   NC: No connection
3. The internal pull resistance value is 75 kΩ.
4. PD: Internal pull-down
   PU: Internal pull-up
   NP: No pull-down/up
5. Section 2.3.1 for pin share scheme detail.

2.2.2 MT7531AE

Table 2-2 MT7531AE Exclusive Pin Description

Pin	Name	Reset *1		After Reset *1				Pull *3,4	Voltage (V)	Driving (mA)	Description
		State *2	Pull *3	State *2	Aux *5	Pull *3	Driving				
GPIO											
50	PAD_GPIO_6	I/O		I/O	1	-	8	PU/PD	3.3	4/8/12/16	General Purpose IO
51	PAD_GPIO_7	I/O		I/O	1	-	8	PU/PD	3.3	4/8/12/16	General Purpose IO
52	PAD_GPIO_8	I/O		I/O	1	-	8	PU/PD	3.3	4/8/12/16	General Purpose IO
53	PAD_GPIO_9	I/O		I/O	1	-	8	PU/PD	3.3	4/8/12/16	General Purpose IO
54	PAD_GPIO_10	I/O		I/O	1	-	8	PU/PD	3.3	4/8/12/16	General Purpose IO
55	PAD_GPIO_11	I/O		I/O	1	-	8	PU/PD	3.3	4/8/12/16	General Purpose IO
56	PAD_GPIO_12	I/O		I/O	1	-	8	PU/PD	3.3	4/8/12/16	General Purpose IO
SGMII											
35	PAD_SGMII_TXN_P6	A		A					3.3		P6 SGMII differential transmit TX -
36	PAD_SGMII_TXP_P6	A		A					3.3		P6 SGMII differential transmit TX+
38	PAD_SGMII_RXP_P6	A		A					3.3		P6 SGMII differential receive RX +
39	PAD_SGMII_RXN_P6	A		A					3.3		P6 SGMII differential receive RX -
41	PAD_SGMII_RXN_P5	A		A					3.3		P5 SGMII differential receive RX -
42	PAD_SGMII_RXP_P5	A		A					3.3		P5 SGMII differential receive RX+
44	PAD_SGMII_TXP_P5	A		A					3.3		P5 SGMII differential transmit TX +
45	PAD_SGMII_TXN_P5	A		A					3.3		P5 SGMII differential transmit TX -
POWER											
47	DVDDIO_2	P		P					3.3		Digital IO power supply
37, 43	AVDD10_SGMII	P		P					1.15		SGMII analog power supply
40	AVDD33_SGMII	P		P					3.3		SGMII analog power supply
58	DVDDL	P		P					1.15		Digital core power supply
59	PAD_VCORE_R	P		P					1.15		BUCK FB analog power supply
60	AVDD33_MISC	P		P					3.3		POR, ELDO analog power supply
GROUND											
34, 46	AVSS10_SGMII	G		G							Ground for SGMII
48, 49	GND	G		G							Ground

2.2.3 MT7531BE

Table 2-3 MT7531BE Exclusive Pin Description

Pin	Name	Reset *1		After Reset *1				Pull *3,4	Voltage (V)	Driving (mA)	Description
		State *2	Pull *3	State *2	Aux *5	Pull *3	Driving				
GPIO											
51	PAD_RG_RXCLK	I/O		I/O	1	-	8	PU/PD	2.5/3.3	4/8/12/16	P5 RGMII RX clock
52	PAD_RG_RXCTL	I/O		I/O	1	-	8	PU/PD	2.5/3.3	4/8/12/16	P5 RGMII RX data valid
53	PAD_RG_RXD0	I/O		I/O	1	-	8	PU/PD	2.5/3.3	4/8/12/16	P5 RGMII RX data bit #0
54	PAD_RG_RXD1	I/O		I/O	1	-	8	PU/PD	2.5/3.3	4/8/12/16	P5 RGMII RX data bit #1
55	PAD_RG_RXD2	I/O		I/O	1	-	8	PU/PD	2.5/3.3	4/8/12/16	P5 RGMII RX data bit #2
56	PAD_RG_RXD3	I/O		I/O	1	-	8	PU/PD	2.5/3.3	4/8/12/16	P5 RGMII RX data bit #3
50	PAD_RG_TXCLK	I/O		I/O	1	-	8	PU/PD	2.5/3.3	4/8/12/16	P5 RGMII TX clock
49	PAD_RG_TXCTL	I/O		I/O	1	-	8	PU/PD	2.5/3.3	4/8/12/16	P5 RGMII TX data valid
48	PAD_RG_TXD0	I/O		I/O	1	-	8	PU/PD	2.5/3.3	4/8/12/16	P5 RGMII TX data bit #0
47	PAD_RG_TXD1	I/O		I/O	1	-	8	PU/PD	2.5/3.3	4/8/12/16	P5 RGMII TX data bit #1
46	PAD_RG_TXD2	I/O		I/O	1	-	8	PU/PD	2.5/3.3	4/8/12/16	P5 RGMII TX data bit #2
45	PAD_RG_TXD3	I/O		I/O	1	-	8	PU/PD	2.5/3.3	4/8/12/16	P5 RGMII TX data bit #3
MISC											
60	NC								3.3		No connection
SGMII											
35	PAD_SGMII_TXN_P6	A		A					3.3		P6 SGMII differential transmit TX -
36	PAD_SGMII_TXP_P6	A		A					3.3		P6 SGMII differential transmit TX+
38	PAD_SGMII_RXP_P6	A		A					3.3		P6 SGMII differential receive RX +
39	PAD_SGMII_RXN_P6	A		A					3.3		P6 SGMII differential receive RX -
POWER											
42, 59	DVDDIO_2	P		P					2.5/3.3		RGMII IO power supply
37	AVDD10_SGMII	P		P					1.15		SGMII analog power supply
41	AVDD33_SGMII	P		P					3.3		SGMII analog power supply
58	DVDDL_FB	P		P					1.15		Digital core power supply BUCK FB analog power supply
GROUND											
34, 40	AVSS10_SGMII	G		G							Ground for SGMII
43, 44	GND	G		G							Ground

2.2.4 MT7531DE

Table 2-4 MT7531DE Exclusive Pin Description

Pin	Name	Reset *1		After Reset *1				Pull *3,4	Voltage (V)	Driving (mA)	Description
		State *2	Pull *3	State *2	Aux *5	Pull *3	Driving				
GPIO											
45	PAD_GPIO_1	I/O		I/O	1	-	8	PU/PD	3.3	4/8/12/16	General Purpose IO
46	PAD_GPIO_2	I/O		I/O	1	-	8	PU/PD	3.3	4/8/12/16	General Purpose IO
47	PAD_GPIO_3	I/O		I/O	1	-	8	PU/PD	3.3	4/8/12/16	General Purpose IO
48	PAD_GPIO_4	I/O		I/O	1	-	8	PU/PD	3.3	4/8/12/16	General Purpose IO
49	PAD_GPIO_5	I/O		I/O	1	-	8	PU/PD	3.3	4/8/12/16	General Purpose IO
50	PAD_GPIO_6	I/O		I/O	1	-	8	PU/PD	3.3	4/8/12/16	General Purpose IO
51	PAD_GPIO_7	I/O		I/O	1	-	8	PU/PD	3.3	4/8/12/16	General Purpose IO
52	PAD_GPIO_8	I/O		I/O	1	-	8	PU/PD	3.3	4/8/12/16	General Purpose IO
53	PAD_GPIO_9	I/O		I/O	1	-	8	PU/PD	3.3	4/8/12/16	General Purpose IO
54	PAD_GPIO_10	I/O		I/O	1	-	8	PU/PD	3.3	4/8/12/16	General Purpose IO
55	PAD_GPIO_11	I/O		I/O	1	-	8	PU/PD	3.3	4/8/12/16	General Purpose IO
56	PAD_GPIO_12	I/O		I/O	1	-	8	PU/PD	3.3	4/8/12/16	General Purpose IO
MISC											
35, 36 38, 39 60	NC								3.3		No connection
POWER											
42, 59	DVDDIO_2	P		P					3.3		Digital IO power supply
37	AVDD10	P		P					1.15		SGMII analog power supply
41	AVDD33	P		P					3.3		SGMII analog power supply
58	DVDDL_FB	P		P					1.15		Digital core power supply BUCK FB analog power supply
GROUND											
34, 40	AVSS10	G		G							Ground for analog
43, 44	GND	G		G							Ground

2.3 Pin Sharing Schemes

Some pins are shared with GPIO to provide maximum flexibility for system designers. The MT7531 provides up to 15 GPIO pins. Users can configure registers specify the pin function. For more information, see the Programmer's Guide. The pin's default function mode is configured on Func.0.

2.3.1 Pin share scheme

Table 2-5 Pin Share

Pins			Func. 0	Func. 1 (default pin func.)	Func. 2
MT7531AE	**MT7531BE**	**MT7531DE**			
PAD_GPIO_0	PAD_GPIO_0	PAD_GPIO_0	GPIO0 **(O)**	INTERRUPT (O)	-
-	PAD_RG_TXD3	PAD_GPIO1	GPIO1 (IO)	PAD_RG_TXD3 (IO)	-
-	PAD_RG_TXD2	PAD_GPIO2	GPIO2 (IO)	PAD_RG_TXD2 (IO)	-
-	PAD_RG_TXD1	PAD_GPIO3	GPIO3 (IO)	PAD_RG_TXD1 (IO)	-
-	PAD_RG_TXD0	PAD_GPIO4	GPIO4 (IO)	PAD_RG_TXD0 (IO)	
-	PAD_RG_TXCTL	PAD_GPIO5	GPIO4 (IO)	PAD_RG_TXCTL (IO)	
PAD_GPIO6	PAD_RG_TXCLK	PAD_GPIO6	GPIO6 (IO)	PAD_RG_TXCLK (IO)	
PAD_GPIO7	PAD_RG_RXCLK	PAD_GPIO7	GPIO7 (IO)	PAD_RG_RXCLK (IO)	
PAD_GPIO8	PAD_RG_RXCTL	PAD_GPIO8	GPIO8 (IO)	PAD_RG_RXCTL (IO)	
PAD_GPIO9	PAD_RG_RXD0	PAD_GPIO9	GPIO9 (IO)	PAD_RG_RXD0 (IO)	
PAD_GPIO10	PAD_RG_RXD1	PAD_GPIO10	GPIO10 (IO)	PAD_RG_RXD1 (IO)	
PAD_GPIO11	PAD_RG_RXD2	PAD_GPIO11	GPIO11 (IO)	PAD_RG_RXD2 (IO)	EXT_P_MDC (O)
PAD_GPIO12	PAD_RG_RXD3	PAD_GPIO12	GPIO12 (IO)	PAD_RG_RXD3 (IO)	EXT_P_MDIO (IO)
PAD_LAN4_LED0	PAD_LAN4_LED0	PAD_LAN4_LED0	GPIO13 **(O)**	PAD_LAN4_LED0 (O)	
PAD_LAN4_LED1	PAD_LAN4_LED1	PAD_LAN4_LED1	GPIO14 (IO)	PAD_LAN4_LED1 (O)	
PAD_LAN3_LED1	PAD_LAN3_LED1	PAD_LAN3_LED1	GPIO15 (IO)	PAD_LAN3_LED1 (O)	
PAD_GPIO_16	PAD_GPIO_16	PAD_GPIO_16	GPIO16 **(O)**	-	
PAD_LAN3_LED0	PAD_LAN3_LED0	PAD_LAN3_LED0	GPIO17 **(O)**	PAD_LAN3_LED0 (O)	
PAD_LAN2_LED0	PAD_LAN2_LED0	PAD_LAN2_LED0	GPIO18 **(O)**	PAD_LAN2_LED0 (O)	
PAD_GPIO_19	PAD_GPIO_19	PAD_GPIO_19	GPIO19 **(O)**	-	
PAD_LAN2_LED1	PAD_LAN2_LED1	PAD_LAN2_LED1	GPIO20 (IO)	PAD_LAN2_LED1 (O)	EXT_P_MDC (O)
PAD_LAN1_LED1	PAD_LAN1_LED1	PAD_LAN1_LED1	GPIO21 (IO)	PAD_LAN1_LED1 (O)	EXT_P_MDIO (IO)
PAD_LAN1_LED0	PAD_LAN1_LED0	PAD_LAN1_LED0	GPIO22 **(O)**	PAD_LAN1_LED0 (O)	

PAD_LAN0_LED1	PAD_LAN0_LED1	PAD_LAN0_LED1	GPIO23 (IO)	PAD_LAN0_LED1 (O)	
PAD_LAN0_LED0	PAD_LAN0_LED0	PAD_LAN0_LED0	GPIO24 **(O)**	PAD_LAN0_LED0 (O)	

Note:

"O" = output function

"I" = input function

"IO" = bi-direction function, high active

2.3.2 xMII PHY/MAC Pin Mapping

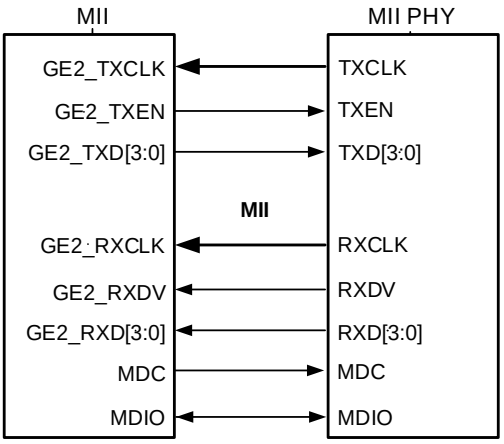


Figure 2-1 MII → MII PHY

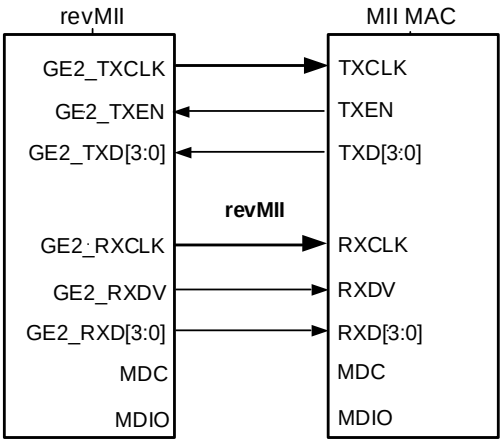


Figure 2-2 revMII → MII MAC

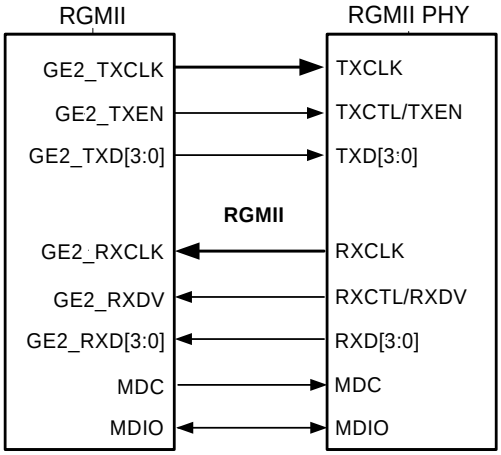


Figure 2-3 RGMII → RGMII PHY

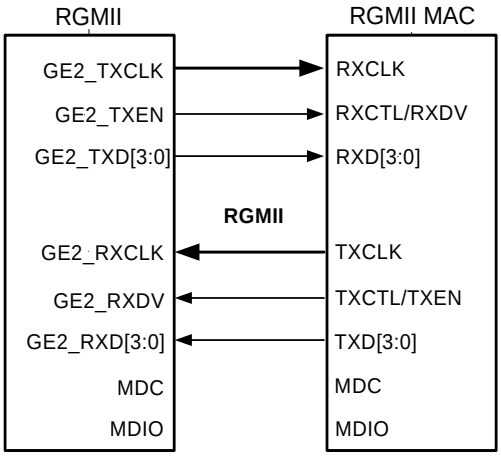


Figure 2-4 RGMII → RGMII MAC

2.4 Strapping Options

Table 2-6 Strapping

Pin Name	Strapping Name	Description
PAD_GPIO_0	TM_DIS	TM_DIS - Test Mode Strap Pull Up : Disable (default) Pull Down: Enable Test Mode
PAD_LAN4_LED0	EEP_MODE	EEP_MODE - EEPROM mode selection Pull up: EEPROM size greater than 16Kbits (24C32 ~ 24C256) (default) Pull down: EEPROM size less than or equal 16Kbits (24C02 ~ 24C16)
PAD_GPIO_16	PON_LT	PON_LT - Enable Power on Light Pull Up: Enable (default) Pull Down: Disable
PAD_GPIO_19	EEP_DIS	EEP_DIS - Disable EEPROM/Flash Autoload. Pull Up : Disable (default) Pull Down: Enable
PAD_LAN1LED0	PHY_EN	PHY_EN - Enable Embedded PHY Pull Up : Enable (default) Pull Down: Disable

NOTE:

1. These strap pins have the internal 75 kΩ pull-high resistor as the default value when the pins are kept floating.
2. Recommended that the strap pins are pulled high or low through the external 4.7 kΩ resistor.

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

Symbol or Pin name	Description	Min.	Max.	Unit
AVDDH	3.3V supply voltage	-0.3	3.63	V
AVDDD33_PLLGP	3.3V supply voltage	-0.3	3.63	V
AVDD33_XTAL	3.3V supply voltage	-0.3	3.63	V
AVDD33_SGMII	3.3V supply voltage	-0.3	3.63	V
AVDDL	1.15V supply voltage	-0.3	1.26	V
DVDDIO DVDDIO_2	3.3V supply voltage	-0.3	3.63	V
DVDDL	1.15V supply voltage	-0.3	1.26	V
AVDD33_MISC	3.3V supply voltage	-0.3	3.63	V
AVDD33_BUCK	1.15V supply voltage	-0.3	3.63	V
PAD_LX	1.15V supply voltage	-0.3	1.26	V
AVDD10_SGMII	1.15V supply voltage	-0.3	1.26	V

3.2 Recommended Operating Range

Table 3-2 Recommended Operating Range

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
AVDDH	3.3V supply voltage	3.135	3.30	3.63	V
AVDDD33_PLLGP	3.3V supply voltage	3.135	3.30	3.63	V
AVDD33_XTAL	3.3V supply voltage	3.135	3.30	3.63	V
AVDD33_SGMII	3.3V supply voltage	3.135	3.30	3.63	V
AVDD33_MISC	3.3V supply voltage	3.135	3.30	3.63	V
AVDD33_BUCK	3.3V supply voltage	3.135	3.30	3.63	V
DVDDIO	3.3V supply voltage	2.97	3.30	3.63	V
DVDDIO_2	3.3V supply voltage	2.97	3.30	3.63	V
	2.5V supply voltage (*1)	2.25	2.50	2.75	V
DVDDL	1.15V supply voltage	1.093	1.15	1.26	V
AVDDL	1.15V supply voltage	1.093	1.15	1.26	V
AVDD10_SGMII	1.15V supply voltage	1.093	1.15	1.26	V

NOTE:

1. Supported on MT7531BE model

3.3 Thermal Characteristics

Thermal characteristics when stationary without an external heat sink in an air-conditioned environment.

Table 3-3 Thermal Characteristics

Symbol	Description	Performance	
		Typ	Unit
T_J	Maximum Junction Temperature (Plastic Package)	125	°C
θ_{JA}	Thermal resistance for JEDEC 2L system PCB	58.2	°C/W
θ_{JA}	Thermal resistance for JEDEC 4L system PCB	54.5	°C/W
θ_{JC}	Thermal resistance for JEDEC 4L system PCB	17.2	°C/W
θ_{JB}	Thermal resistance for JEDEC 4L system PCB	45.41	°C/W
ψ_{Jt}	Thermal characterization parameter for JEDEC 2L system PCB	0.9	°C/W
ψ_{Jt}	Thermal characterization parameter for JEDEC 4L system PCB	0.84	°C/W

Note: JEDEC 51-7 system FR4 PCB size: 76.2x114.3mm (3”x4.5”)

3.4 Operating Conditions

Table 3-4 Operating Conditions

I/O supply voltage	3.3 V +/- 10%
Core supply voltage	1.15 V -5% to +10%
Ambient Temperature Range	-20 to 55 °C
Core supply voltage	1.15 V -5% to +10%

3.5 Storage Conditions

The calculated shelf life in a sealed bag is 12 months if stored between 5 °C and 40 °C at less than 90% relative humidity (RH). After the bag is opened, devices that are subjected to solder reflow or other high temperature processes must be handled in the following manner:

- Mounted within 168 hours of factory conditions, i.e. < 30 °C at 60% RH.
- Storage humidity needs to be maintained at < 10% RH.
- Baking is necessary if the customer has opened the bag without the solder reflow for over 168 hours,
  - Exposed to air <= 72hrs, baking conditions: 125 °C for 17 hrs.
  - Exposed to air > 72hrs, baking conditions: 125 °C for 27 hrs.

3.6 External XTAL Specification

Table 3-5 External XTAL Specifications

Parameter	Min	Typ	Max	Unit
Frequency		25		MHz
Drive Level		210		uW
Frequency Tolerance	-50		+50	ppm
Equivalent Series Resistance			100	Ω
Load Capacitance		16		pF
Series resistor connected between XTALO and crystal		150		Ω

3.7 DC Electrical Characteristics

3.7.1 GPIO pins

Table 3-6 GPIO Electrical Characteristics

3.3V GPIO					
Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input low voltage	-0.3	-	0.8	V
V_{IH}	Input high voltage	2.0	-	3.9	V
V_{OL}	Output low voltage	-0.3	-	0.4	V
V_{OH}	Output high voltage	2.6	-	3.9	V
R_{PU}	Input pull-up resistance	40	75	190	KΩ
R_{PD}	Input pull-down resistance	40	75	190	KΩ

3.7.1 RGMII pins

Table 3-7 RGMII Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R_{PU}	Input pull-up resistance	40	75	190	KΩ
R_{PD}	Input pull-down resistance	40	75	190	KΩ
3.3V RGMII					
V_{IL}	Input low voltage	-0.3	-	0.8	V
V_{IH}	Input high voltage	2.0	-	3.9	V
V_{OL}	Output low voltage	-0.3	-	0.4	V
V_{OH}	Output high voltage	2.6	-	3.9	V

2.5V RGMII					
V_{IL}	Input low voltage	-0.3	-	0.7	V
V_{IH}	Input high voltage	1.6	-	3.0	V
V_{OL}	Output low voltage	-0.3	-	0.4	V
V_{OH}	Output high voltage	1.9	-	3.0	V

3.8 AC Electrical Characteristics

3.8.1 RGMII Interface

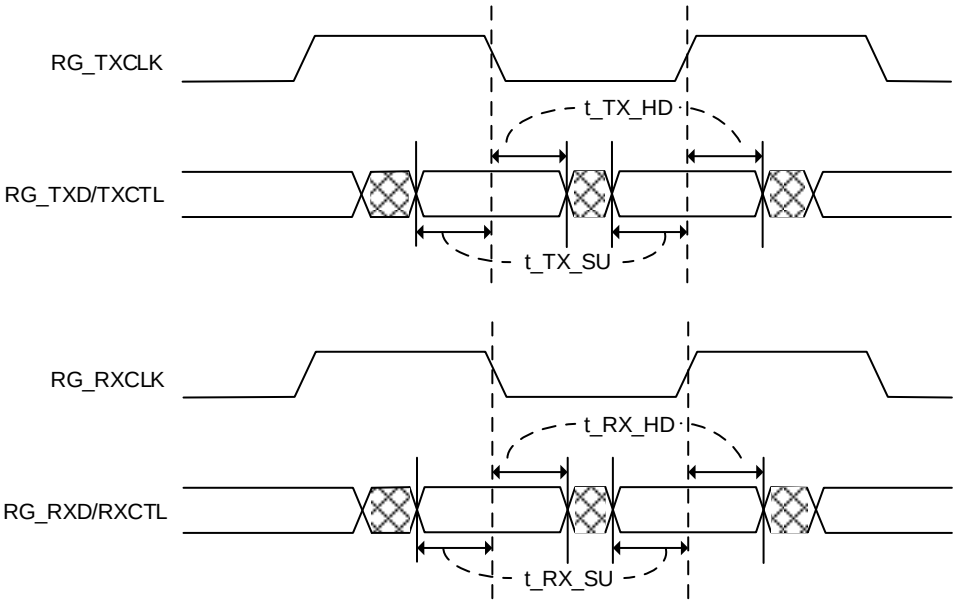


Figure 3-1 RGMII Timing

Table 3-8 RGMII Interface Diagram Key

Symbol	Description	Min	Max	Unit	Remark
t_TX_SU	Setup time for output signals (e.g. RG_TXD*, RG_TXCTL)	1.2	-	ns	output load: 5 pF
t_TX_HD	Hold time for output signals	1.2	-	ns	output load: 5 pF
t_RX_SU	Setup time for input signals (e.g. RG_RXD*, RG_RXCTL)	1.0	-	ns	
t_RX_HD	Hold time for input signals	1.0	-	ns	

3.8.2 MII Interface

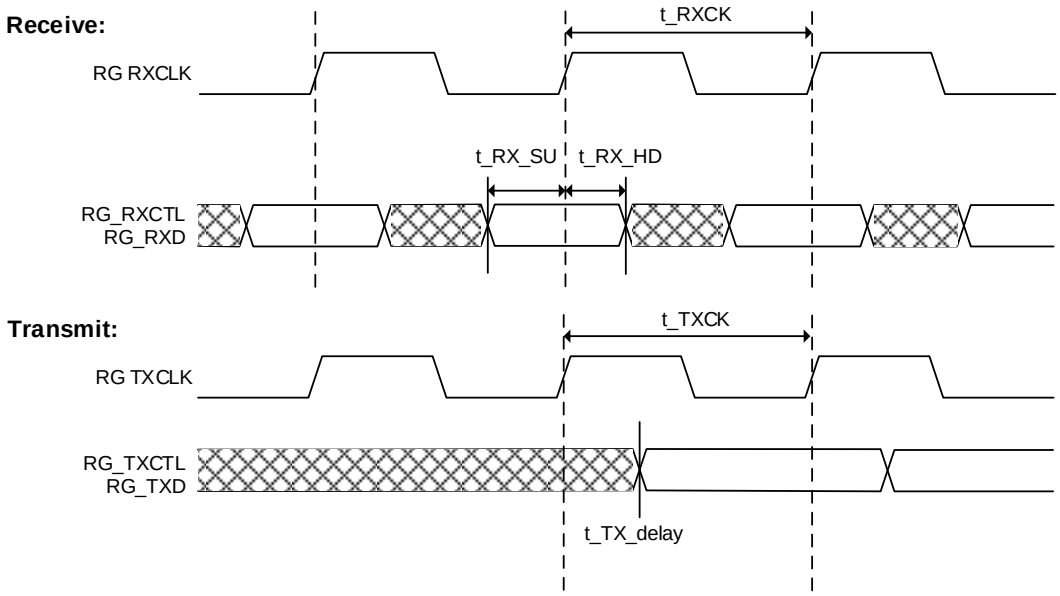


Figure 3-2 MII Timing

Table 3-9 MII Interface Diagram Key

Symbol	Description	Min	Max	Unit	Remark
t_TX_delay	Delay to output signals (e.g. RG_TXD*, RG_TXCTL)	-	25	ns	output load: 10 pF
t_RX_SU	Setup time for input signals (e.g. RG_RXD*, RG_RXCTL)	10	-	ns	
t_RX_HD	Hold time for input signals	10	-	ns	

Note: For 25 MHz TXCLK & RXCLK

3.8.3 SMI Interface

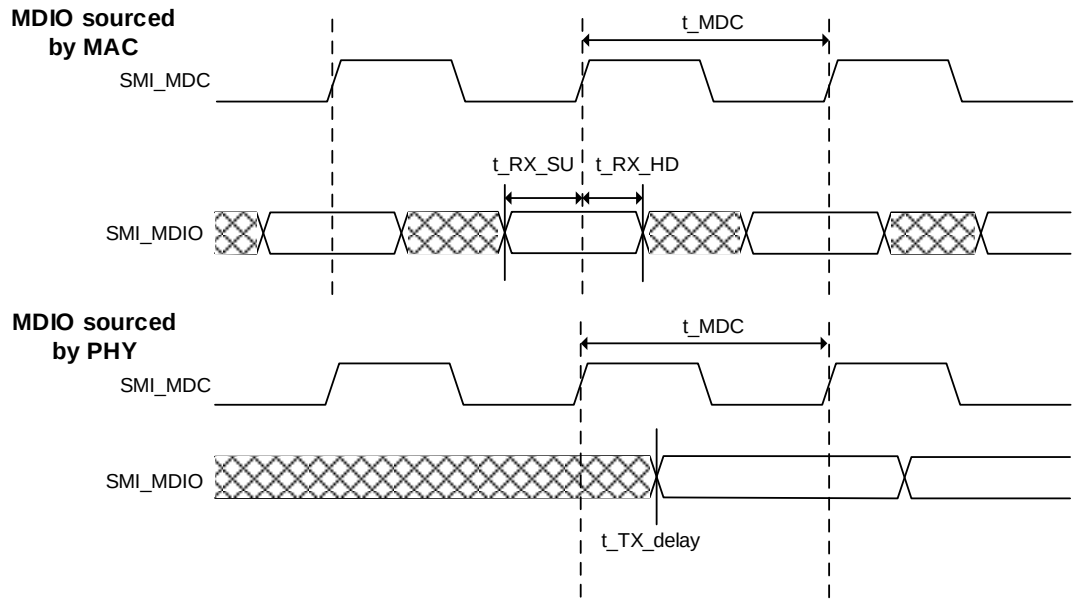


Figure 3-3 SMI MDIO Timing

Table 3-10 SMI Interface Diagram Key

Symbol	Description	Min	Max	Unit	Remark
t_TX_delay	Clock to output delay from the PHY	0	300	ns	
t_RX_SU	Setup time referenced to the rising edge of SMI_MDC	10	-	ns	
t_RX_HD	Hold time referenced to the rising edge of SMI_MDC	10	-	ns	

Note: For 2.5 MHz SMI_MDC

3.9 Power-on Sequence

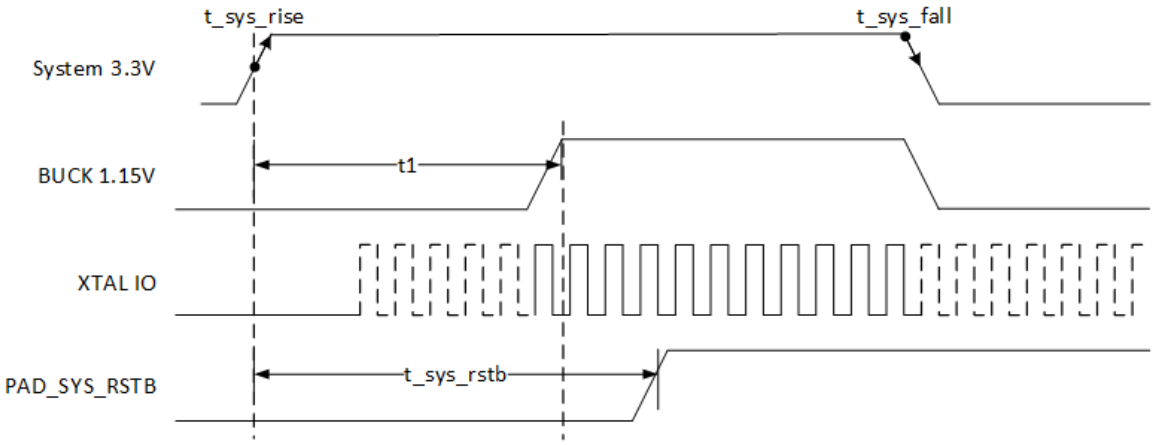


Figure 3-4 Power ON Sequence

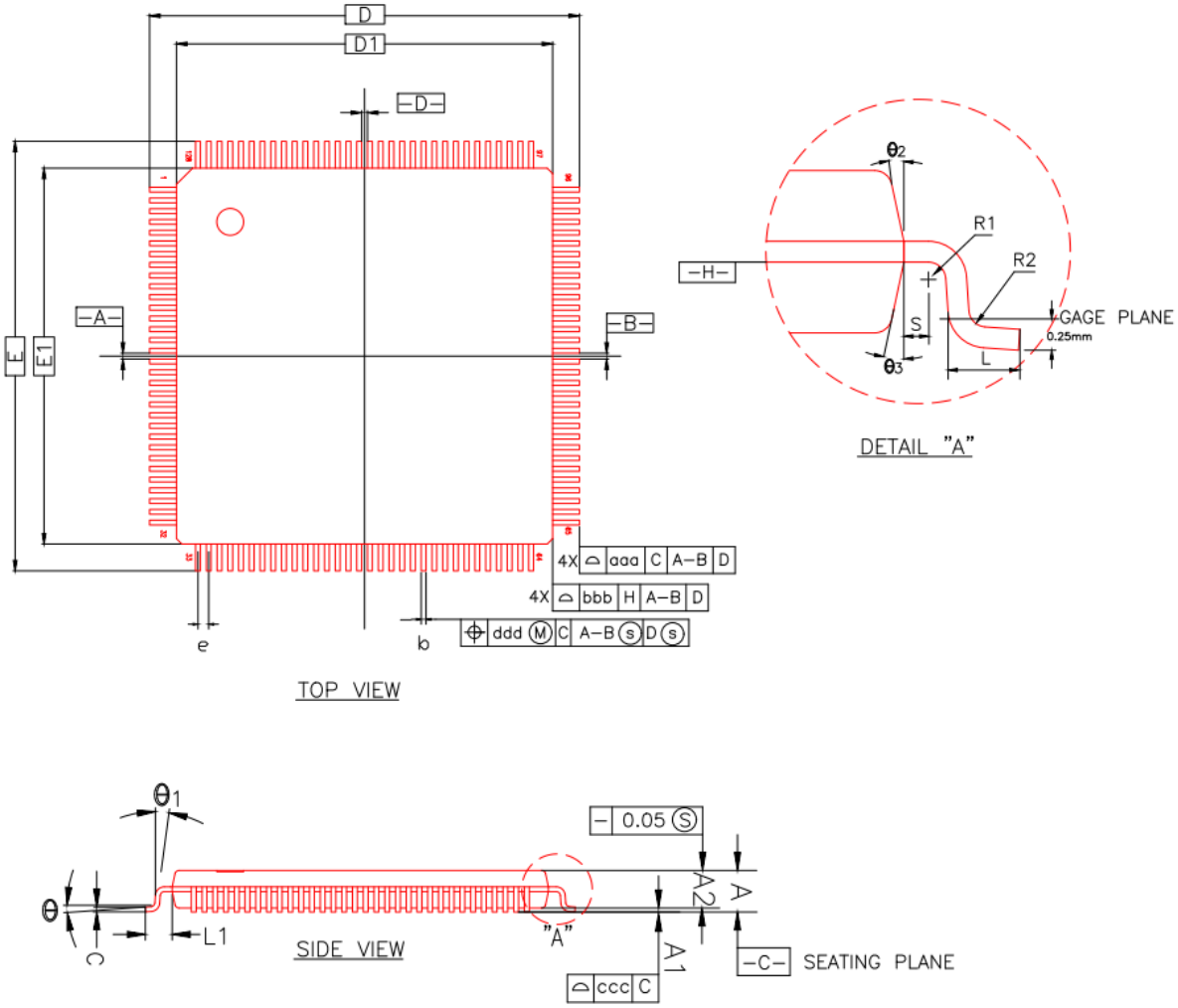
Table 3-11 Power ON Sequence Diagram Key

Symbol	Description	Min	Max	Unit
t1	System 3.3V(2.8V) to BUCK power ready (1.15V)	1	-	ms
t_sys_rstb	system reset time	25	-	ms
t_sys_fall	system 3.3V fall from 3.3V to 2.6V	150	-	us
t_sys_rise	system 3.3V rise from 2.8V to 3.3V	-	10	ms

4 Package Information

4.1 Dimensions - LQFP (14 x 14mm)

Figure 4-1 Package Dimension



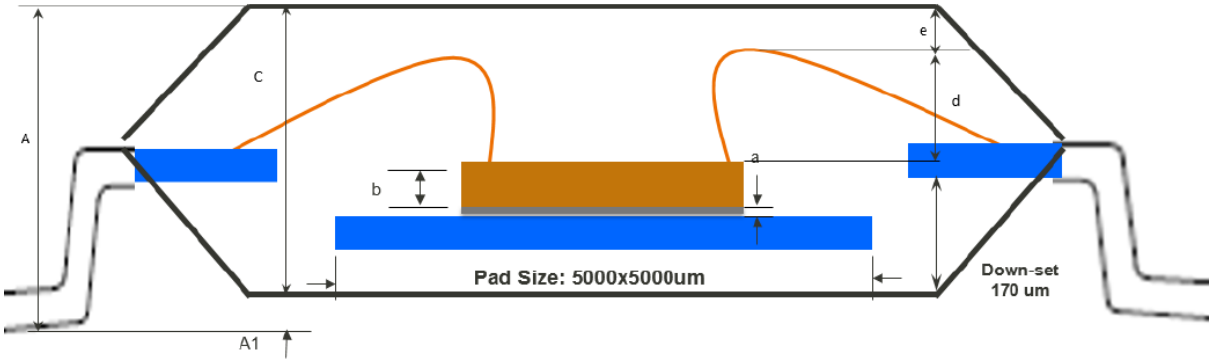
ITEM		SYMBOL	MIN.	NOM.	MAX.
Total height		A	—	—	1.60
Stand off		A1	0.05	—	0.15
Mold thickness		A2	1.35	1.40	1.45
Lead width		b	0.13	0.18	0.23
Outer Lead Distance	X	D	16.00 BSC.		
	Y	E	16.00 BSC.		
Package size	X	D1	14.00 BSC.		
	Y	E1	14.00 BSC.		
Lead pitch		e	0.40 BSC.		
R 2		R2	0.08	—	0.20
R 1		R1	0.08	—	—
Angle		θ	0°	3.5°	7°
Angle 1		θ1	0°	—	—
Angle 2		θ2	11°	12°	13°
Angle 3		θ3	11°	12°	13°
L/F thickness		c	0.09	—	0.20
L		L	0.45	0.60	0.75
Lead length		L1	1.00 REF		
S		S	0.20	—	—
Package profile of a surface		aaa	0.20		
Package profile of a surface		bbb	0.20		
Lead profile of a surface		ccc	0.08		
Lead position		ddd	0.07		

NOTE:

1. Controlling dimensions are in millimeters.
2. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
3. The pattern of pin 1 fiducially is for reference only.

4.1.1 Diagram Key

Table 4-1 Package Diagram Key



	Description	Symbol	Nominal (um)
Package Stack Up	Die Bond Line Thickness	a	25
	Die Thickness	b	304.8
	Mold Cap Thickness	c	1400
	Max Loop Height	d	355.6
	Max Loop Height to Package Clearance	e	120.7
Package Outline	Overall Package Height	A	1600 max.
	Stand Off	A1	150 max.
	Substrate & Mold Cap Thickness	A2	--
	Solder Ball Size	G	--

4.2 Reflow Profile Guideline

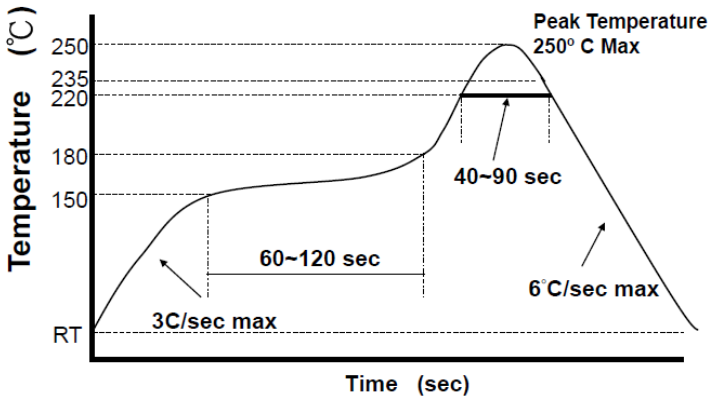


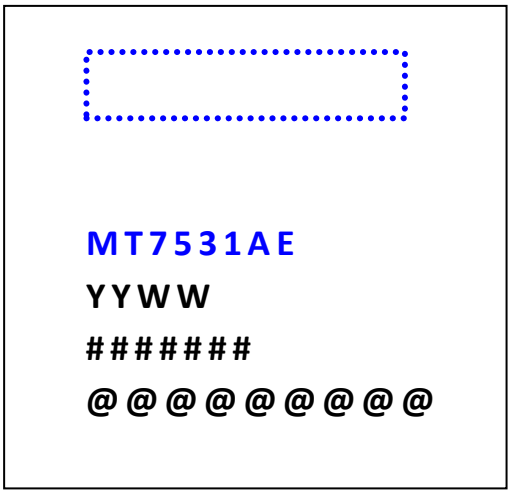
Figure 4-2 Reflow profile

Notes:

1. Reflow profile guideline is designed for SnAgCulead-free solder paste.
2. Reflow temperature is defined at the solder ball of package/or the lead of package.
3. MTK would recommend customer following the solder paste vendor's guideline to design a profile appropriate your line and products.
4. Appropriate N2 atmosphere is recommended since it would widen the process window and mitigate the risk for having solder open issues.

4.3 Top Marking

4.3.1 MT7531AE



Description:

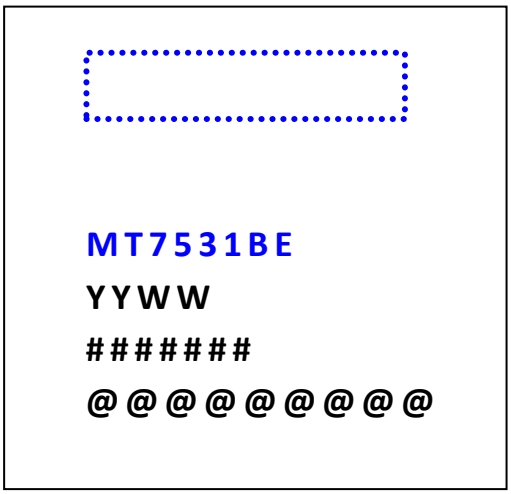
YYWW: Date code

#: LOT NO.

@: Internal control code

Figure 4-3 MT7531AE Top marking

4.3.2 MT7531BE



Description:

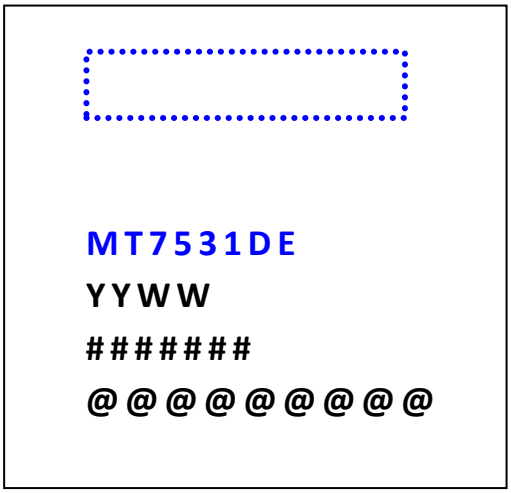
YYWW: Date code

#: LOT NO.

@: Internal control code

Figure 4-4 MT7531BE Top marking

4.3.3 MT7531DE



Description:

YYWW: Date code

#: LOT NO.

@: Internal control code

Figure 4-5 MT7531BE Top marking

4.4 Ordering Information

Part Number	Package (Green/RoHS Compliant)
MT7531AE	14 x 14 mm, 128P-LQFP
MT7531BE	14 x 14 mm, 128P-LQFP
MT7531DE	14 x 14 mm, 128P-LQFP

1.

2.

MediaTek Inc. No. 1, Dusing 1st Rd., Hsinchu Science Park, Hsinchu City, Taiwan, R.O.C
Tel: +886-3-567-0766
Fax: +886-3-568-7610
www.mediatek.com

Figure 4-6