

Field Programmable Crystal Oscillator

Series CPPFX

- Programmed in the field with the PG-3200 oscillator programming instrument within seconds.
- Factory Programmable
- Can be programmed twice
- Standard Package Options
- Also available in 2.7V

Instrument Part Number:

CPPFXC1LZ-A5B6-XX.XXXX TS

CPPFX
SERIES
CPPFX

C
OUTPUT
C = CMOS
T = TTL

1
PACKAGE STYLE
1 = Full Size
4 = Half Size
5 = 3.2x5 Ceramic
7 = 5x7 Ceramic
8 = PLASTIC SMD

L
VOLTAGE
Blank = 5V
L = 3.3V
R = 2.7V

Z
ADDED FEATURE
Blank = Cut Tape
B = Bulk
T = Tube
Z = Tape and Reel

A5
OPERATING TEMP
Blank = 0°C~+70°C
A3 = -55°C~+125°C
A5 = -20°C~+70°C
A7 = -40°C~+85°C

B6
STABILITY
B6 = ±100PPM
BP = ±50PPM
BR = ±25PPM

XX.XXXX
FREQUENCY
0.50 ~ 133.00MHz

TS
TRI-STATE
TS = Tri-State
PD = Power Down

Specifications:

Description	Min	Typ	Max	Unit
Frequency Range: Programmable to any discrete frequency	0.500		133	MHz
Available Stability Options:	-100 -50 -25		+100 +50 +25	PPM
Programmable Supply Voltage: (1-133 MHz) (1-100 MHz) (1-66.0 MHz)	4.5 3.0 2.5	5.0 3.3 2.7	5.5 3.6 3.0	V V V
Operating Temperature Range Options:	-55 -20 -40		+125 +70 +85	°C °C °C
Storage Temperature:	-55		+125	°C
Aging: Ta=°25C,Vdd=5V/3.3V			±5	PPM/Year

Programmable Output Level:

CMOS/TTL

Operating Conditions:

Description	Min	Max	Unit
V_{DD} Supply Voltage	2.7	5.5	V
C_{TTL} Max capacitive load on outputs for TTL levels 4.5V-5.5V V _{DD} , ≤ 40 MHz 4.5V-5.5V V _{DD} , 40 - 133 MHz		50 25	pF pF
C_{CMOS} Max capacitive load on outputs for CMOS levels 4.5V-5.5V V _{DD} , ≤ 66 MHz 4.5V-5.5V V _{DD} , 66 - 133 MHz 3.0V-3.6V V _{DD} , ≤ 40 MHz 3.0V-3.6V V _{DD} , 40 - 100 MHz 2.5-3.0V V _{DD} , ≤ 66 MHz		50 25 30 15 25	pF pF pF pF pF

Output Clock Switching Characteristics:

Description	Test Conditions	Min	Typ	Max	Unit
Duty Cycle:	≤ 50 MHz, $C_L = 50$ pF	45	-	55	%
TTL @ 1.4V	50 - 66 MHz, $C_L = 15$ pF	45	-	55	%
4.5-5.5 V_{DD}	66 - 125 MHz, $C_L = 25$ pF	40	-	60	%
	125 - 133 MHz, $C_L = 15$ pF	40	-	60	%
Duty Cycle:	≤ 66 MHz, $C_L \leq 25$ pF	45	-	55	%
CMOS @ $V_{DD}/2$	66 - 125 MHz, $C_L \leq 25$ pF	40	-	60	%
4.5-5.5 V_{DD}	125 - 133 MHz, $C_L \leq 15$ pF	60	-	60	%
					%
3.0-3.6 V_{DD}	≤ 40 MHz, $C_L \leq 30$ pF	45	-	55	%
	40 - 100 MHz, $C_L \leq 15$ pF	40	-	60	%
Rise/Fall:	0.8V - 2.0V, 4.5 - 5.5 V_{DD} , $C_L = 50$ pF			1.8	ns
	0.8V - 2.0V, 4.5 - 5.5 V_{DD} , $C_L = 25$ pF			1.2	ns
	0.8V - 2.0V, 4.5 - 5.5 V_{DD} , $C_L = 15$ pF			0.9	ns
	0.2V - 0.8 * V_{DD} , 4.5 - 5.5 V_{DD} , $C_L = 50$ pF			3.4	ns
	0.2V - 0.8 * V_{DD} , 3.0 - 3.6 V_{DD} , $C_L = 30$ pF			4.0	ns
	0.2V - 0.8 * V_{DD} , 3.0 - 3.6 V_{DD} , $C_L = 15$ pF			2.4	ns
Start Up Time	From Power On	-	-	2	ms
Power Down Delay Time	PWR_DOWN pin LOW to output Hi-Z,				
Synchronous	T = Frequency Oscillator Period		T/2	T+10	ns
Asynchronous			10	15	ns
Output Disable Time	OE pin LOW to output Hi-Z,				
Synchronous	T = Frequency Oscillator Period		T/2	T+10	ns
Asynchronous			10	15	ns
Output Enable Time				100	ns
RMS Period Jitter	≤ 33.000 MHz		11	13	ps
	> 33.000 MHz		8	11	ps
Peak to Peak*	≤ 33.000 MHz		80	110	ps
	> 33.000 MHz		65	80	ps

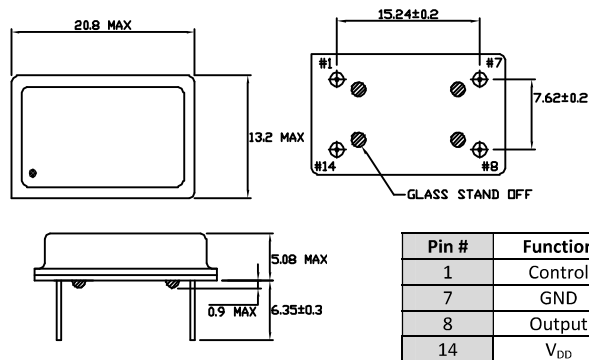
* Jitter Tested at $> 1,000,000$ samples, exceeding JEDEC std JESD65

Electrical Characteristics:

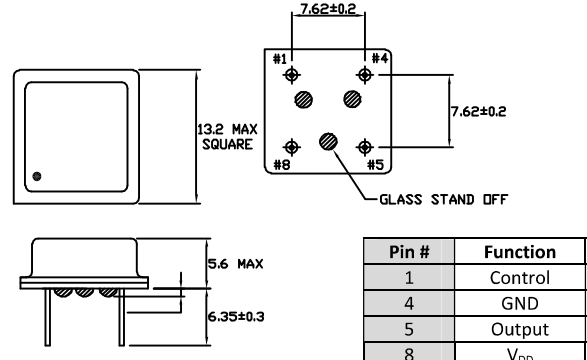
Description	Test Conditions	Min	Typ	Max	Unit
Input Characteristics (Pin 1):					
V _{IL} , Low-Level Input Voltage (To Tri-State or Power Down)	V _{DD} = 5.0 V	-	-	0.8	V
	V _{DD} = 3.3 V	-	-	0.2 * V _{DD}	V
	V _{DD} = 2.7 V	-	-	0.2 * V _{DD}	V
V _{IH} , High-Level Input Voltage (To Enable Output or Open)	V _{DD} = 5.0 V	2.0	-	-	V
	V _{DD} = 3.3 V	0.7 * V _{DD}	-	-	V
I _{IL} , Input Low Current	V _{IN} = 0 V	-	-	10	μA
I _{IH} , Input High Current	V _{IN} = V _{DD}	-	-	5	μA
Output Characteristics:					
V _{OL} , Low-Level Output Voltage	V _{DD} = 5.0 V, I _{OL} = 16mA	-	-	0.4	V
	V _{DD} = 3.3 V, I _{OL} = 8mA	-	-	0.4	V
V _{IHTTL} , High-Level Output Voltage	V _{DD} = 5.0 V, I _{OL} = -16mA	2.4	-	-	V
V _{IHCMOS} , High-Level Output Voltage	V _{DD} = 5.0 V, I _{OL} = -16mA	V _{DD} -0.4	-	-	V
	V _{DD} = 3.3 V, I _{OL} = -8mA	V _{DD} -0.4	-	-	V
Power Supply Current: (Unloaded)	V _{DD} = 5.0 V, F _O ≤ 133 MHz	-	-	45	mA
	V _{DD} = 3.3 V, F _O ≤ 100 MHz	-	-	25	mA
	V _{DD} = 2.7 V, F _O ≤ 66.0 MHz	-	-	20	mA
Standby Current:		-	10	50	μA
Tri-State Leakage Current	V _{DD} = 5.0 V	-	20	-	μA
Output Enable Mode:	Output is Tri-Stated				
Power Down Mode:	Output is Tri-Stated				

*Note: Bypass V_{DD} to GND with a 0.01 μ F capacitor

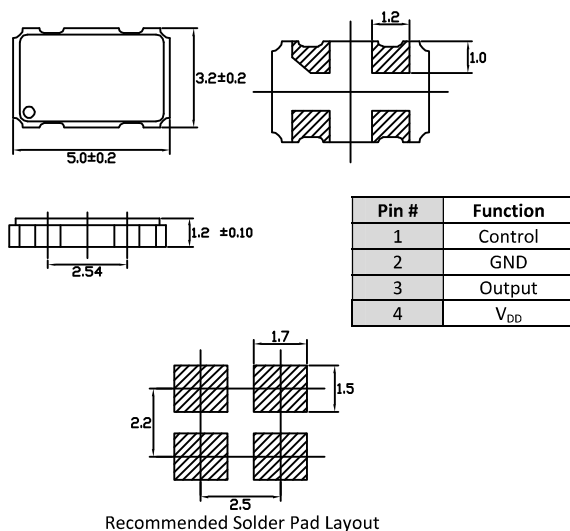
Style 1 Full Size 14 Pin Dip



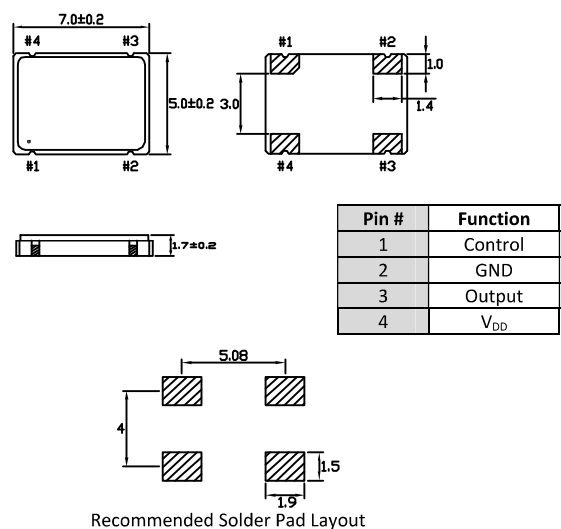
Style 4 Half Size 8 Pin Dip



Style 5 3.2x5 Ceramic SMD



Style 7 5x7 Ceramic SMD



*Note: Bypass V_{DD} to GND with a 0.01 μ F capacitor

Style 8 Plastic SMD

