Features

- Green Device Available
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

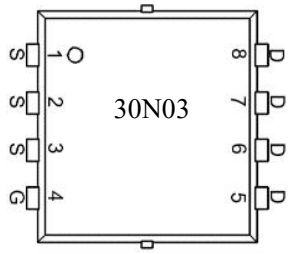
Bvdss	Rdson	ID
30V	8mΩ	30A

Application

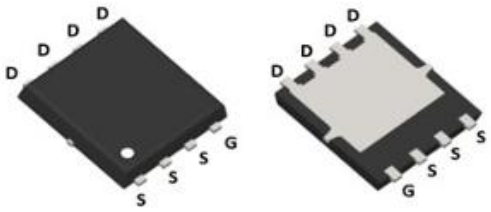
- DC-DC Converters
- Power management functions
- Synchronous-rectification applications

RoHS

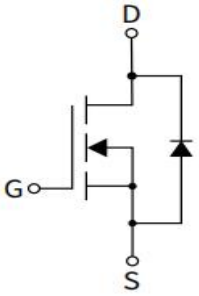
Package



Marking and pin assignment



PDFN3*3-8L top view



Schematic diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Quantity
30N03	30N03D	PDFN3*3-8L	5000

Absolute Maximum Ratings (T_J=25℃ unless otherwise specified)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current, V_{GS}@10V[1]	T_A=25℃	I_D	30	A
	T_A=70℃		20	A
Pulsed Drain Current[2]		I_{DM}	90	A
Single Pulsed Avalanche Energy[3]		E_{AS}	39	mJ
Avalanche Current		I_{AS}	30	A
Power Dissipation[4]		P_D@T_A=25℃	15	W
Operating Junction Temperature Range		T_J	-55~+150	℃
Storage Temperature Range		T_{STG}	-55~+150	℃

Thermal Resistance Ratings

Parameter	Symbol	Typ.	Max.	Unit
Thermal Resistance,Junction-to-Case	$R_{\theta JC}$	--	--	℃/W
Thermal Resistance,Junction-to-Ambient[1]	$R_{\theta JA}$	--	85	℃/W

Ordering Information

Ordering Number	Package	Pin Assignment			Packing
Halogen Free		G	D	S	
HL30N03D	PDFN3*3-8L	4	5,6,7,8	1,2,3	Tape Reel

Electrical Characteristics (T_J=25℃,unless otherwise specified)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{DSS}	V_{GS}=0V,I_D=250μA	30	-	-	V
BV_{DSS} Temperature Coefficient	$\triangle BV_{DSS}/\triangle T_J$	Reference to 25℃, I_D=1mA	-	0.034	-	V/℃
Drain-Source Leakage Current	I_{DSS}	V_{DS}=24V,V_{GS}=0V,T_J=25℃	-	-	1	μA
		V_{DS}=24V,V_{GS}=0V,T_J=55℃	-	-	5	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS},I_D=250μA	1.2	1.5	2.5	V
Static Drain-Source On-Resistance[2]	$R_{DS(on)}$	V_{GS}=10V, I_D=7A	-	8	12	mΩ
		V_{GS}=4.5V, I_D=4A	-	11	18	
Gate Resistance	R_g	V_{DS}=0V,V_{GS}=0V,f=1MHz	-	1.04	2.1	Ω
Input Capacitance	C_{lss}	V_{DS}=15V,V_{GS}=0V, f=1MHz	-	816	-	pF
Output Capacitance	C_{oss}		-	107.8	-	
Reverse Transfer Capacitance	C_{rss}		-	82.6	-	
Total Gate Charge(4.5V)	Q_g	V_{DS}=15V,V_{GS}=4.5V, I_D=7A	-	8.4	-	nC
Gate-Source Charge	Q_{gs}		-	3.1	-	
Gate-Drain Charge	Q_{gd}		-	2.8	-	
Turn-on Delay Time	$T_{d(on)}$	V_{GS}=10V,V_{DD}=15V, R_G=3.3Ω,I_D=7A	-	2.4	-	nS
Turn-on Rise Time	T_r		-	72	-	
Turn-Off Delay Time	$T_{d(off)}$		-	36	-	
Turn-Off Fall Time	T_f		-	14.4	-	
Continuous Source Current[1,5]	I_S	V_G=V_D=0V,Force Current	-	-	30	A
Pulsed Source Current[2,5]	I_{SM}		-	-	30	A
Diode Forward Voltage[2]	V_{SD}	V_{GS}=0V,I_S=1A,T_J=25℃	-	-	1.2	V

Notes:

1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.

2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%.

3.The EAS data shows Max. rating . The test condition is V_{DD}=25V,V_{GS}=10V,L=0.1mH,I_{AS}=20A.

4.The power dissipation is limited by 150℃ junction temperature.

5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Performance Characteristics

Figure1: Output Characteristics

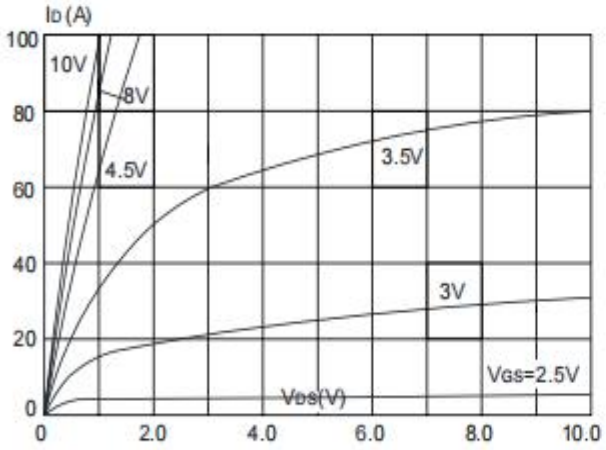


Figure 2: Typical Transfer Characteristics

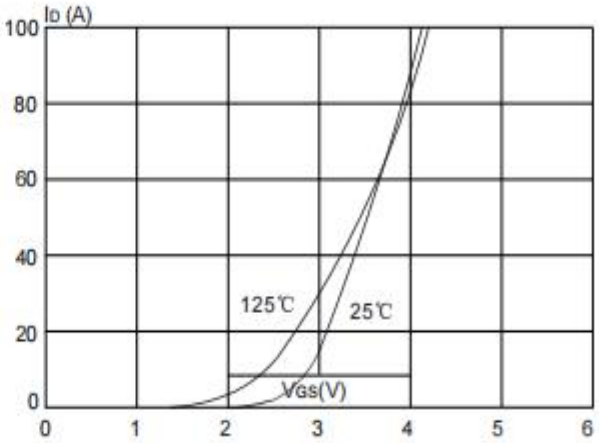


Figure 3: On-resistance vs. Drain Current

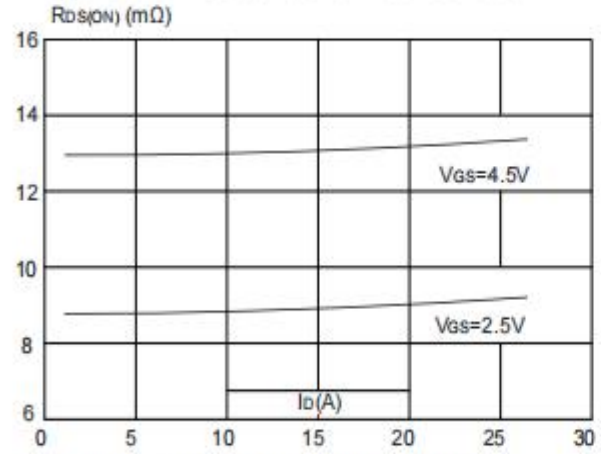


Figure 4: Body Diode Characteristics

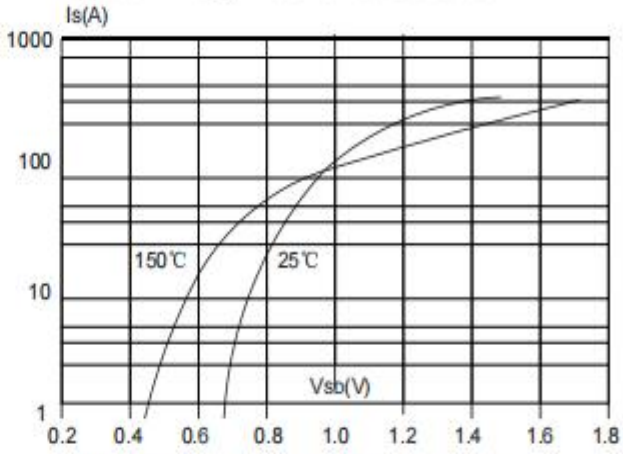


Figure 5: Gate Charge Characteristics

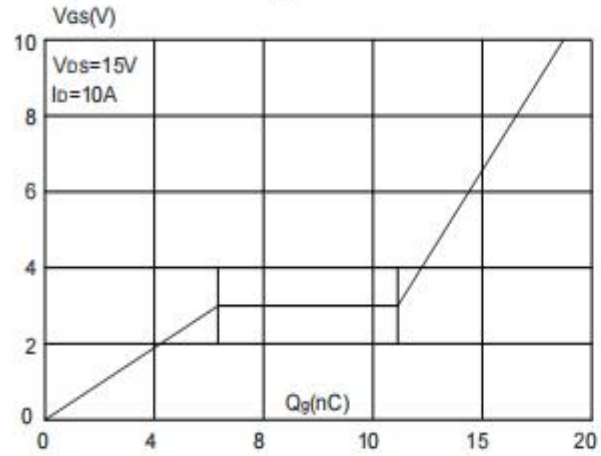


Figure 6: Capacitance Characteristics

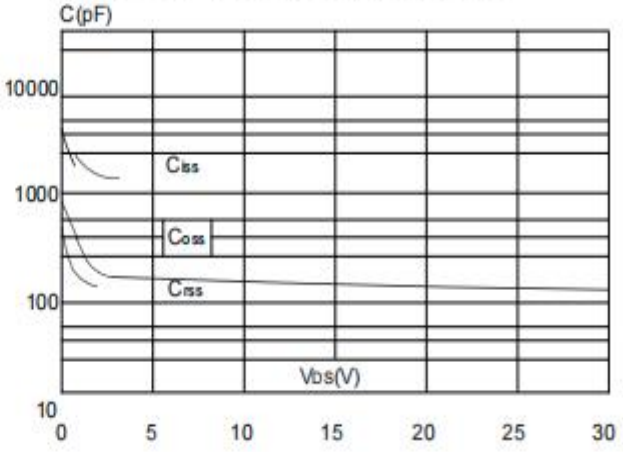


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

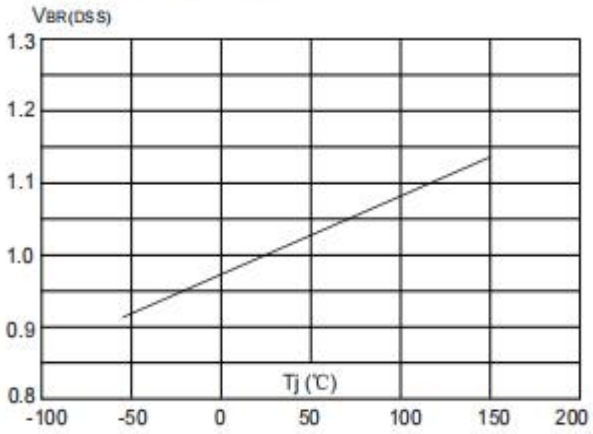


Figure 8: Normalized on Resistance vs. Junction Temperature

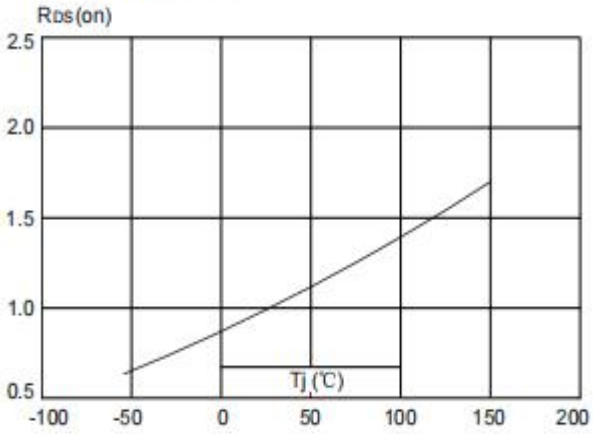


Figure 9: Maximum Safe Operating Area

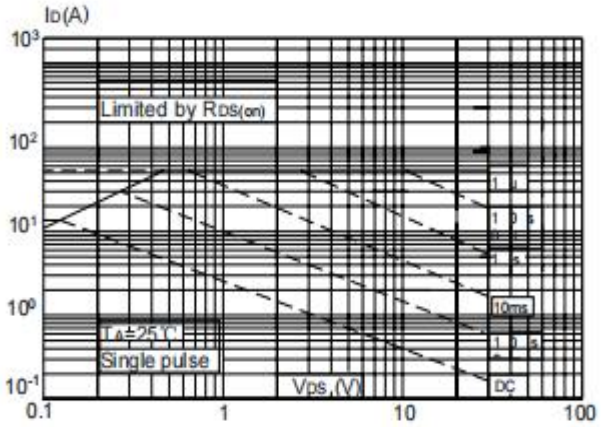


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

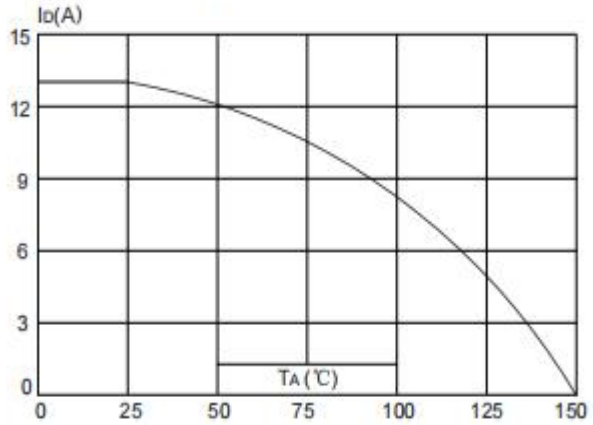
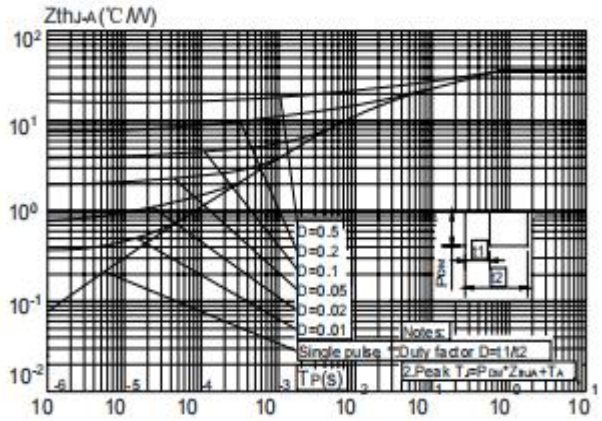


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



Test Circuit

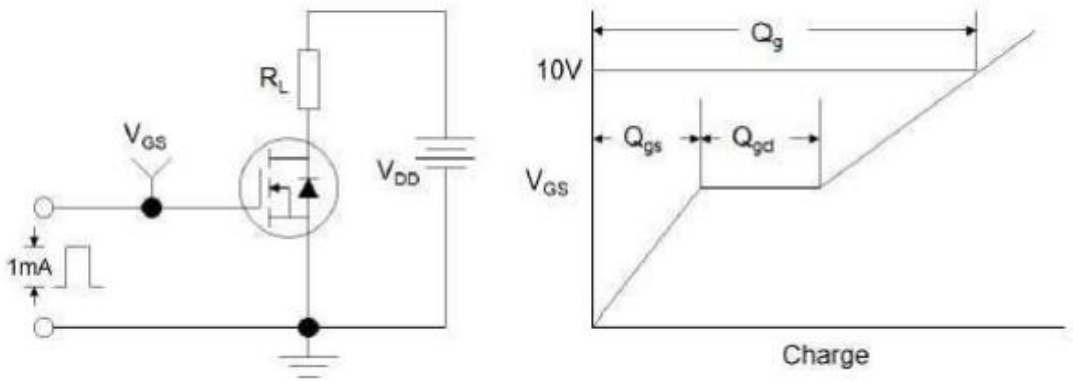


Figure1:Gate Charge Test Circuit & Waveform

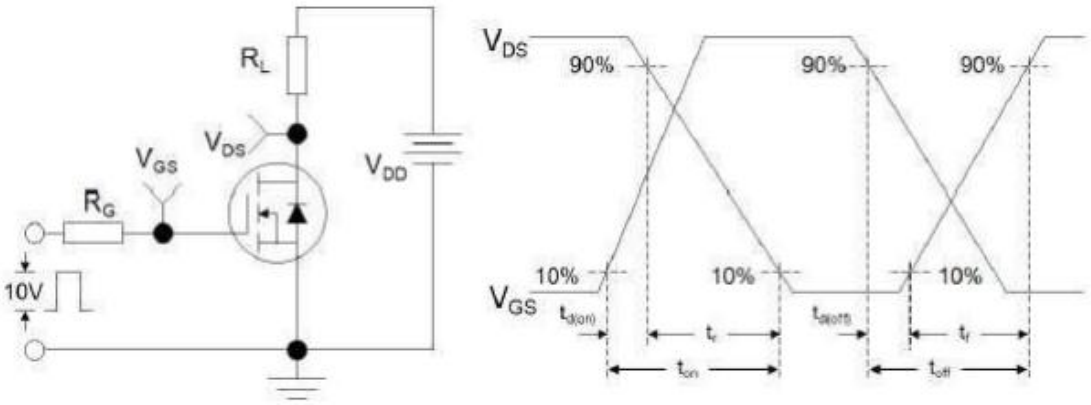


Figure 2: Resistive Switching Test Circuit & Waveforms

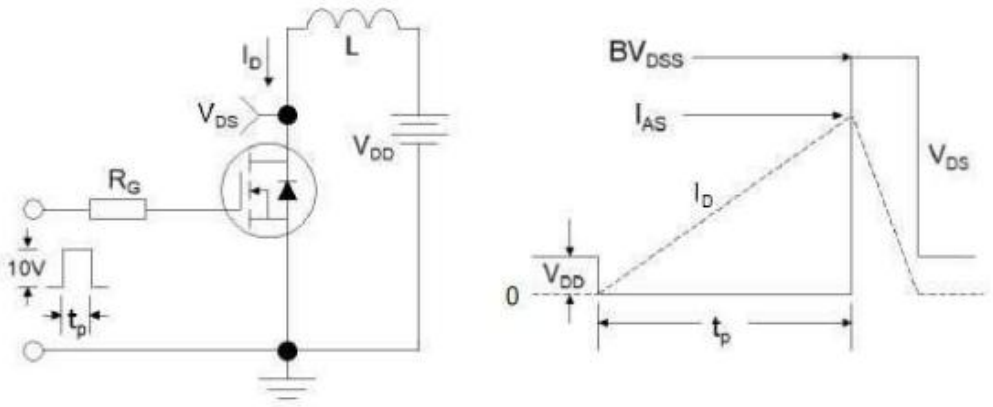
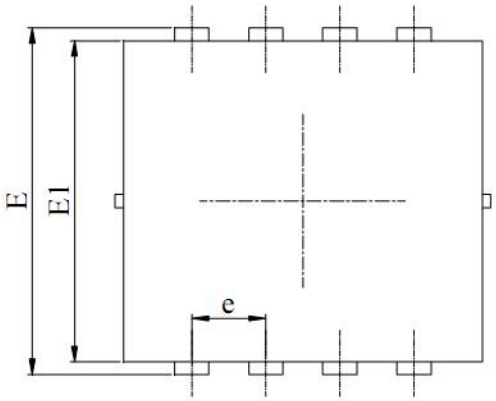
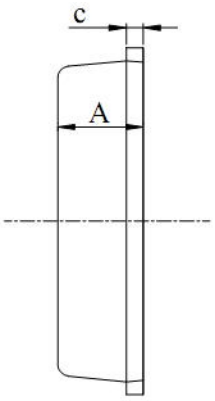


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms

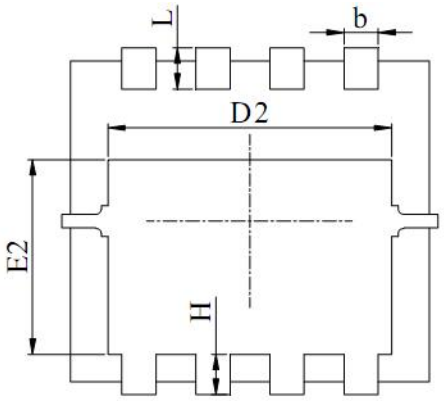
Package Dimensions PDFN3x3-8L



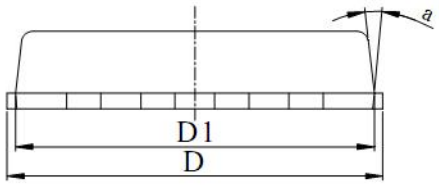
Top View



Side View



Bottom View

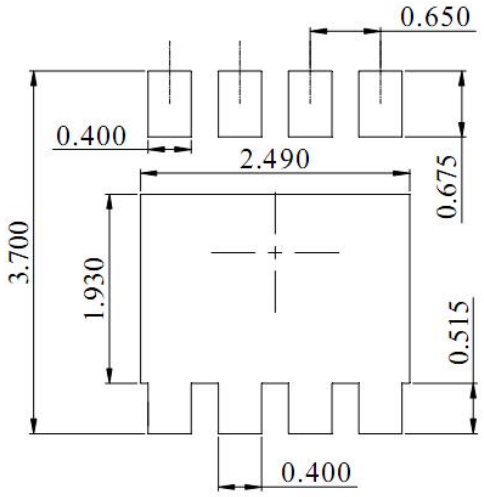


Front View

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. ALL DIMNESIONS IN MILLIMETER (ANNGLE IN DEGREE).
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM.	MILLIMETER		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.20	0.25
D	3.00	3.15	3.25
D1	2.95	3.05	3.15
D2	2.39	2.49	2.59
E	3.20	3.30	3.40
E1	2.95	3.05	3.15
E2	1.70	1.80	1.90
e		0.65 BSC	
H	0.30	0.40	0.50
L	0.25	0.40	0.50
a	---	---	15°



DIMENSIONS:MILLIMETERS

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