

# IPW65R041CFD7XKSA1-VB Datasheet

## SJ\_Multi-EPI TO247 Single-N 650V MOSFET

### PRODUCT SUMMARY

$V_{DS}$ (V) at $T_J$ max.	700	
$R_{DS(on)}$ at 25 °C ( $\Omega$ )	$V_{GS} = 10\text{ V}$	0.06
$Q_g$ max. (nC)	273	
$Q_{gs}$ (nC)	46	
$Q_{gd}$ (nC)	79	
Configuration	Single	

### FEATURES

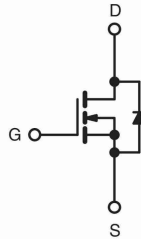
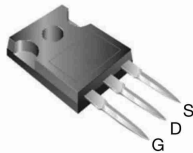
- Low figure-of-merit (FOM)  $R_{on} \times Q_g$
- Low input capacitance ( $C_{iss}$ )
- Reduced switching and conduction losses
- Ultra low gate charge ( $Q_g$ )
- Avalanche energy rated (UIS)


**RoHS**  
 COMPLIANT

### APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Industrial
  - Welding
  - Induction heating
  - Motor drives
  - Battery chargers
  - Renewable energy
  - Solar (PV inverters)

TO-247AC



N-Channel MOSFET


### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ °C}$ , unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V <sub>DS</sub>	650	V
Gate-Source Voltage			V <sub>GS</sub>	± 30	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 25 °C	I <sub>D</sub>	47	A
		T <sub>C</sub> = 100 °C		30	
Pulsed Drain Current <sup>a</sup>			I <sub>DM</sub>	142	
Linear Derating Factor				3.3	W/°C
Single Pulse Avalanche Energy <sup>b</sup>			E <sub>AS</sub>	1410	mJ
Maximum Power Dissipation			P <sub>D</sub>	415	W
Operating Junction and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C
Drain-Source Voltage Slope	T <sub>J</sub> = 125 °C		dV/dt	37	V/ns
Reverse Diode dV/dt <sup>d</sup>				9	
Soldering Recommendations (Peak Temperature) <sup>c</sup>	for 10 s			300	°C

#### Notes

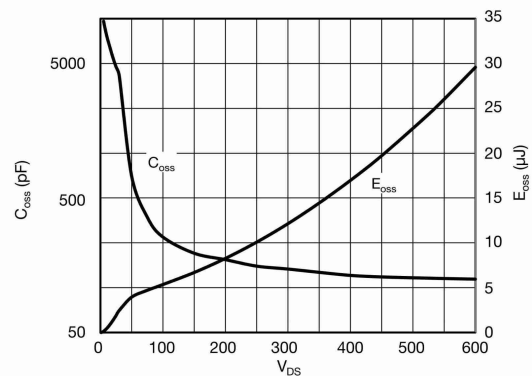
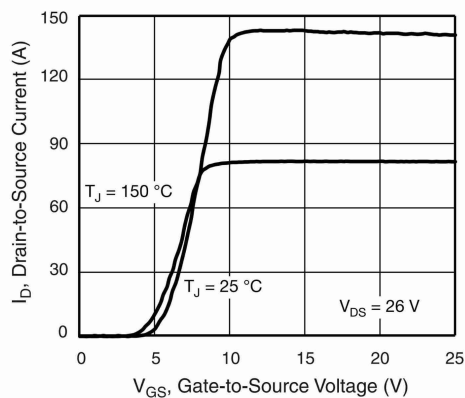
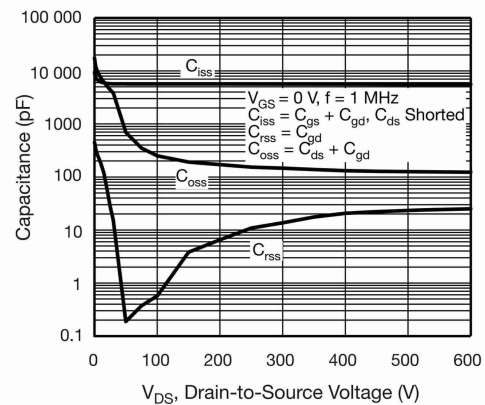
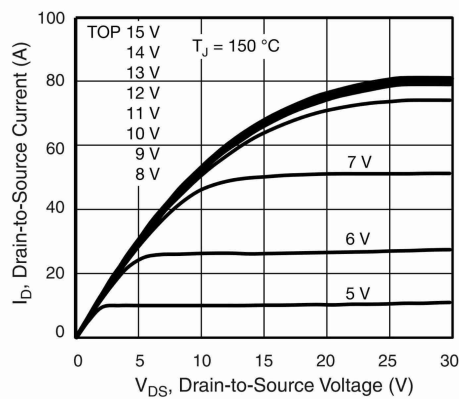
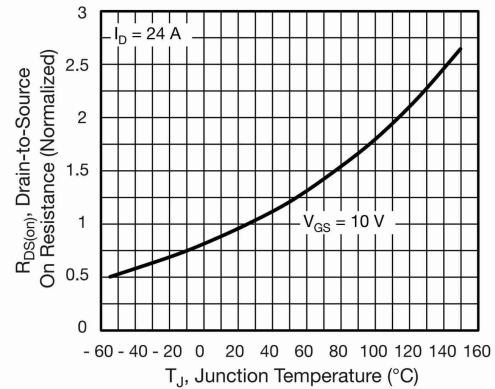
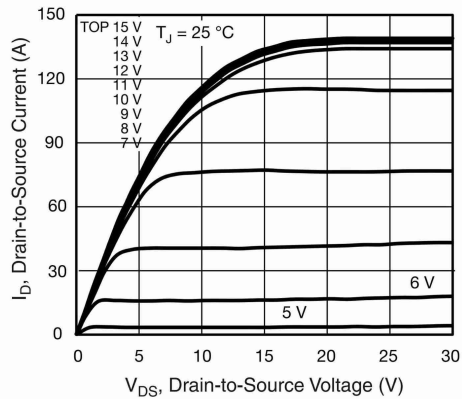
- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50\text{ V}$ , starting  $T_J = 25\text{ °C}$ ,  $L = 28.2\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 10\text{ A}$ .
- 1.6 mm from case.
- $I_{SD} \leq I_D$ ,  $dI/dt = 100\text{ A}/\mu\text{s}$ , starting  $T_J = 25\text{ °C}$ .

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	40	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	0.3	

SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		650	-	-	V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	0.70	-	V/°C
Gate-Source Threshold Voltage (N)	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2	-	4	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
		V <sub>GS</sub> = ± 30 V		-	-	± 1	μA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 650 V, V <sub>GS</sub> = 0 V		-	-	1	μA
		V <sub>DS</sub> = 520 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	-	25	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 24 A	-	0.06	-	Ω
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 30 V, I <sub>D</sub> = 24 A		-	16.7	-	S
Dynamic							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 100 V, f = 1 MHz		-	5682	-	pF
Output Capacitance	C <sub>oss</sub>			-	251	-	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	1	-	
Effective Output Capacitance, Energy Related <sup>a</sup>	C <sub>o(er)</sub>	V <sub>DS</sub> = 0 V to 520 V, V <sub>GS</sub> = 0 V		-	192	-	pF
Effective Output Capacitance, Time Related <sup>b</sup>	C <sub>o(tr)</sub>			-	665	-	
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 24 A, V <sub>DS</sub> = 520 V	-	182	273	nC
Gate-Source Charge	Q <sub>gs</sub>			-	46	-	
Gate-Drain Charge	Q <sub>gd</sub>			-	79	-	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 520 V, I <sub>D</sub> = 6 A, V <sub>GS</sub> = 10 V, R <sub>g</sub> = 9.1 Ω		-	47	94	ns
Rise Time	t <sub>r</sub>			-	87	131	
Turn-Off Delay Time	t <sub>d(off)</sub>			-	156	234	
Fall Time	t <sub>f</sub>			-	103	206	
Gate Input Resistance	R <sub>g</sub>	f = 1 MHz, open drain		-	0.64	-	Ω
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	47	A
Pulsed Diode Forward Current	I <sub>SM</sub>			-	-	139	
Diode Forward Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 24 A, V <sub>GS</sub> = 0 V		-	0.9	1.2	V
Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = I <sub>S</sub> = 24 A, dI/dt = 100 A/μs, V <sub>R</sub> = 25 V		-	753	1506	ns
Reverse Recovery Charge	Q <sub>rr</sub>			-	14	28	μC
Reverse Recovery Current	I <sub>RRM</sub>			-	28	-	A

**Notes**

- a.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ .  
 b.  $C_{oss(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ .

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

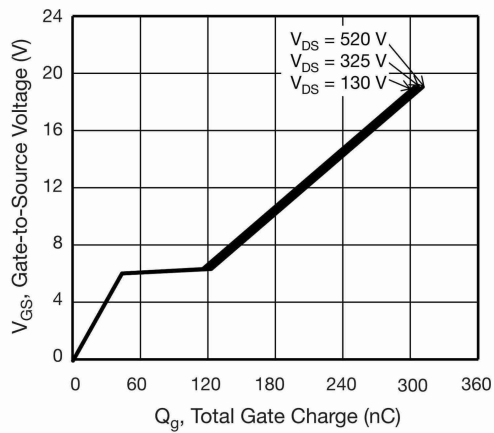


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

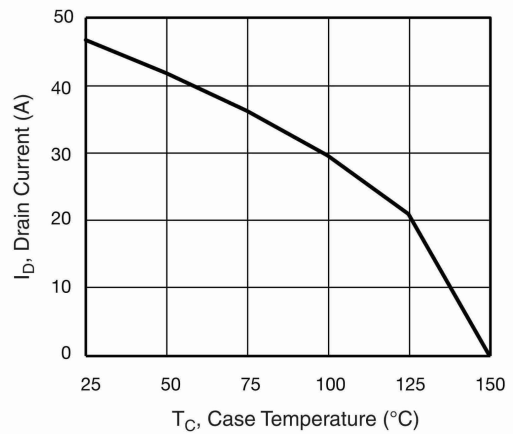


Fig. 10 - Maximum Drain Current vs. Case Temperature

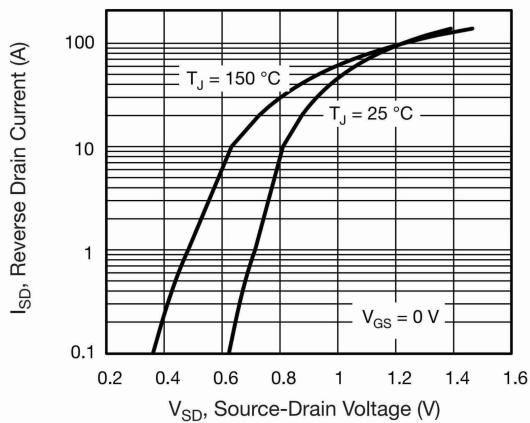


Fig. 8 - Typical Source-Drain Diode Forward Voltage

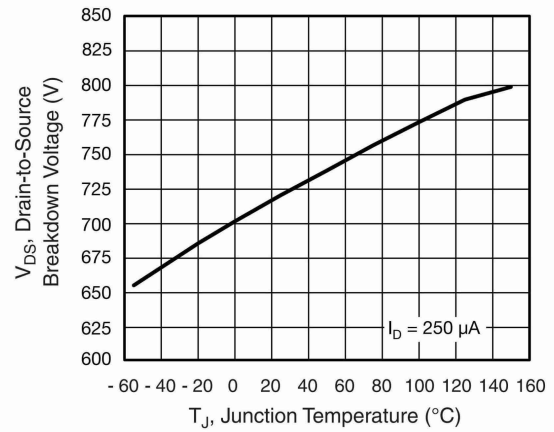


Fig. 11 - Temperature vs. Drain-to-Source Voltage

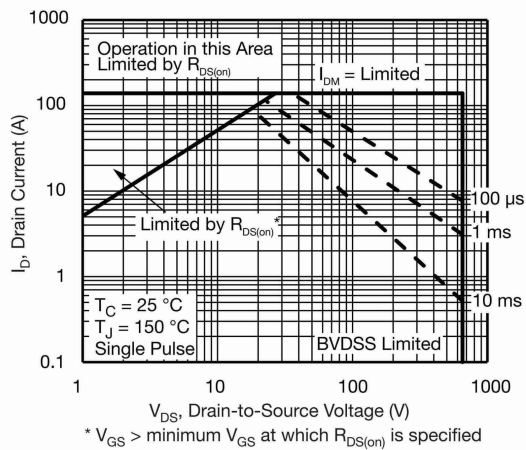


Fig. 9 - Maximum Safe Operating Area

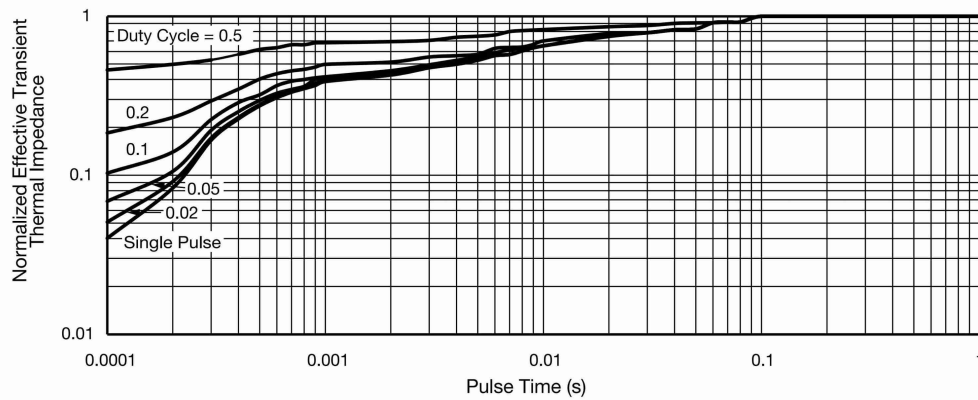


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

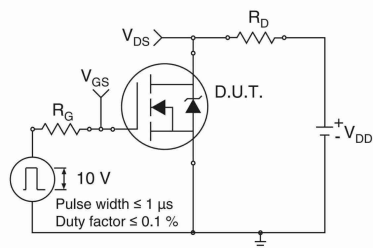


Fig. 13 - Switching Time Test Circuit

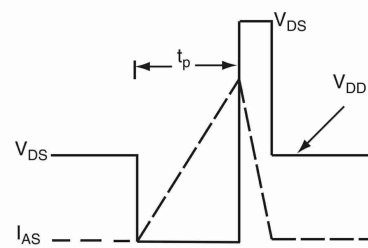


Fig. 16 - Unclamped Inductive Waveforms

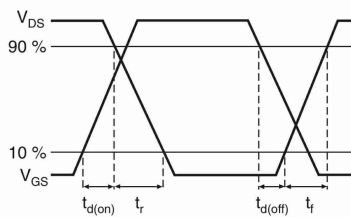


Fig. 14 - Switching Time Waveforms

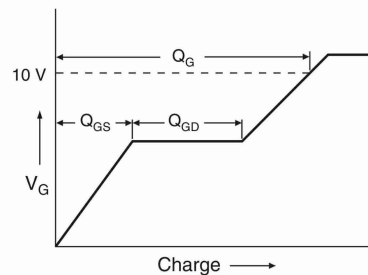


Fig. 17 - Basic Gate Charge Waveform

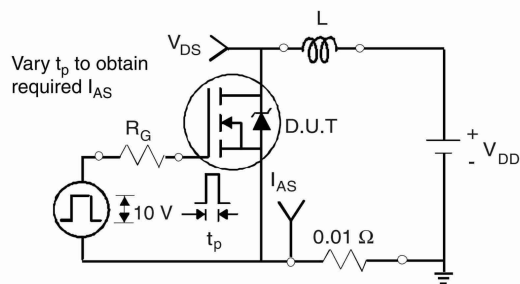


Fig. 15 - Unclamped Inductive Test Circuit

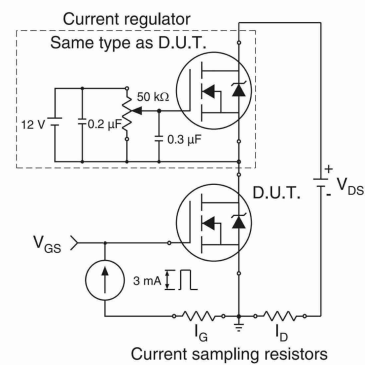
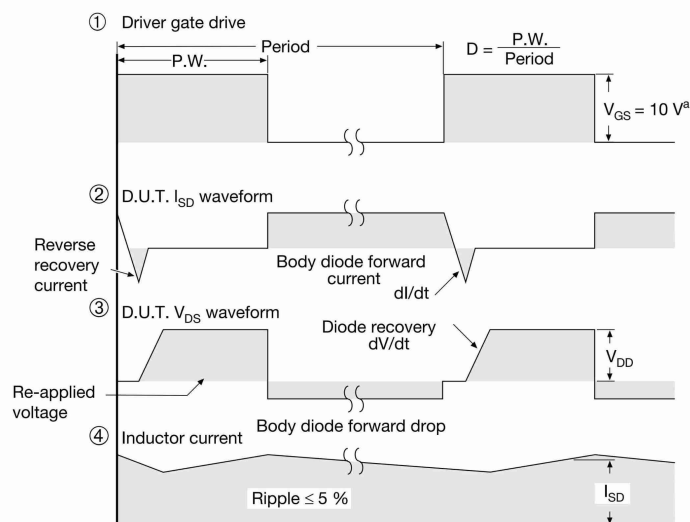
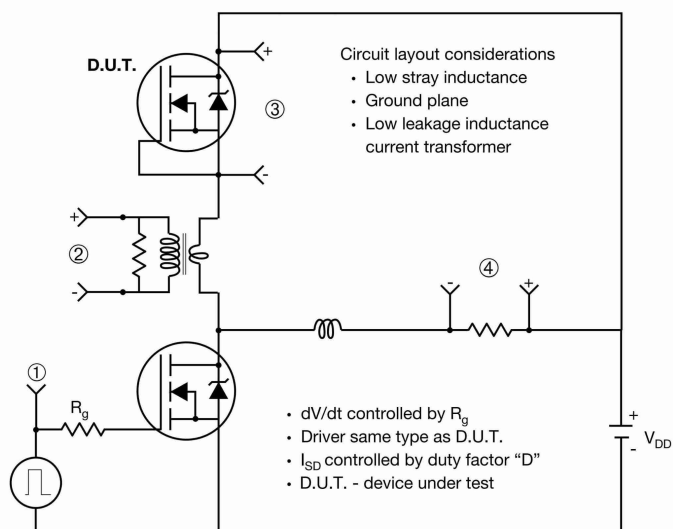


Fig. 18 - Gate Charge Test Circuit

### Peak Diode Recovery dV/dt Test Circuit

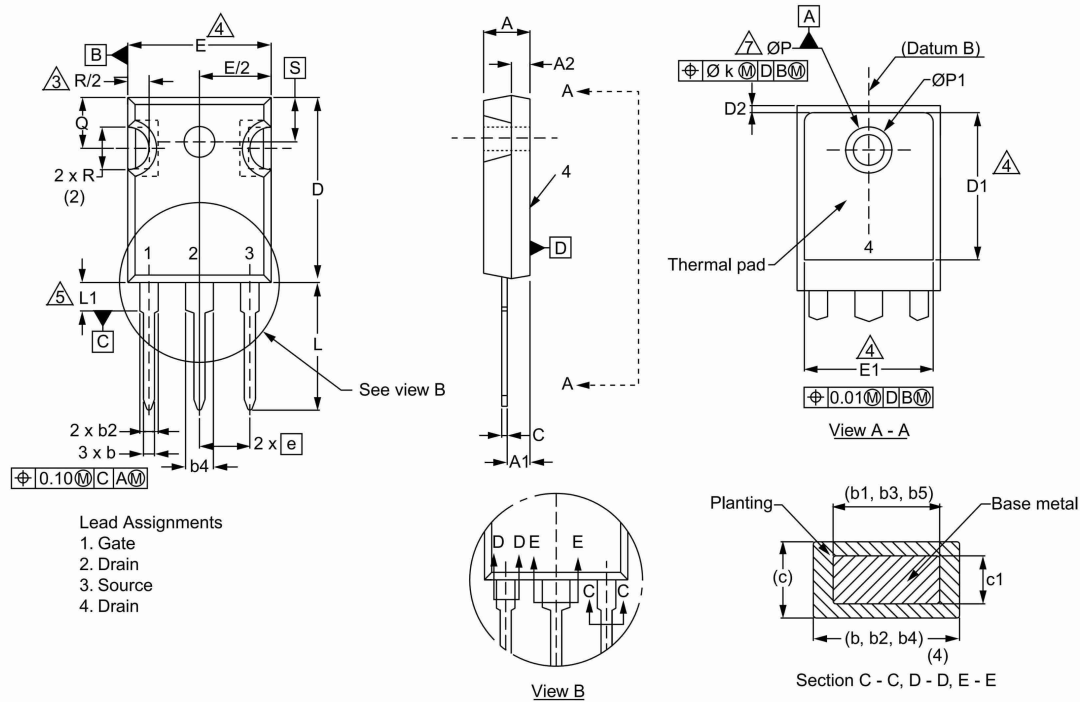


#### Note

a.  $V_{GS} = 5 V$  for logic level devices

Fig. 19 - For N-Channel

TO-247AC (High Voltage)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.58	5.31	0.180	0.209
A1	2.21	2.59	0.087	0.102
A2	1.17	2.49	0.046	0.098
b	0.99	1.40	0.039	0.055
b1	0.99	1.35	0.039	0.053
b2	1.53	2.39	0.060	0.094
b3	1.65	2.37	0.065	0.093
b4	2.42	3.43	0.095	0.135
b5	2.59	3.38	0.102	0.133
c	0.38	0.86	0.015	0.034
c1	0.38	0.76	0.015	0.030
D	19.71	20.82	0.776	0.820
D1	13.08	-	0.515	-

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D2	0.51	1.30	0.020	0.051
E	15.29	15.87	0.602	0.625
E1	13.72	-	0.540	-
e	5.46 BSC		0.215 BSC	
Ø k	0.254		0.010	
L	14.20	16.25	0.559	0.640
L1	3.71	4.29	0.146	0.169
N	7.62 BSC		0.300 BSC	
Ø P	3.51	3.66	0.138	0.144
Ø P1	-	7.39	-	0.291
Q	5.31	5.69	0.209	0.224
R	4.52	5.49	0.178	0.216
S	5.51 BSC		0.217 BSC	



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