

# CSD19536KTT-VB Datasheet

## 100V Trench TO263 Single-N MOSFET

### PRODUCT SUMMARY

$V_{DS}$ (V)	100
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = 10$ V	0.0030
$I_D$ (A) <sup>a</sup>	180
Configuration	Single

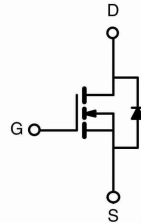
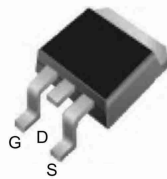
### FEATURES

- TrenchFET® Power MOSFET
- Package with Low Thermal Resistance
- 100 %  $R_g$  and UIS Tested



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

D<sup>2</sup>PAK (TO-263)



N-Channel MOSFET

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ , unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		$V_{DS}$	100	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	
Continuous Drain Current	$T_C = 25^\circ\text{C}^a$	$I_D$	180	A
	$T_C = 125^\circ\text{C}$		140	
Continuous Source Current (Diode Conduction) <sup>a</sup>		$I_S$	180	
Pulsed Drain Current <sup>b</sup>		$I_{DM}$	680	
Single Pulse Avalanche Current	$L = 0.1$ mH	$I_{AS}$	73	
Single Pulse Avalanche Energy		$E_{AS}$	266	mJ
Maximum Power Dissipation <sup>b</sup>	$T_C = 25^\circ\text{C}$	$P_D$	375	W
	$T_C = 125^\circ\text{C}$		125	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	- 55 to + 175	$^\circ\text{C}$

### THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-Ambient	PCB Mount <sup>c</sup>	$R_{thJA}$	40	$^\circ\text{C}/\text{W}$
Junction-to-Case (Drain)		$R_{thJC}$	0.6	

#### Notes

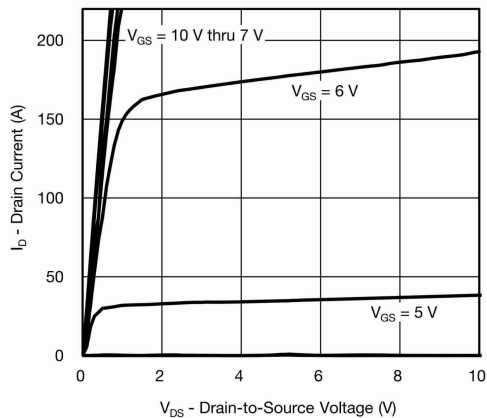
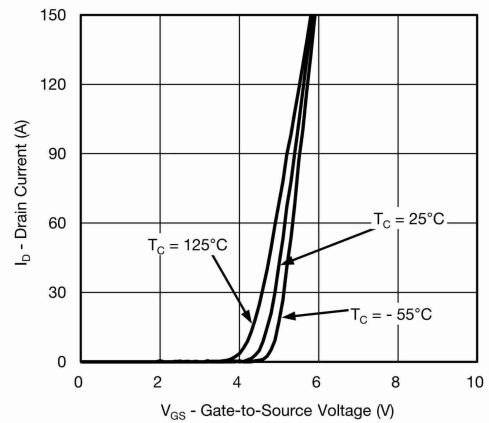
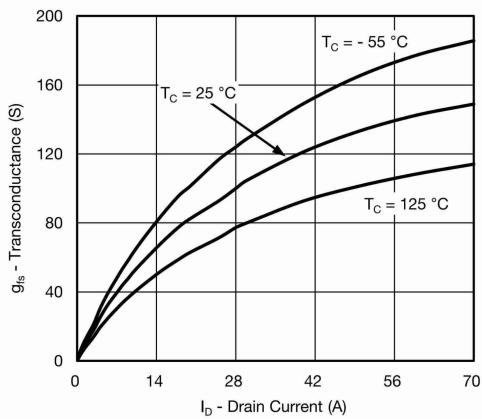
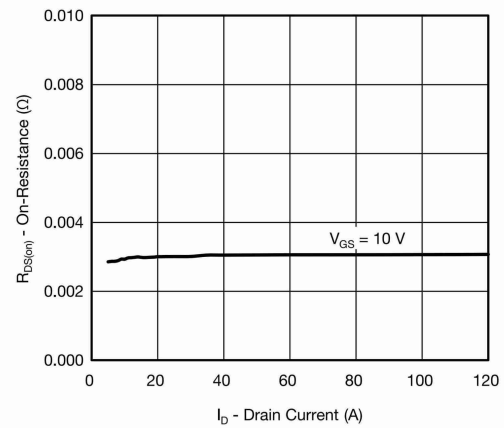
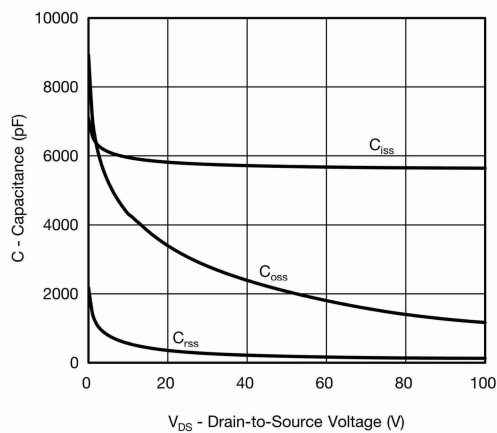
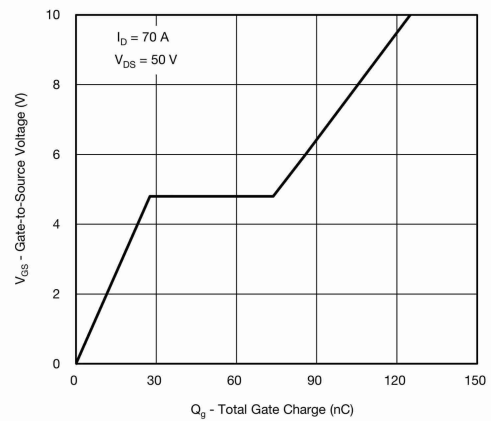
- Base on  $T_C = 25^\circ\text{C}$ .
- Pulse test; pulse width  $\leq 300$   $\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- When mounted on 1" square PCB (FR-4 material).
- Parametric verification ongoing.

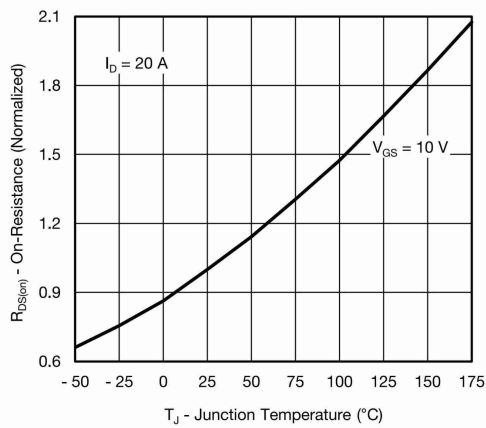
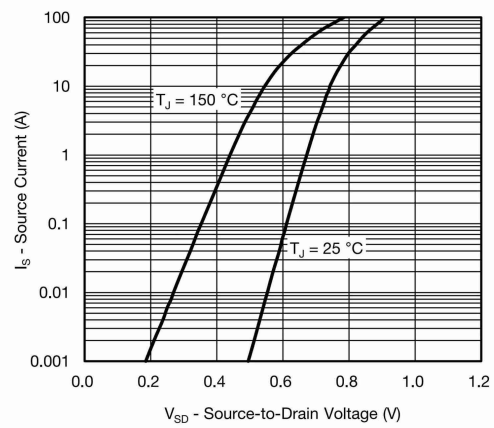
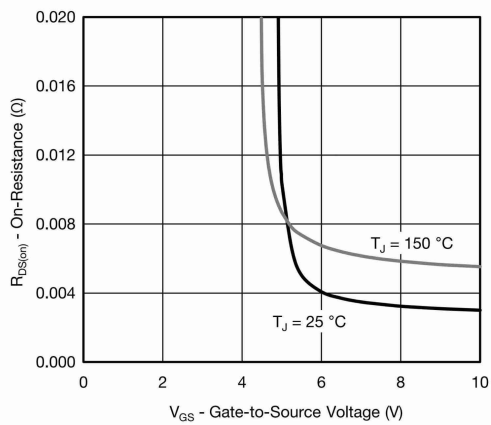
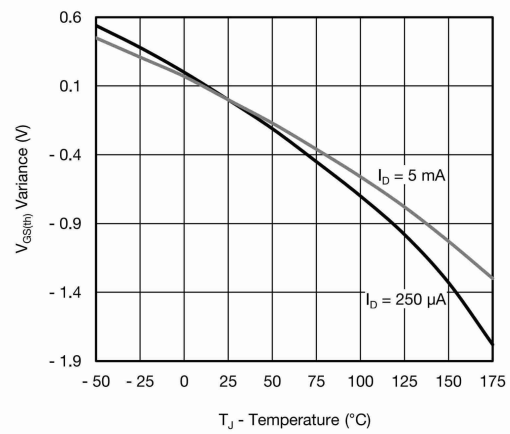
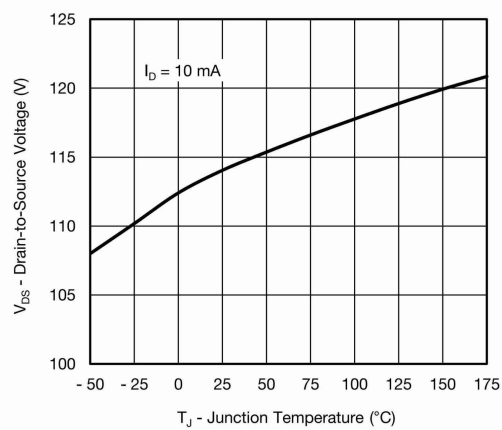
SPECIFICATIONS (T <sub>C</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0, I <sub>D</sub> = 250 μA		100	-	-	V
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2.5	3.0	3.5	
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 100 V	-	-	1	μA
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 100 V, T <sub>J</sub> = 125 °C	-	-	50	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 100 V, T <sub>J</sub> = 175 °C	-	-	500	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V	V <sub>DS</sub> ≥ 5 V	120	-	-	A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A	-	0.0030	-	Ω
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A, T <sub>J</sub> = 125 °C	-	0.0064	-	
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A, T <sub>J</sub> = 175 °C	-	0.0080	-	
Forward Transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 20 A		-	82	-	S
Dynamic <sup>b</sup>							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 25 V, f = 1 MHz	-	5780	7230	pF
Output Capacitance	C <sub>oss</sub>			-	3070	3840	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	305	385	
Total Gate Charge <sup>c</sup>	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 70 A	-	125	190	nC
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>			-	28	-	
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			-	46	-	
Gate Resistance	R <sub>g</sub>	f = 1 MHz		1.6	3.3	5	Ω
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = 50 V, R <sub>L</sub> = 0.7 Ω I <sub>D</sub> ≈ 70 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω		-	16	25	ns
Rise Time <sup>c</sup>	t <sub>r</sub>			-	110	165	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			-	40	60	
Fall Time <sup>c</sup>	t <sub>f</sub>			-	12	20	
Source-Drain Diode Ratings and Characteristics <sup>b</sup>							
Pulsed Current <sup>a</sup>	I <sub>SM</sub>			-	-	480	A
Forward Voltage	V <sub>SD</sub>	I <sub>F</sub> = 100 A, V <sub>GS</sub> = 0		-	0.9	1.5	V

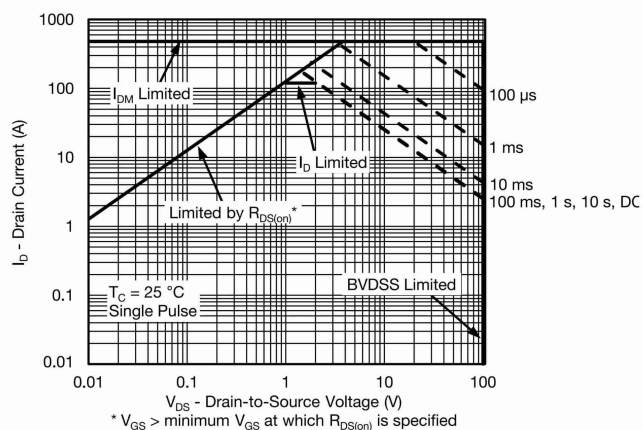
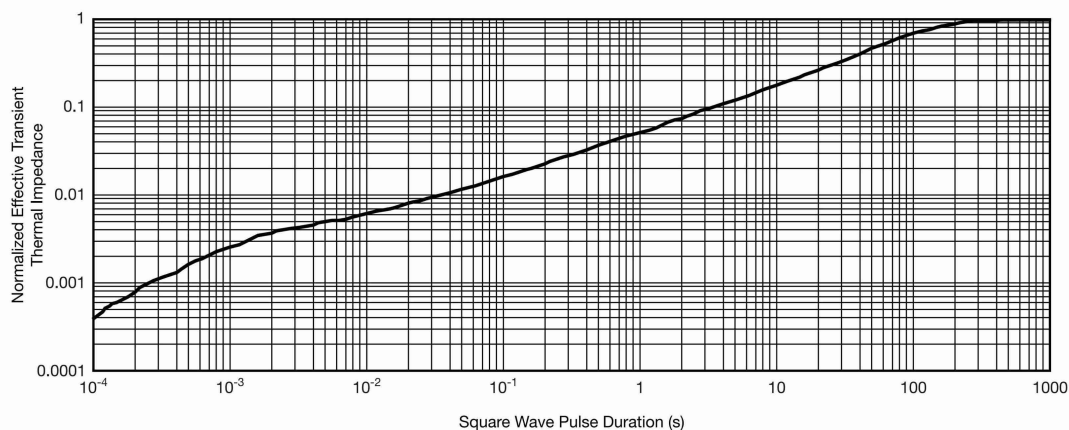
**Notes**

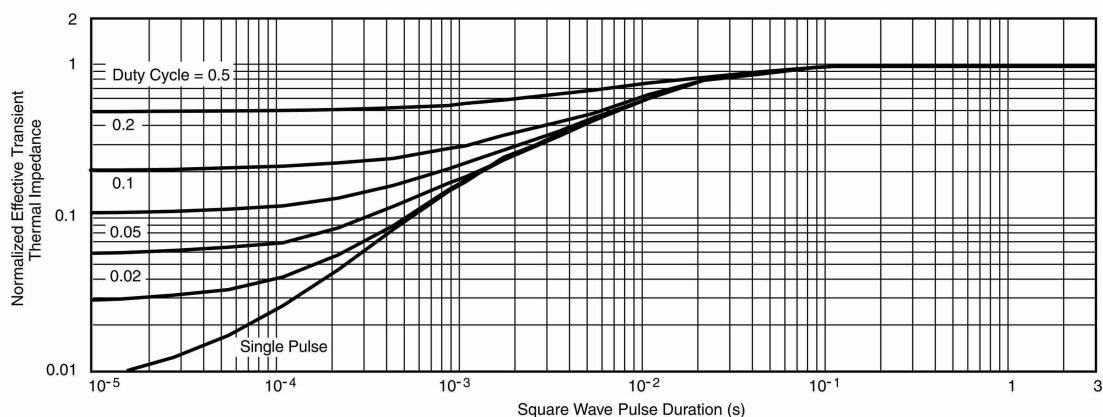
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
 b. Guaranteed by design, not subject to production testing.  
 c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)

**Output Characteristics**

**Transfer Characteristics**

**Transconductance**

**On-Resistance vs. Drain Current**

**Capacitance**

**Gate Charge**

**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

**On-Resistance vs. Junction Temperature**

**Source Drain Diode Forward Voltage**

**On-Resistance vs. Gate-to-Source Voltage**

**Threshold Voltage**

**Drain Source Breakdown vs. Junction Temperature**

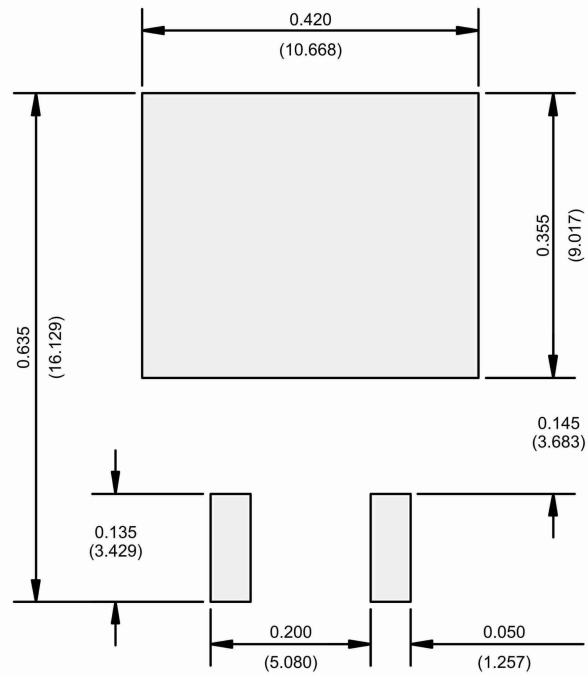
**THERMAL RATINGS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

**Safe Operating Area**

**Normalized Thermal Transient Impedance, Junction-to-Ambient**

**THERMAL RATINGS** ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)


**Normalized Thermal Transient Impedance, Junction-to-Case**

**Note**

- The characteristics shown in the two graphs
    - Normalized Transient Thermal Impedance Junction to Ambient ( $25\text{ }^{\circ}\text{C}$ )
    - Normalized Transient Thermal Impedance Junction to Case ( $25\text{ }^{\circ}\text{C}$ )
- are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

**RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**

Recommended Minimum Pads  
Dimensions in Inches/(mm)

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