● General Description

The AGM605A combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$.

This device is ideal for load switch and battery protection applications.

● Features

- Advance high cell density Trench technology
- Low $R_{DS(ON)}$ to minimize conductive loss
- Low Gate Charge for fast switching
- Low Thermal resistance
- 100% Avalanche tested
- 100% DVDS tested

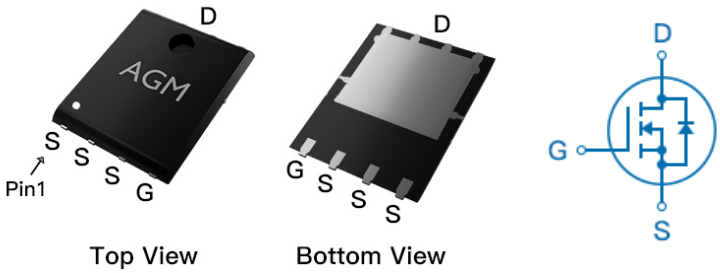
● Application

- MB/VGA Vcore
- SMPS 2nd Synchronous Rectifier
- POL application
- BLDC Motor driver

Product Summary

BVDSS	RDSON	ID
60V	4.4mΩ	80A

PDFN5*6 Pin Configuration



Top View Bottom View

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
AGM605A	AGM605A	PDFN5*6	330mm	12mm	3000

Table 1. Absolute Maximum Ratings (TA=25℃)

Symbol	Parameter	Value	Unit
VDS	Drain-Source Voltage (VGS=0V)	60	V
VGS	Gate-Source Voltage (VDS=0V)	±20	V
ID	Drain Current-Continuous(Tc=25℃) **(Note 1)**	80	A
	Drain Current-Continuous(Tc=100℃)	52	A
IDM (pluse)	Drain Current-Continuous@ Current-Pulsed **(Note 2)**	320	A
PD	Maximum Power Dissipation(Tc=25℃)	147	w
	Maximum Power Dissipation(Tc=100℃)	59	w
EAS	Avalanche energy **(Note 3)**	135	mJ
TJ,TSTG	Operating Junction and Storage Temperature Range	-55 To 150	℃

Table 2. Thermal Characteristic

Symbol	Parameter	Typ	Max	Unit
RθJA	Thermal Resistance Junction-ambient (Steady State)[1]	---	20	℃/W
RθJC	Thermal Resistance Junction-Case[1]	---	0.85	℃/W

Table 3. Electrical Characteristics (TJ=25℃unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On/Off States						
BV_{DSS}	Drain-Source Breakdown Voltage	VGS=0V ID=250μA	60	--	--	V
IDSS	Zero Gate Voltage Drain Current	VDS=60V,VGS=0V	--	--	1	μA
IGSS	Gate-Body Leakage Current	VGS=±20V,VDS=0V	--	--	±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	VDS=VGS,ID=250μA	1.2	--	2.2	V
gFS	Forward Transconductance	VDS=5V,ID=15A	--	10	--	S
RDS(on)	Drain-Source On-State Resistance	VGS=10V, ID=20A	--	4.4	5.6	mΩ
		VGS=4.5V, ID=15A	--	5.8	7.8	mΩ
Dynamic Characteristics						
Ciss	Input Capacitance	VDS=30V,VGS=0V, F=1MHZ	--	1925	--	pF
Coss	Output Capacitance		--	500	--	pF
Crss	Reverse Transfer Capacitance		--	15	--	pF
Rg	Gate resistance	VGS=0V, VDS=-0V,f=1.0MHz	--	2.0	--	Ω
Switching Times						
td(on)	Turn-on Delay Time	VGS=10V,VDS=30V, ID=40A,RGEN=4.7Ω	--	13	--	nS
tr	Turn-on Rise Time		--	4.0	--	nS
td(off)	Turn-Off Delay Time		--	78	--	nS
tf	Turn-Off Fall Time		--	12	--	nS
Qg	Total Gate Charge	VGS=10V, VDS=30V, ID=40A	--	31.5	--	nC
Qgs	Gate-Source Charge		--	4.3	--	nC
Qgd	Gate-Drain Charge		--	2.0	--	nC
Source-Drain Diode Characteristics						
ISD	Source-Drain Current(Body Diode)		--	--	80	A
VSD	Forward on Voltage	VGS=0V,IS=20A	--	--	1.2	V
trr	Reverse Recovery Time	IF=20A , dI/dt=100A/μs , TJ=25℃	--	23	--	ns
Qrr	Reverse Recovery Charge		--	60	--	nc

Notes 1.The maximum current rating is package limited.

Notes 2.Repetitive Rating: Pulse width limited by maximum junction temperature.

Notes 3.EAS condition: TJ=25℃,VDD=30V,Vgs=10V,ID=30A,L=0.3mH,RG=25ohm

N- Channel Typical Characteristics

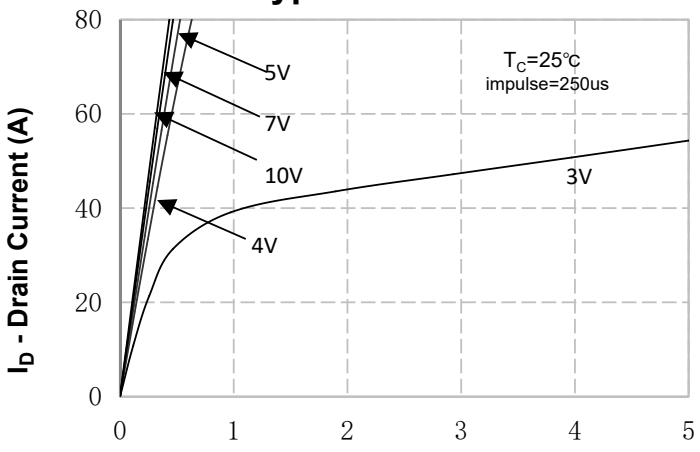


Figure 1. On-Region Characteristics

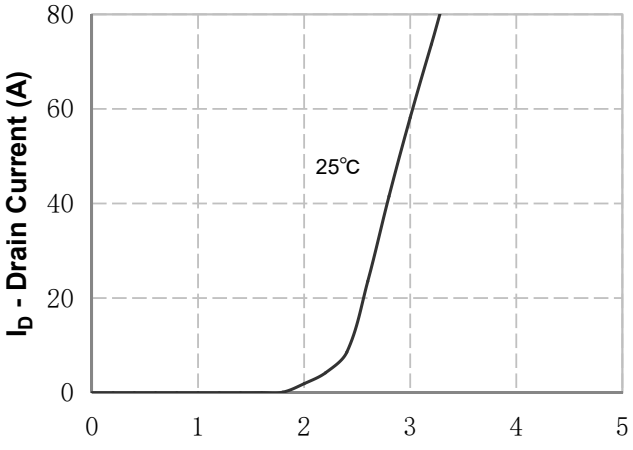


Figure 2. Transfer Characteristics

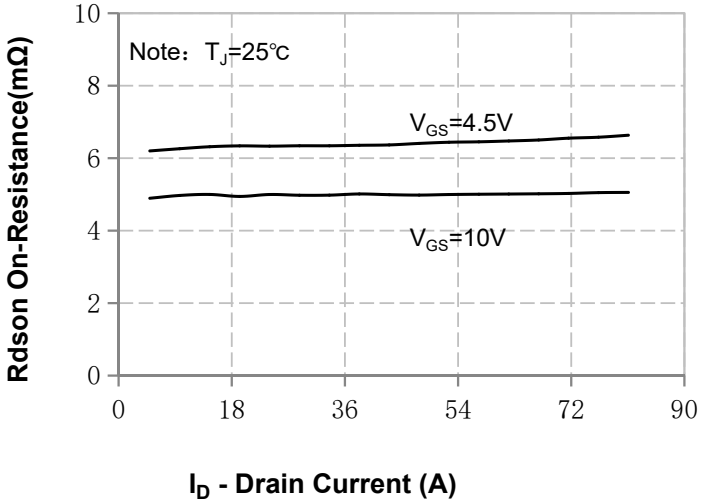


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

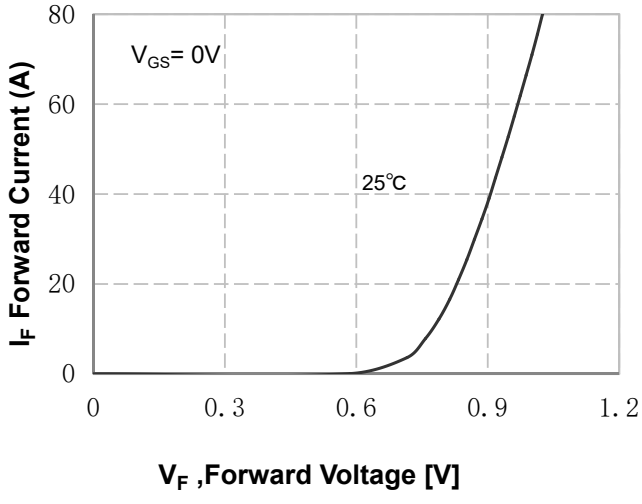


Figure 4. Body Diode Forward Voltage Variation vs Source Current

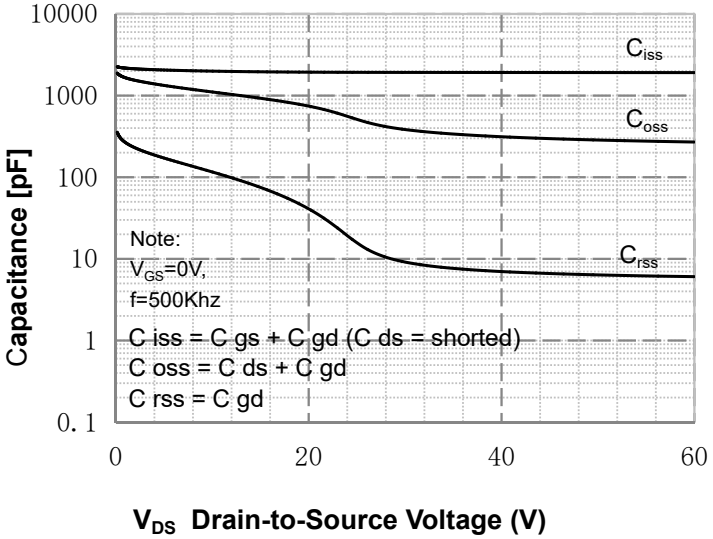


Figure 5. Capacitance Characteristics

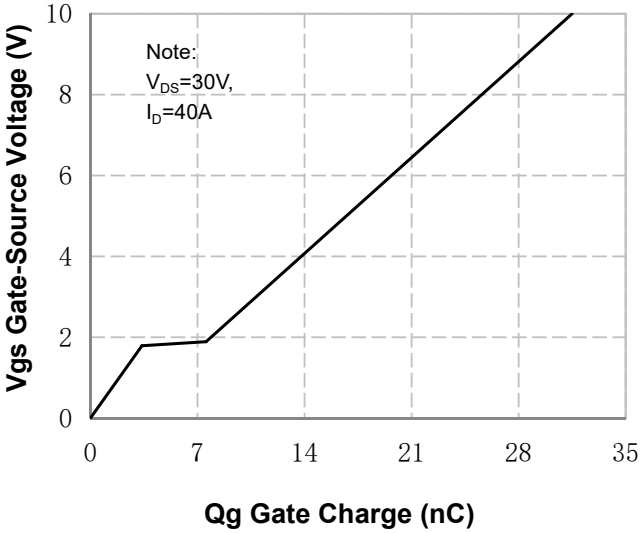


Figure 6. Gate Charge Characteristics

N- Channel Typical Characteristics (Continued)

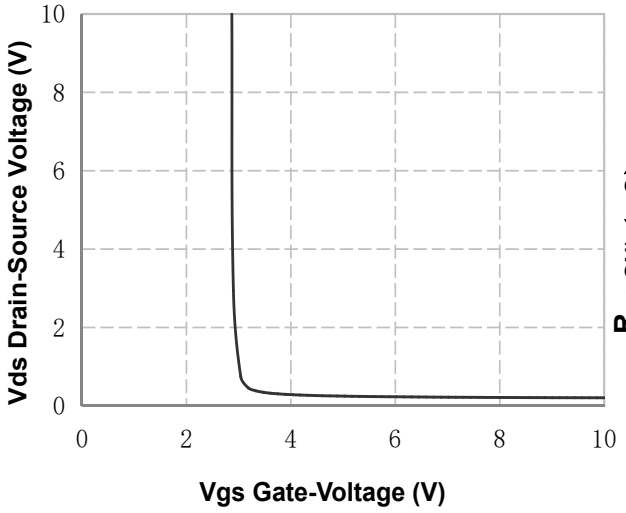


Figure 7. Vds Drain-Source Voltage vs Gate Voltage

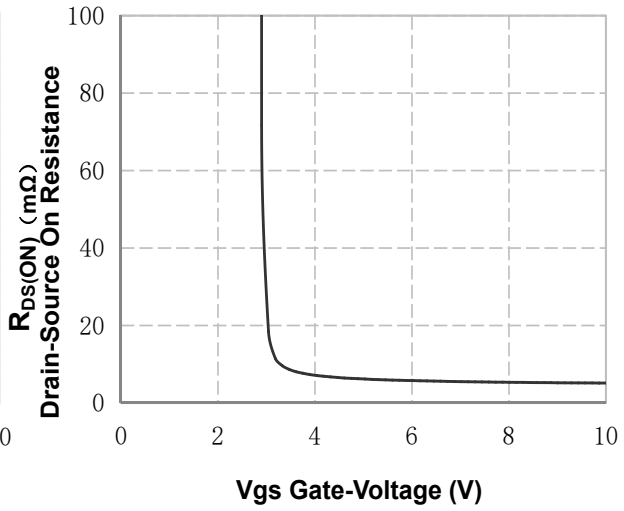


Figure 8. On-Resistance vs Gate Voltage

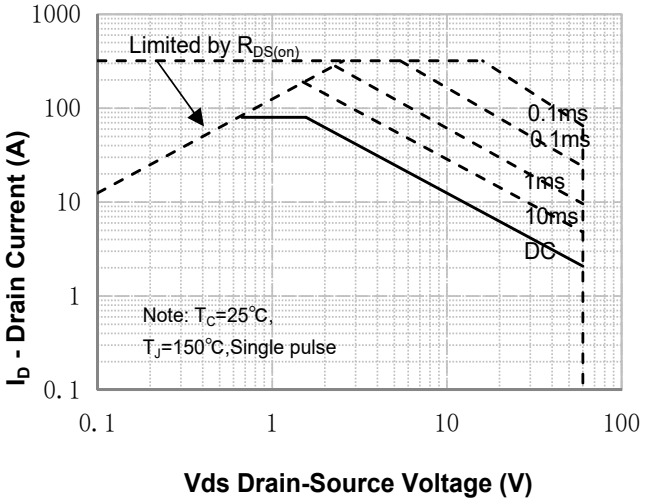


Figure 9. Maximum Safe Operating Area

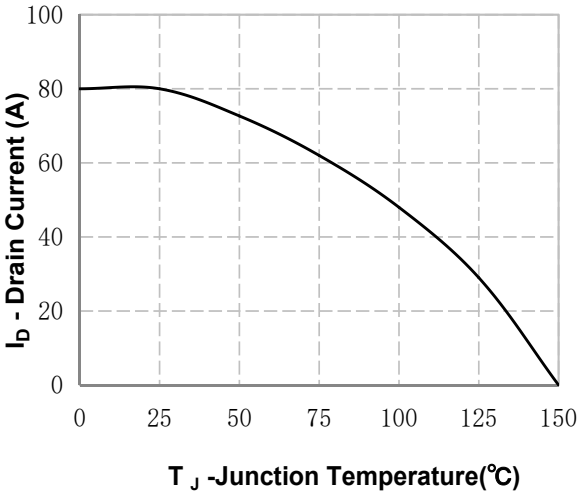


Figure 10. Maximum Continuous Drain Current vs Temperature

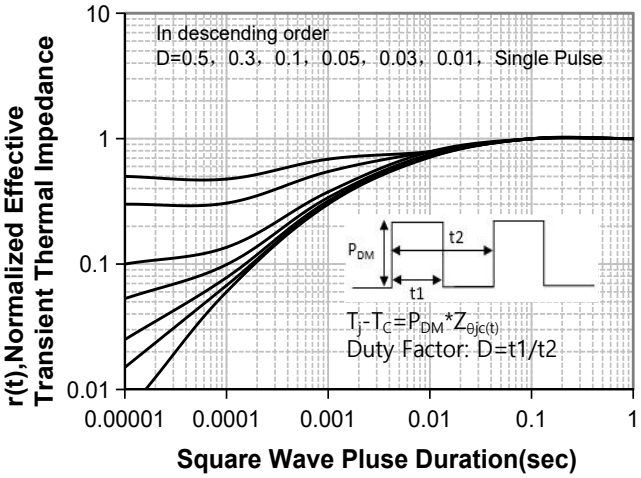
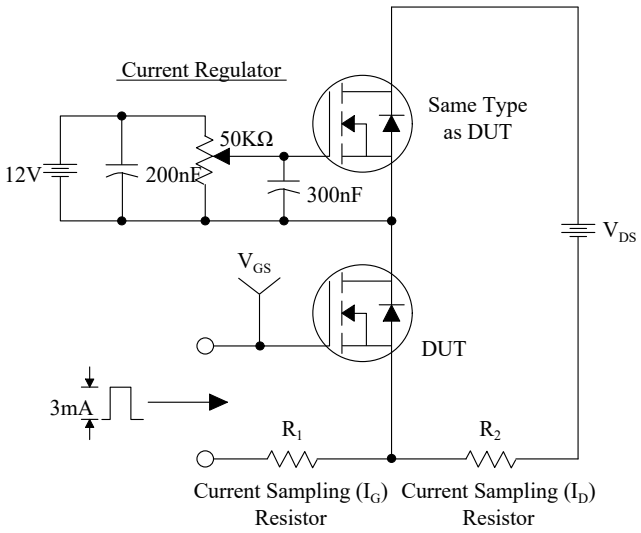
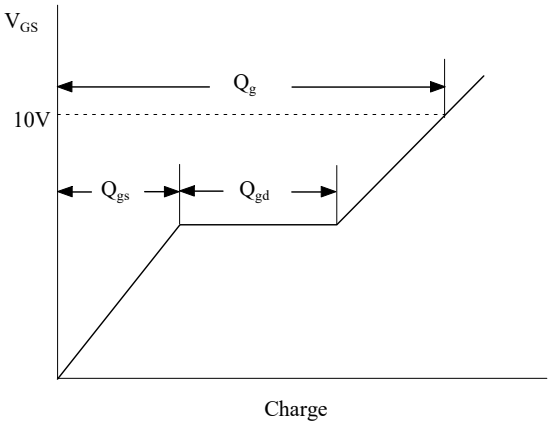


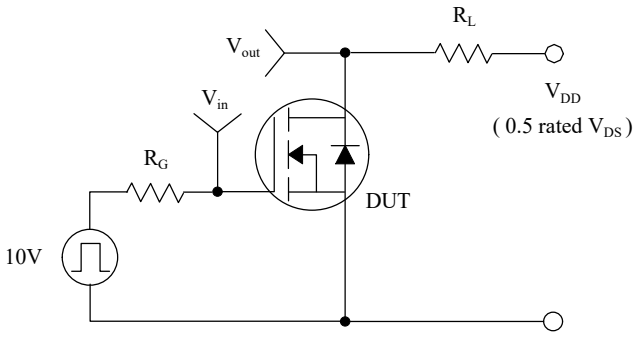
Figure 11. Transient Thermal Response Curve

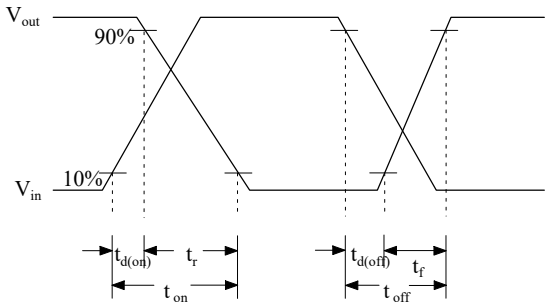
Gate Charge Test Circuit & Waveform



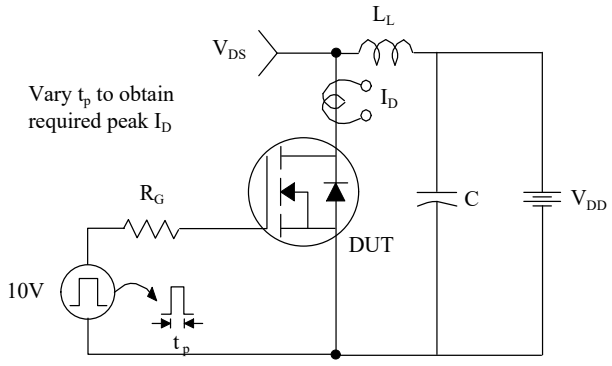


Resistive Switching Test Circuit & Waveforms

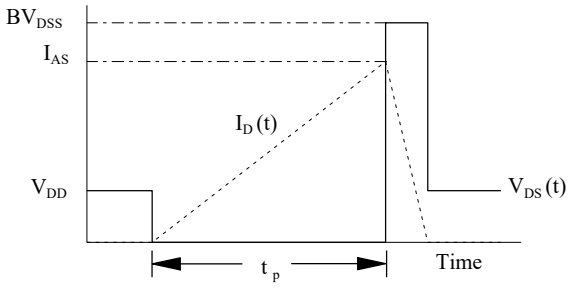




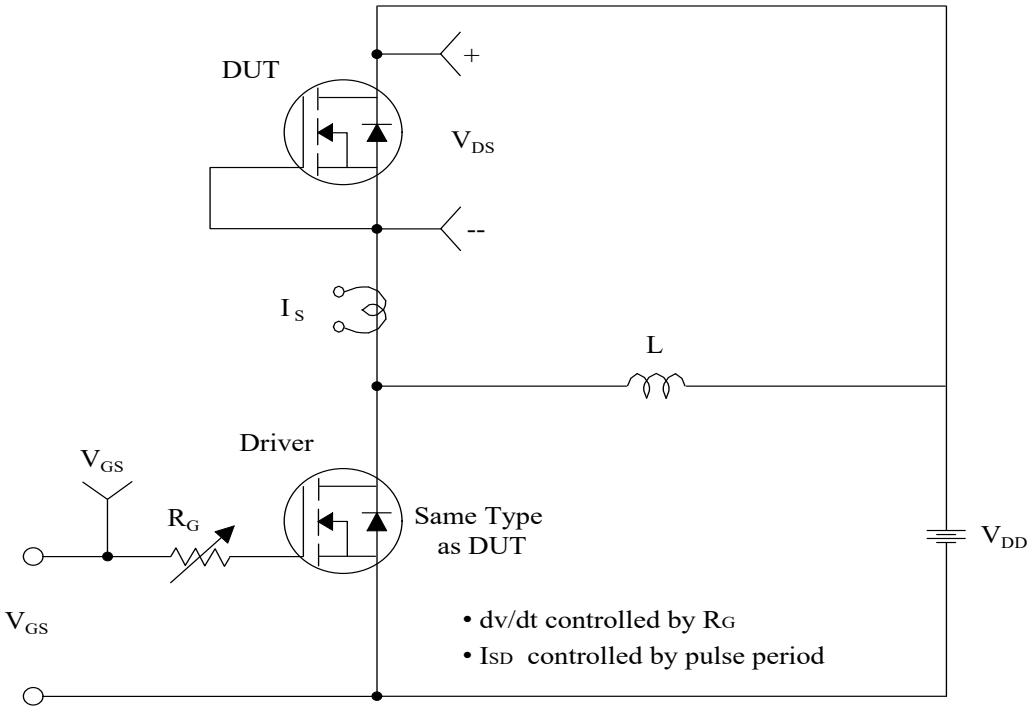
Unclamped Inductive Switching Test Circuit & Waveforms

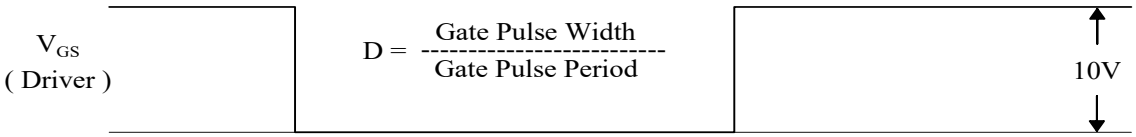


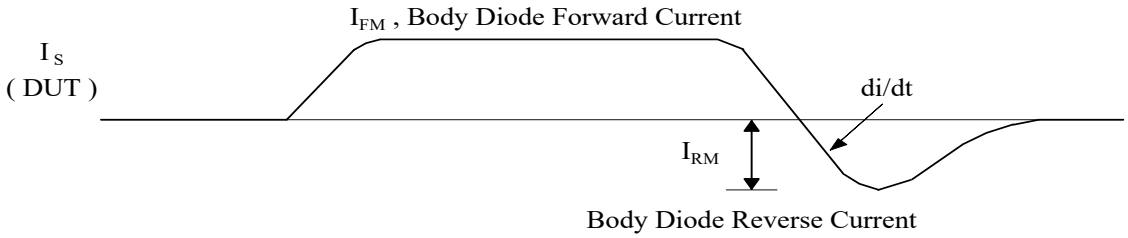
$$E_{AS} = \frac{1}{2} L_L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

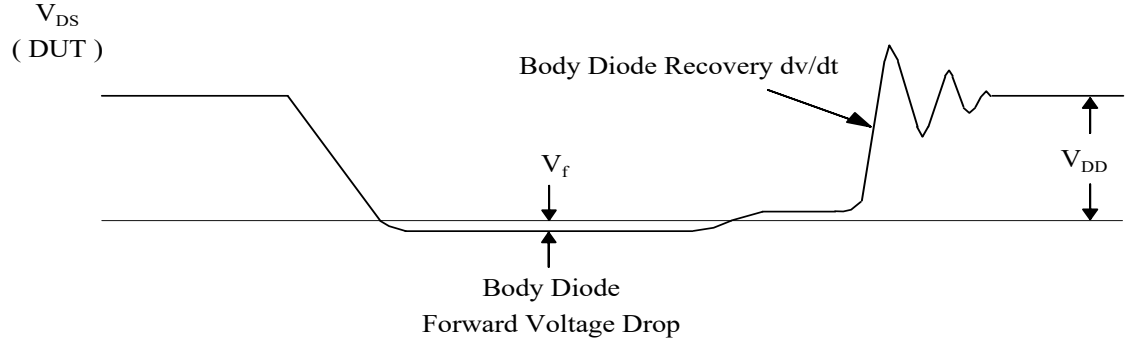


Peak Diode Recovery dv/dt Test Circuit & Waveforms

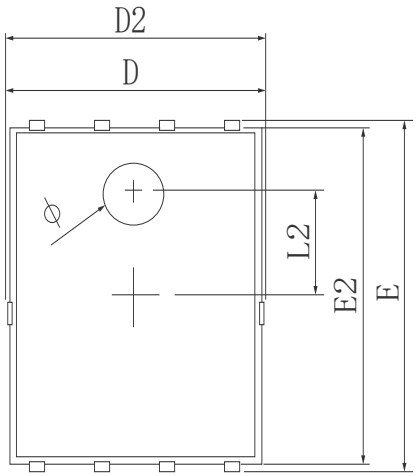


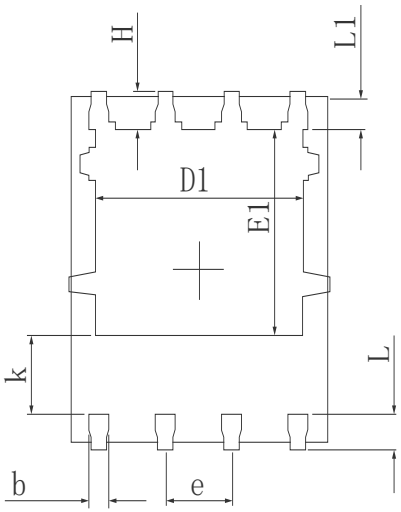


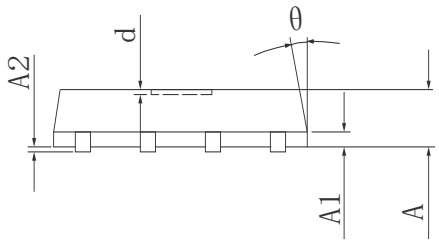




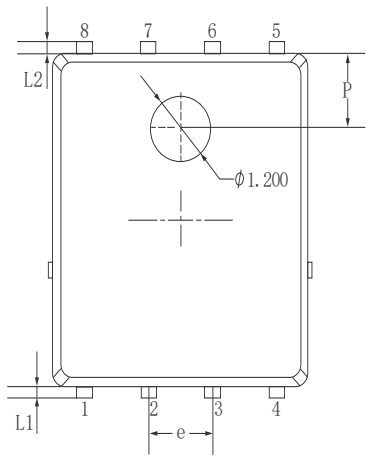
●Dimensions（PDFN5*6）

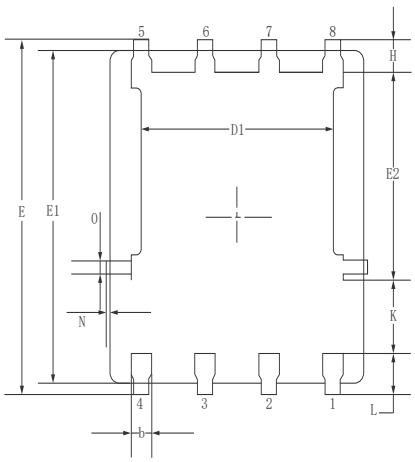


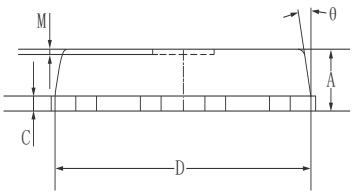




SYMBOL	MILLIMETER		
	MIN	Typ.	MAX
A	0.900	1.000	1.100
A1	0.254 REF.		
A2	0~0.05		
D	4.824	4.900	4.976
D1	3.910	4.010	4.110
D2	4.924	5.000	5.076
E	5.924	6.000	6.076
E1	3.375	3.475	3.575
E2	5.674	5.750	5.826
b	0.350	0.400	0.450
e	1.270 TYP.		
L	0.534	0.610	0.686
L1	0.424	0.500	0.576
L2	1.800 REF.		
k	1.190	1.290	1.390
H	0.549	0.625	0.701
θ	8°	10°	12°
Φ	1.100	1.200	1.300
d			0.100





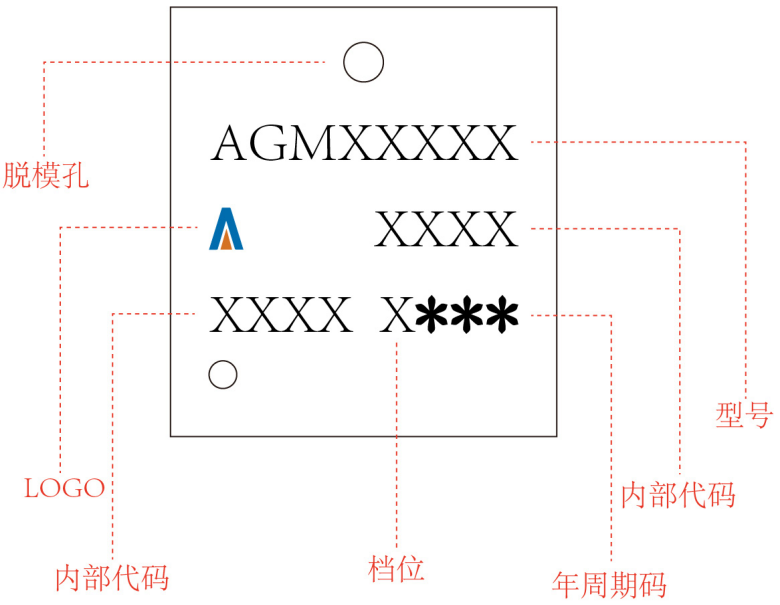


Symbol	Millimeters		
	MIN.	NOM.	MAX.
A	0.90	1.05	1.20
b	0.35	0.40	0.50
C	0.20	0.25	0.35
D	4.90	5.05	5.20
D1	3.72	3.82	3.92
E	6.00	6.15	6.30
E1	5.60	5.75	5.90
E2	3.47	3.57	3.67
e	1.27 BSC.		
H	0.48	0.58	0.68
K	1.17	1.27	1.37
L	0.64	0.74	0.84
L1/L2	0.20 REF.		
θ	8°	10°	12°
M	0.08 REF.		
N	0	-	0.15
O	0.25 REF.		
P	1.28 REF.		

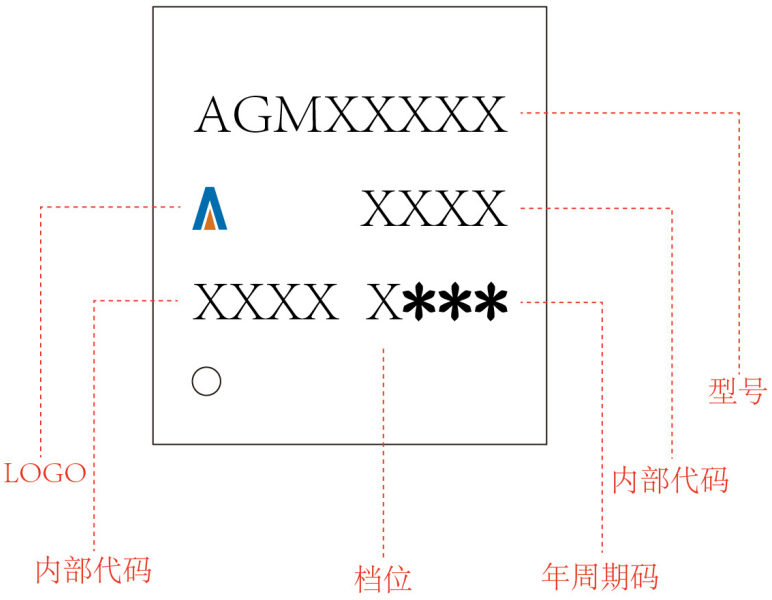
PDFN5*6

Marking Instructions:

Model1:



Model2:



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This document is the fifth version issued on October 10th, 2024. This document replaces all previously provided information.