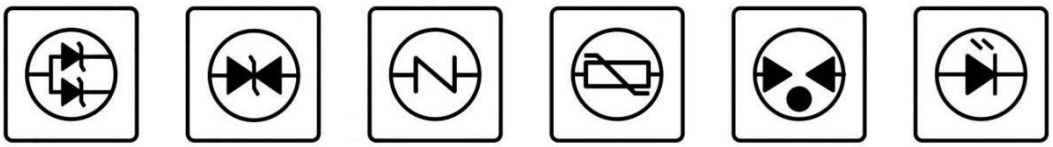
MSKSEMI 美森科
SEMICONDUCTOR



TPD4E05U06DQAR-MS

Product specification

TPD4E05U06DQAR-MS

Features

- Solid-state silicon-avalanche technology
- Lowoperating and clamping voltage
- Up to four I/OLines of Protection
- Ultra low capacitance: 0.5pFtypical(I/O to I/O)
- Low Leakage
- Low operating voltage:3.3V
- Flow-Through design

Mechanical Characteristics

- USON-10 package (2.5×1.0×0.58mm)
- Molding compound flammability rating: UL 94V-0
- Packaging: Tape and Reel
- RoHS/WEEE Compliant

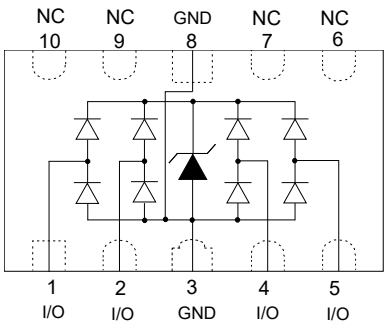
IEC COMPATIBILITY (EN61000-4)

- **IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact)**
- **IEC 61000-4-4 (EFT) 40A (5/50ns)**
- **IEC 61000-4-5(Lightning) 5A(8/20μs)**

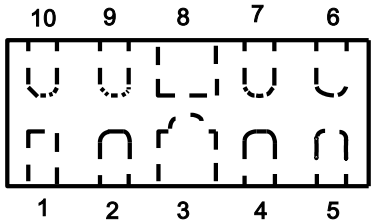
Applications

- Digital Visual Interface(DVI)
- MDDI Ports
- DisplayPortTM Interface
- PCI Express
- High Definition Multi-Media Interface(HDMI)
- eSATA Interfaces

Reference News

PACKAGE OUTLINE	Circuit Diagram	Marking
		
USON-10		

Schematic & PIN Configuration



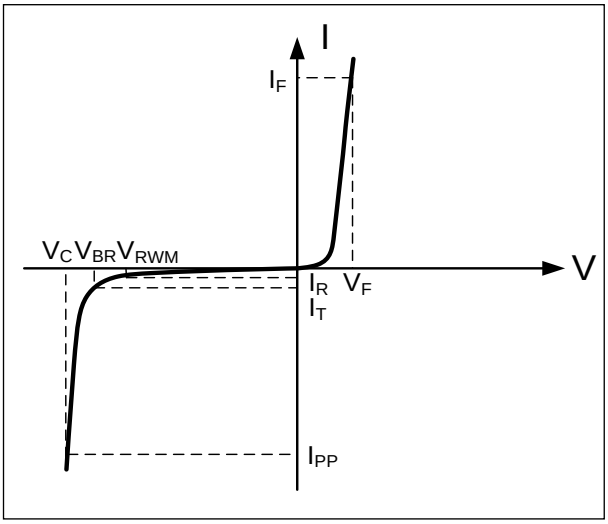
Pin	Identificaion
1,2,4,5	Input Lines
6,7,9, 10	Output Lines (No Internal Connection)
3,8	Ground

Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power (t_p =8/20μs)	P_{PP}	80	Watts
Peak Pulse Current (t_p =8/20μs)	I_{pp}	5	A
ESD per IEC 61000-4-2(Air) ESD per IEC 61000-4-2(contact)	V_{ESD}	+/-25 +/-25	kV
Operating Temperature	T_J	-55 to + 125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Parameters (T=25°C)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_F	Forward Current
V_F	Forward Voltage @ I_F

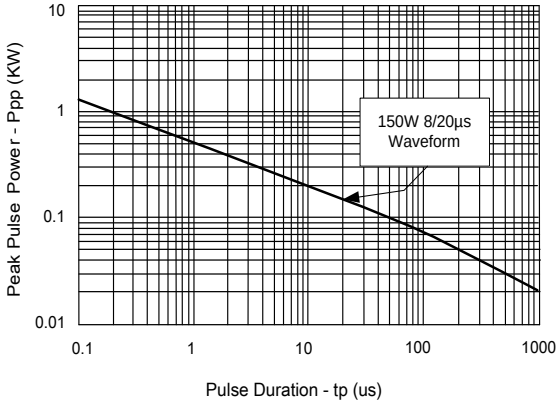


Electrical Characteristics

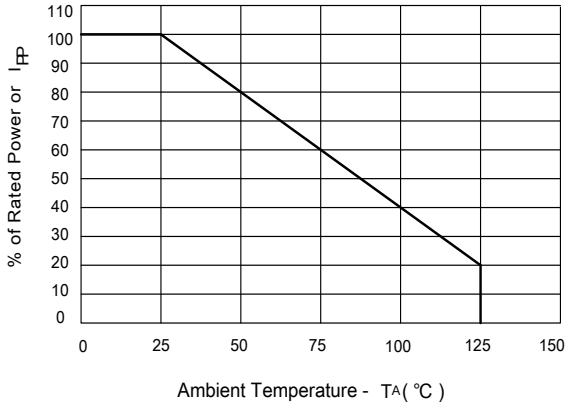
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}	Any I/O pin to ground			3.3	V
Reverse Breakdown Voltage	V_{BR}	I_t = 1mA Any I/O pin to ground	6.0			V
Reverse Leakage Current	I_R	V_{RWM} = 3V, T=25°C Any I/O pin to ground			1	μA
Clamping Voltage	Vc	I_{pp}=5A, t_p=8/20 μ s Any I/O pin to ground			15	V
Junction Capacitance	C_j	V_R = 0V, f = 1MHz I/O pin to GND			0.8	pF
		V_R = 0V, f = 1MHz Between I/O pins		0.3		pF

Typical Characteristics

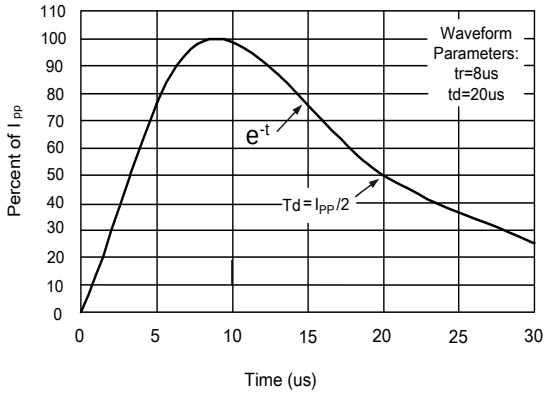
Non-Repetitive Peak Pulse Power vs. Pulse Time



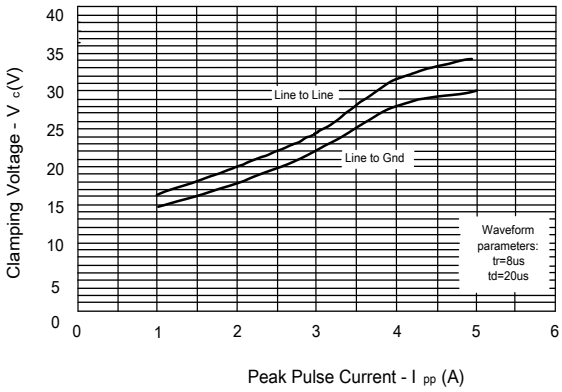
Power Derating curve



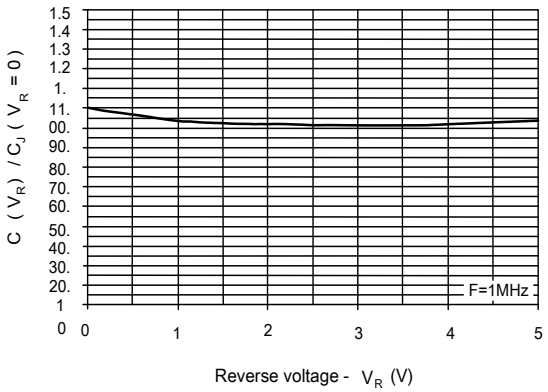
Pulse Waveform



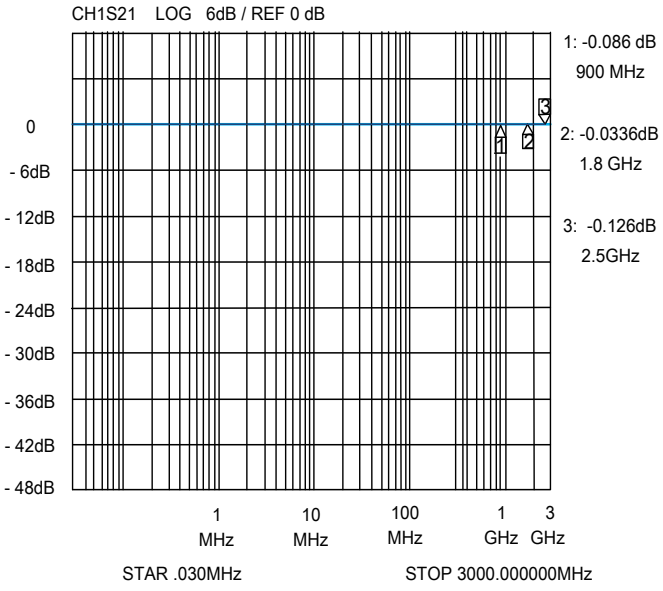
Clamping Voltage vs.Peak Pulse Current



Normalized Capacitance vs. Reverse Voltage



Insertion Loss S21 - I/O to GND



Design Recommendations for HDMI protection

Adding external ESD protection to HDMI ports can be challenging. First, ESD protection devices have an inherent junction capacitance. Furthermore, adding even a small amount of capacitance will cause the impedance of the differential pair to drop. Second, large packages and land pattern requirements cause discontinuities that adversely affect signal integrity. The TPD4E05U06DQAR-MS are specifically designed for protection of high-speed interfaces such as HDMI.

They present <0.4pF capacitance between the pairs while being rated to handle ±25kV ESDcontact discharges (±25kV air discharge) as outlined in IEC 61000-4-2. Each device is in a leadless SLP package that is less than 1.1mm wide. They are designed such that the traces flow straight through the device. The narrow package and flow-through design reduces discontinuities and minimizes impact on signal integrity. This becomes even more critical as signal speeds increase.

Pin Configuration

Figure 1 is an example of how to route the high speed differential traces through the ESD3V3U4ULC . The solid line represents the PCB trace. The PCB traces are used to connect the pin pairs for each line (pin 1 to pin 10, pin 2 to pin 9, pin 4 to pin 7, pin 5 to pin 6). For example, line 1 enters at pin 1 and exits at Pin 10 and the PCB trace connects pin 1 and 10 together. This is true for lines connected at pins 2, 4, and 5 also. Ground is connected at pins 3 and 8. One large ground pad should be used in lieu of two separate pads. The same layout rules apply for the ESD3V3U4ULC .

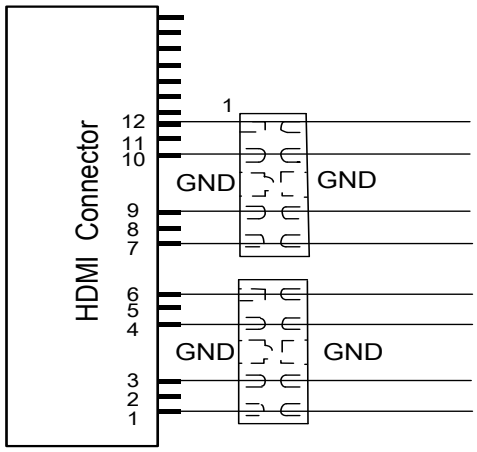


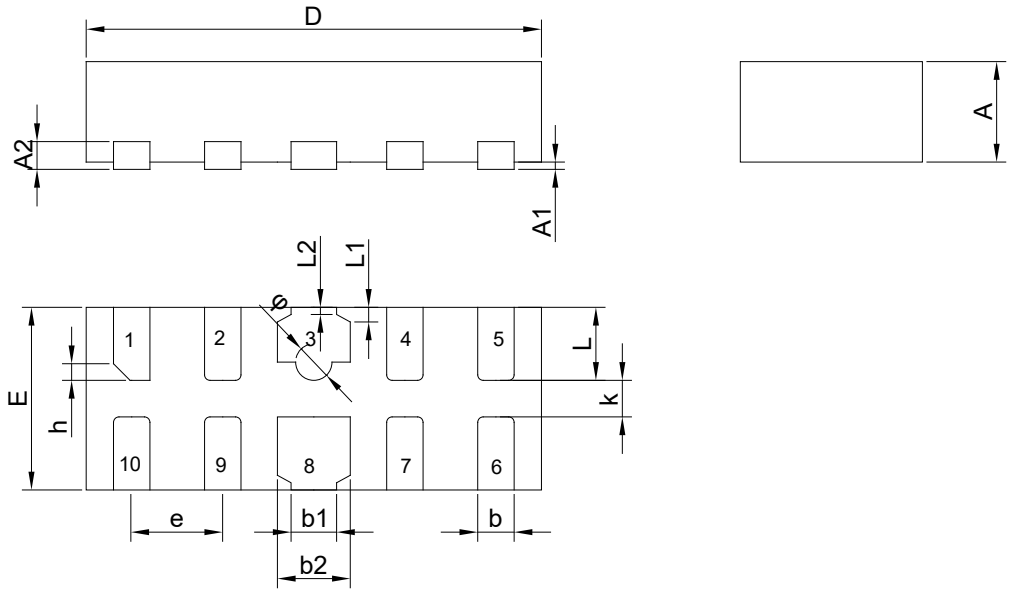
Figure 1.Flow though layout Using

Design Recommendations for HDMI Protection

Good circuit board layout is critical not only for signal integrity, but also for effective suppression of ESD induced transients. For optimum ESD protection, the following guidelines are recommended:

- Place the device as close to the connector as possible.This practice restricts ESD coupling into adjacent traces and reduces parasitic inductance.
- The ESD transient return path to ground should be kept as short as possible.
  Whenever possible, use multiple micro vias connected directly from the device ground pad to the ground plane.
- Avoid running critical signals near board edges.

Dimension (DFN2510)



Dimensions in Millimeter							
Symbol	Min.	Nom.	Max.	Symbol	Min.	Nom.	Max.
A	0.500	0.550	0.600	D	2.450	2.500	2.550
A1	0.00	/	0.05	E	0.950	1.00	1.050
A2	0.122	0.152	0.200	e	0.450	0.500	0.550
b	0.150	0.200	0.250	h	0.080	0.120	0.150
b1	0.200	0.250	0.300	k	0.150	0.200	0.250
b2	0.350	0.400	0.450	L	0.350	0.400	0.450
L1		0.075 REF		L2		0.05 REF	
φ	0.150	0.200	0.250				

REEL SPECIFICATION

P/N	PKG	QTY
TPD4E05U06DQAR-MS	DFN2510	3000

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