1-MSPS/800-KSPS, 3.3V-5.25V, ULTRA LOW POWER, 12-/10-/8-BIT SAR ANALOG-TO-DIGITAL CONVERTER

FEATURES

- Single 3.3V to 4.8V Supply Operation for CI7476E/77E/78E
  Single 4V to 5.25V Supply Operation for CI7476/77/78
- Fast Throughput Rate:
  1 MSPS for CI7476E/77E/78E
  800 KSPS for CI7476/77/78
- ±1.25LSB INL, ±1LSB DNL (CI7476)
- No Pipeline Delays
- SPI/DSP/MICROWIRE™/QSPI™ Compatible Serial Interface
- Variable Power Management
- Low Power (CI7476 typical):
  3.6mW (4V, 800KSPS)
  6.15mW (5V, 800KSPS)
- Second-Source for AD7476/77/78
- 6-Pin SOT-23 Package

APPLICATIONS

- Battery Powered Systems
  Personal digital assistants
  Medical instruments
  Mobile communications
- Instrumentation and Control Systems
- Data Acquisition Systems
- High Speed Modems
- Optical Sensors

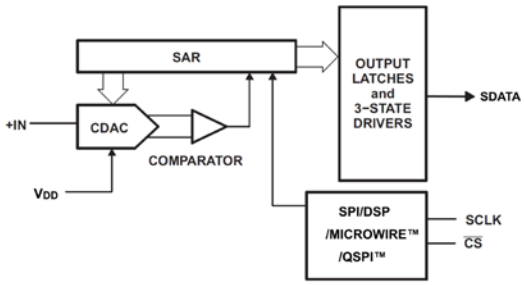


Figure 1. Functional Block Diagram

DESCRIPTION

The CI7476, CI7477, and CI7478 are, respectively, 12-bit, 10-bit, and 8-bit, high speed, low power, small size, successive approximation ADCs. These devices can operate from a single 3.3 V to 4.8 V supply with a 1-MSPS throughput (CI7476E/CI7477E/CI7478E), or operate from a single 4 V to 5.25 V supply with an 800-KSPS throughput (CI7476/CI7477/CI7478) . The CI7476/ CI7477/ CI7478 is available in a 6-pin SOT-23 package and has an operating temperature range of -40°C to 85°C.

The C7476/C7477/ C7478 is a drop-in replacement for the AD7476/AD7477/AD7478 and consumes only half dynamic power of their counterpart.

SPECIFICATIONS

At-40℃ to 85℃, f_{SAMPLE} = 1 MSPS and f_{SCLK} = 20 MHz if 3.3 V ≤ V_{DD} ≤ 4.8 V ; f_{SAMPLE} = 800 KSPS and f_{SCLK} = 16 MHz if 4 V ≤ V_{DD} ≤ 5.25 V . (unless otherwise noted)

PARAMETER	TEST CONDITIONS	CI7476/76E			CI7477/77E			CI7478/78E			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SYSTEM PERFORMANCE											
Resolution			12			10			8		Bits
No missing codes		12			10			8			Bits
Integral linearity		-1.25		1.25	-1		1	-0.5		0.5	LSB
Differential linearity		-1		1	-1		1	-0.5		0.5	LSB
f_{SAMPLE} Throughput rate	f_{SCLK} = 16 MHz, 4 V ≤ V_{DD} ≤ 5.25 V			800			800			800	KSPS
	f_{SCLK} = 20 MHz, 3.3 V ≤ V_{DD} ≤ 4.8 V			1			1			1	MSPS
SNR	f_{IN} = 100 kHz		72			61.5			49.5		dB
THD	f_{IN} = 100 kHz		-82			-73.5			-66		dB

CI7476

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
I_{DD} Supply current, normal operation	Digital inputs = 0 V or V_{DD}	f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 4 V		0.90	1.00	mA
		f_{SAMPLE} =800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 5 V		1.23	1.50	
		f_{SAMPLE} = 500 KSPS, f_{SCLK} = 10 MHz, V_{DD} = 4 V		0.46	0.52	
		f_{SAMPLE} = 500 KSPS, f_{SCLK} = 10 MHz, V_{DD} = 5 V		0.75	0.80	
POWER DISSIPATION, CI7476						
Normal operation		f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 4 V		3.60	4.0	mW
		f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 5 V		6.15	7.5	mW

CI7477

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
I_{DD} Supply current, normal operation	Digital inputs = 0 V or V_{DD}	f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 4 V		0.87	1.05	mA
		f_{SAMPLE} =800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 5 V		1.05	1.25	
		f_{SAMPLE} = 500 KSPS, f_{SCLK} = 10 MHz, V_{DD} = 4 V		0.48	0.58	
		f_{SAMPLE} = 500 KSPS, f_{SCLK} = 10 MHz, V_{DD} = 5 V		0.80	0.98	
POWER DISSIPATION, CI7477						
Normal operation		f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 4 V		3.45	4.25	mW
		f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 5 V		5.25	6.25	mW

CI7478

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
I_{DD} Supply current, normal operation	Digital inputs = 0 V or V_{DD}	f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 4 V		**0.76**	**1.02**	mA
		f_{SAMPLE} =800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 5 V		**1.00**	**1.24**	
		f_{SAMPLE} = 500 KSPS, f_{SCLK} = 10 MHz, V_{DD} = 4 V		**0.45**	**0.55**	
		f_{SAMPLE} = 500 KSPS, f_{SCLK} = 10 MHz, V_{DD} = 5 V		**0.60**	**0.75**	
POWER DISSIPATION, CI7478						
Normal operation		f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 4 V		**3.05**	**4.10**	mW
		f_{SAMPLE} = 800 KSPS, f_{SCLK} = 16 MHz, V_{DD} = 5 V		**4.95**	**6.20**	mW

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

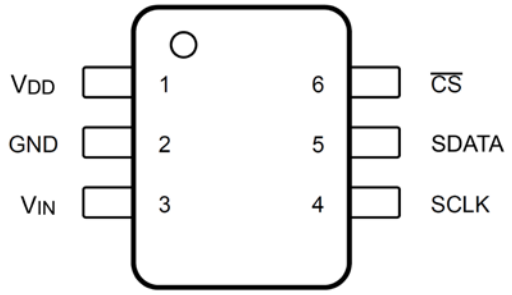


Figure 2. Pin Configuration

TERMINAL		DESCRIPTION
NAME	NO.	
V_{DD}	1	Power Supply Input.
GND	2	The ground return for the supply and signals.
V_{IN}	3	Analog Input. This signal can range from 0 V to V_{DD}.
SCLK	4	Digital clock input. This clock directly controls the conversion and readout processes.
SDATA	5	Digital data output. The output samples are clocked out of this pin on falling edges of the SCLK pin.
$\overline{CS}$	6	Chip Select. On the falling edge of $\overline{CS}$, a conversion process begins.

TYPICAL CONNECTION

Figure 3 shows a typical connection diagram for the CI7476/77/78. The 5 V supply should come from a stable power supply such as an LDO. The supply to CI7476/77/78 should be decoupled to the ground. A 1-µF and a 10-nF decoupling capacitor are required between the V_{DD} and GND pins of the converter. This capacitor should be placed as close as possible to the pins of the device. Always set the V_{DD} supply to be greater than or equal to the maximum input signal to avoid saturation of codes.

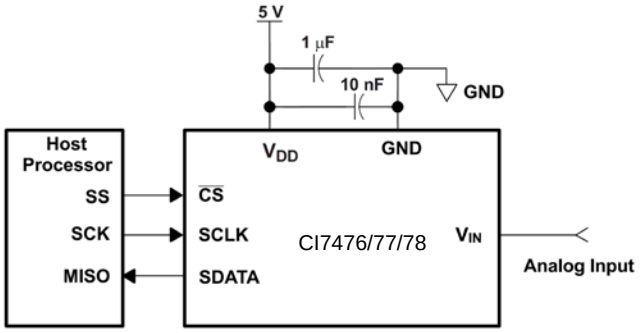


Figure 3. Typical Circuit Configuration

TIMING DIAGRAM

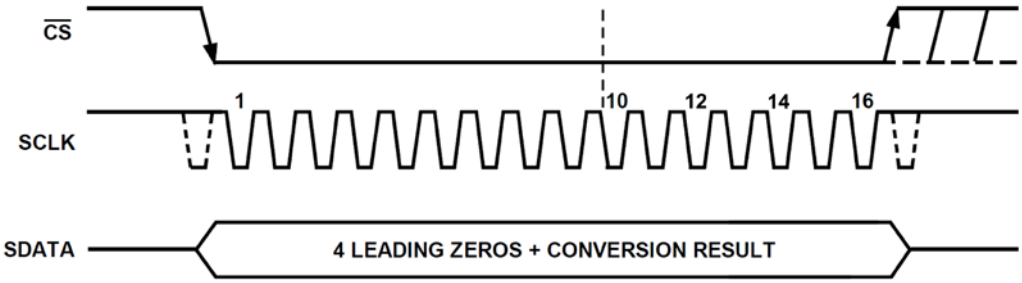


Figure 4. Timing Diagram

The conversion is initiated on the falling edge of $\overline{CS}$. The device outputs data while the conversion is in progress, and it requires 16/14/12 serial clock cycles to complete the conversion and access the full results. The CI7476/CI7477 CI7478 data word contains 4 leading zeros, followed by 12 -bit/10-bit/8-bit data in MSB first format.

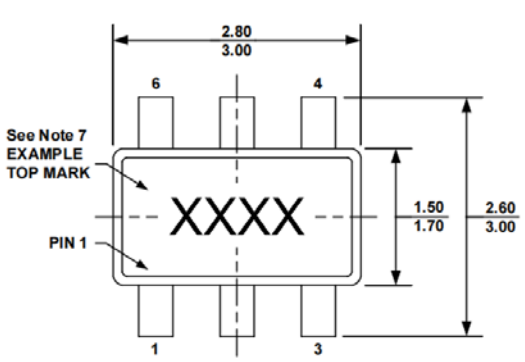
Once a data transfer is complete, SDATA will return to the tri-state mode, and another conversion can be initiated after the quiet time has elapsed by again bringing $\overline{CS}$ low.

POWER-DOWN MODE

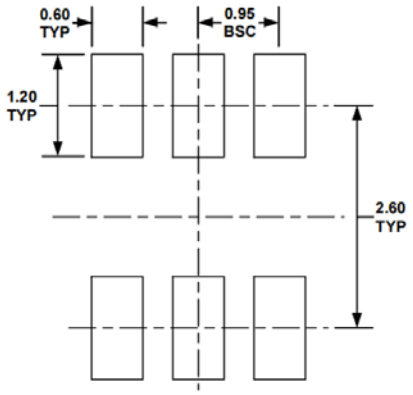
The CI7476/77/78 family has an auto power-down feature. Besides powering down all circuitry, the converter consumes only a small amount of current in this mode. The device automatically wakes up when $\overline{CS}$ falls. However, not all of the functional blocks are fully powered until sometime before the third falling edge of SCLK. The device powers down once it reaches the end of conversion which is the 16th falling edge of SCLK for the CI7476 (the 14th and 12th for the CI7477 and CI7478, respectively). The device enters power down mode if $\overline{CS}$ goes high before the 10th SCLK falling edge. Ongoing conversion stops and SDATA goes to three-state under this power down condition.

These converters achieve lower power dissipation for a fixed throughput rate by using higher SCLK frequencies. Higher SCLK frequencies reduce the acquisition time and conversion time. This means the converters spend more time in auto power-down mode per conversion cycle. For a particular SCLK frequency, the acquisition time and conversion time are fixed. Therefore, a lower throughput increases the proportion of the time the converters are in power down, thereby reducing power consumption.

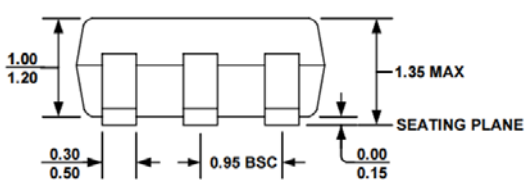
OUTLINE DIMENTIONS



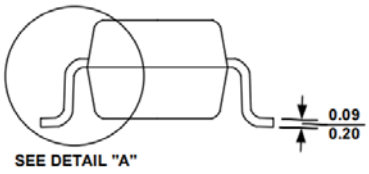
TOP VIEW



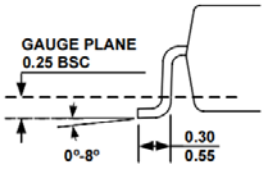
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-178, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

NOTES

1. Unpacked ICs, tube-mounted ICs, etc. must be stored in a drying cabinet, and the humidity in the drying cabinet < 20% R.H.
2. After access, the components are stored in an electrostatic packaging protective bag.
3. Anti-static damage: the device is an electrostatic sensitive device, and sufficient anti-static measures should be taken during transmission, assembly and testing.
4. The user should conduct a visual inspection before use, and the bottom, side and surrounding of the circuit can be welded only if it is bright. If oxidation occurs, the circuit can be processed by means of oxidation, and the circuit must be soldered within 12 hours after processing.