250KSPS, 3.3V-5.25V, ULTRA LOW POWER, 10-/12-BIT SAR ANALOG-TO-DIGITAL CONVERTER

FEATURES

- Specified for V_{DD} of 3.3V to 5.25V
- Fast Throughput Rate:250 KSPS
- ±0.5LSB INL,±0.5LSB DNL (CI7920)
- Wide input bandwidth
  71.5 dB SNR at 100 kHz input frequency
- No Pipeline Delays
- SPI/DSP/MICROWIRE™/QSPI™ Compatible Serial Interface
- Variable Power Management
- Low Power (CI7920 typical):
  1.1mW (3.3V, 250 KSPS)
  2.8mW (5V, 250 KSPS)
- Second-Source for AD7910/20
- 6-Pin SOT-23 Package (Stock)
  6-Pin SC-70 and 8-Pin MSOP Packages (Planned)

APPLICATIONS

- Battery Powered Systems
  Personal digital assistants
  Medical instruments
  Mobile communications
- Instrumentation and Control Systems
- Data Acquisition Systems
- High Speed Modems
- Optical Sensors

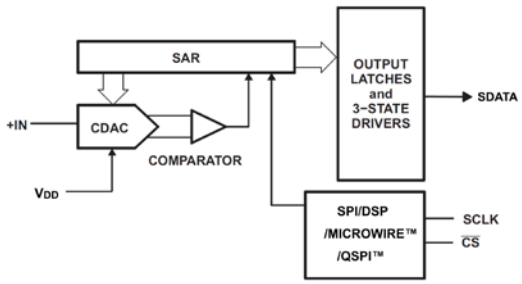


Figure 1. Functional Block Diagram

DESCRIPTION

The CI7910 and CI7920 are, respectively, 10-bit and 12-bit, high speed, low power, small size, successive approximation ADCs. The parts operate from a single 3.3 V to 5.25 V power supply and feature throughput rates up to 250 KSPS.

The CI7910/ CI7920 is available in a 6-pin SOT-23 package and has an operating temperature range of -40°C to 85°C.

The CI7910/CI7920 is a drop-in replacement tor the AD7910/AD7920 and consumes only one third dynamic power of their counterpart

SPECIFICATIONS

At-40℃ to 85℃, f_{SAMPLE} = 250 KSPS and f_{SCLK} = 5 MHz, if 3.3 V ≤ V_{DD} ≤ 5.25 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	CI7910			CI7920			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
SYSTEM PERFORMANCE								
Resolution			**10**			**12**		Bits
No missing codes			**10**			**12**		Bits
Integral linearity			**0.5**			**0.5**		LSB
Differential linearity			**0.5**			**0.5**		LSB
f_{SAMPLE} Throughput rate	f_{SCLK} = 5 MHz, 3.3 V ≤ V_{DD} ≤ 5.25 V		**250**			**250**		KSPS
SNR	f_{IN} = 100 kHz, 3.3 V ≤ V_{DD} ≤ 5.25 V		**61.5**			**72**		dB
THD	f_{IN} = 100 kHz, 3.3 V ≤ V_{DD} ≤ 5.25 V		**-73.5**			**-82**		dB

CI7910

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
I_{DD} Supply current, normal operation	Digital inputs = 0 V or V_{DD}	f_{SAMPLE} = 250 KSPS, f_{SCLK} = 5 MHz, V_{DD} = 3.3 V		**0.33**	**0.34**	mA
		f_{SAMPLE} = 250 KSPS, f_{SCLK} = 5 MHz, V_{DD} = 4.5 V		**0.44**		
		f_{SAMPLE} = 250 KSPS, f_{SCLK} = 5 MHz, V_{DD} = 5 V		**0.50**	**0.54**	
POWER DISSIPATION, CI7910						
Normal operation		f_{SAMPLE} = 250 KSPS, f_{SCLK} = 5 MHz, V_{DD} = 3.3 V		**1.09**	**1.12**	mW
		f_{SAMPLE} = 250 KSPS, f_{SCLK} = 5 MHz, V_{DD} = 5 V		**2.50**	**2.70**	mW

CI7920

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
I_{DD} Supply current, normal operation	Digital inputs = 0 V or V_{DD}	f_{SAMPLE} = 250 KSPS, f_{SCLK} = 5 MHz, V_{DD} = 3.3 V		**0.33**	**0.37**	mA
		f_{SAMPLE} = 250 KSPS, f_{SCLK} = 5 MHz, V_{DD} = 4.5 V		**0.50**		
		f_{SAMPLE} = 250 KSPS, f_{SCLK} = 5 MHz, V_{DD} = 5 V		**0.56**	**0.60**	
POWER DISSIPATION, CI7920						
Normal operation		f_{SAMPLE} = 250 KSPS, f_{SCLK} = 5 MHz, V_{DD} = 3.3 V		**1.10**	**1.22**	mW
		f_{SAMPLE} = 250 KSPS, f_{SCLK} = 5 MHz, V_{DD} = 5 V		**2.80**	**3.00**	mW

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

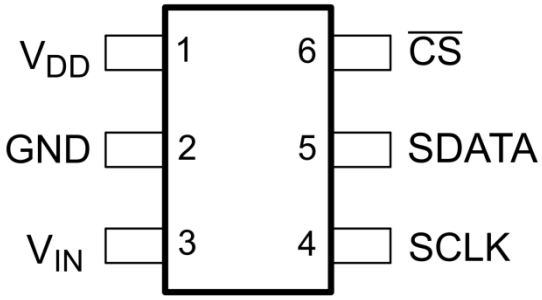


Figure 2. Pin Configuration

TERMINAL		DESCRIPTION
NAME	NO.	
V_{DD}	1	Power Supply Input. The V_{DD} range is from 3.3 V to 5.25 V.
GND	2	The ground return for the supply and signals.
V_{IN}	3	Analog Input. This signal can range from 0 V to V_{DD}.
SCLK	4	Digital clock input. This clock directly controls the conversion and readout processes.
SDATA	5	Digital data output. The output samples are clocked out of this pin on falling edges of the SCLK pin.
$\overline{CS}$	6	Chip Select. On the falling edge of $\overline{CS}$, a conversion process begins.

TYPICAL CONNECTION

Figure 3 shows a typical connection diagram for the CI7910/CI7920 . The 5 V supply should come from a stable power supply such as an LDO. The supply to CI7910/CI7920 should be decoupled to the ground. Two decoupling capacitors, one 1-µF and one 10-nF, are suggested to be inserted between the V_{DD} and GND pins of the converter. The capacitors should be placed as close as possible to the pins of the device. Always set the V_{DD} supply to be greater than or equal to the maximum input signal to avoid saturation of codes.

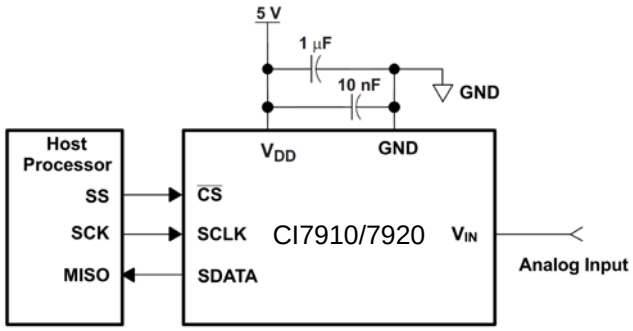


Figure 3. Typical Circuit Configuration

TIMING DIAGRAM

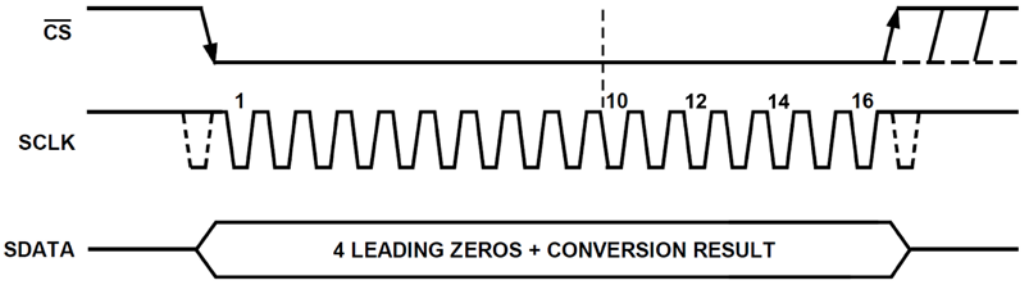


Figure 4. Timing Diagram

The conversion is initiated on the falling edge of $\overline{CS}$. The device outputs data while the conversion is in progress, and it requires 14/16 serial clock cycles to complete the conversion and access the full results. The CI7910 /CI7920 data word contains 4 leading zeros, followed by 10-bit/12-bit data in MSB first format.

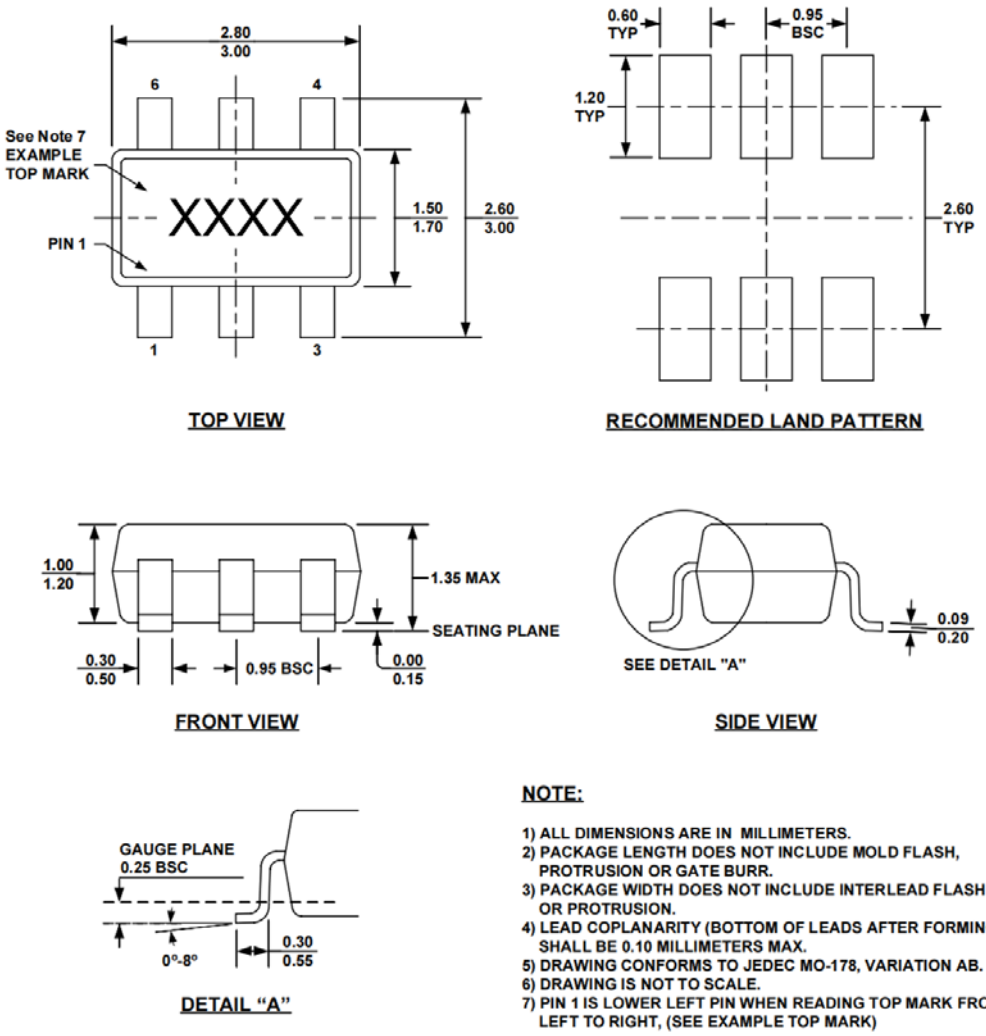
Once a data transfer is complete, SDATA will return to the tri-state mode, and another conversion can be initiated after the quiet time has elapsed by again bringing $\overline{CS}$ low.

POWER-DOWN MODE

The CI7910/20 family has an auto power-down feature. Besides powering down all circuitry, the converter consumes only a small amount of current in this mode. The device automatically wakes up when $\overline{CS}$ falls. However, not all of the functional blocks are fully powered until sometime before the third falling edge of SCLK. The device powers down once it reaches the end of conversion which is the 16th falling edge of SCLK for the CI7920 (the 14th for the CI7910, respectively). The device enters power down mode if $\overline{CS}$ goes high before the 10th SCLK falling edge. Ongoing conversion stops and SDATA goes to three-state under this power down condition.

These converters achieve lower power dissipation for a fixed throughput rate by using higher SCLK frequencies. Higher SCLK frequencies reduce the acquisition time and conversion time. This means the converters spend more time in auto power-down mode per conversion cycle. For a particular SCLK frequency, the acquisition time and conversion time are fixed. Therefore, a lower throughput increases the proportion of the time the converters are in power down, thereby reducing power consumption.

OUTLINE DIMENTIONS



NOTES

1. Unpacked ICs, tube-mounted ICs, etc. must be stored in a drying cabinet, and the humidity in the drying cabinet < 20% R.H.

2. After access, the components are stored in an electrostatic packaging protective bag.

3. Anti-static damage: the device is an electrostatic sensitive device, and sufficient anti-static measures should be taken during transmission, assembly and testing.

4. The user should conduct a visual inspection before use, and the bottom, side and surrounding of the circuit can be welded only if it is bright. If oxidation occurs, the circuit can be processed by means of oxidation, and the circuit must be soldered within 12 hours after processing.