ISL9116BIRN-EVZ

The ISL9116BIRN-EVZ platform allows quick evaluation of the high-performance features of the ISL9116B boost regulator. The ISL9116B is a highly integrated boost-switching regulator that accepts input voltages below the regulated output voltage. It features an extremely low quiescent current consumption, excellent efficiency, and an I^2C interface allowing access to its internal registers for output voltage and operation mode control.

Features

- Small, compact design
- I^2C interface for programmable V_{OUT}, slew rate and various operation modes (Auto-PFM, Forced PWM)
- Connectors, test points, and jumpers for easy probing

Specifications

The board operates with the following conditions:

- Input voltage rating from 0.8V to 5.5V
- Programmable output voltage range of 1.8V to 5.375V and selectable transition slew rate through I^2C interface
- Output current: up to $500\times(V_{IN}/V_{OUT})$mA ($V_{IN}$ > 2.5V)
- Operating temperature range: -40°C to +85°C

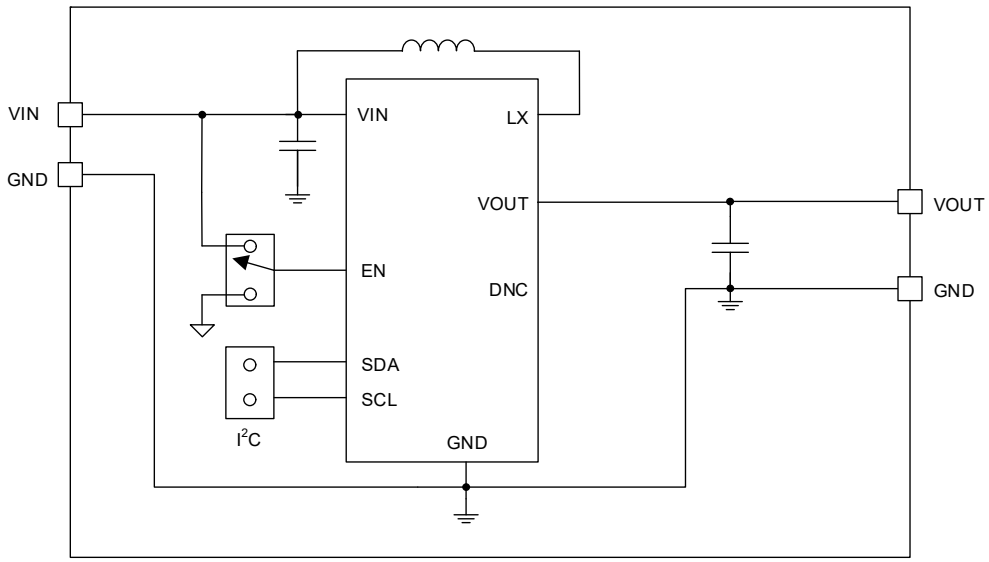

Figure 1. ISL9116BIRN-EVZ Block Diagram

Contents

1. Functional Description

The evaluation board (EVB) provides a simple platform to evaluate the feature-rich ISL9116B boost regulator. The board regulates at 3.3V output after start-up. The output voltage can be programmed by I^2C and is optimized to best perform with the ISL9116B IC series. The input power and load connections are provided through multi-pin connectors for high-current operations.

The evaluation board is shown in Figure 5. Table 1 lists the test points and jumpers for the boards. The ISL9116B internal registers can be accessed by I^2C through the onboard jumper header, J5, and its mode control register configures the part into the various operation modes. See Evaluation Software Installation and Use to configure the board output voltage and operation modes.

Table 1. Description of Test Points and Jumpers

Test Points	Description
J1	Header for connecting input power
J2	Header for connecting external load
J4	Header for the EN pin J4 = GND disables the part output; J4 = V_{IN} enables the part output
J5	Header for connecting I^2C interface
J1 S+/S-	V_{IN} Kelvin connection for efficiency measurements
J2 S+/S-	V_{OUT} Kelvin connection for efficiency measurements
TP1	Through Hole Mount PCB test point for LX
TP3	Through Hole Mount PCB test point for VOUT
TP4	Single turret terminal test point for VIN
TP5	Single turret terminal test point for VOUT
TP6	Single turret terminal test point for GND
TP7	Single turret terminal test point for GND

1.1 Operational Characteristics

The V_{IN} range is 0.8V to 5.5V, while the adjustable V_{OUT} range is 1.8V to 5.375V. The I_{OUT} range of the board is 0 to 500 × (V_{IN}/V_{OUT})mA (V_{OUT} > 2.5V). The operating ambient temperature range is -40°C to +85°C.

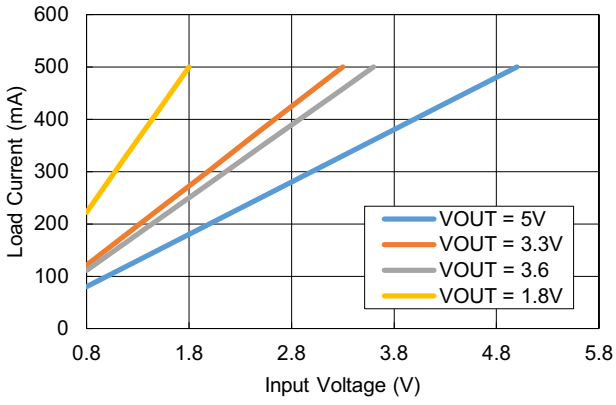

Figure 2. Maximum Load Current vs Input Voltage

1.2 Setup and Configuration

The default output voltage is set at 3.3V. Use the following procedures to configure and power up the board properly. During the power-on process, the expected waveforms are shown in Figure 3.

1. Connect the power supply to J1, with a voltage setting between 1.8V and 5.375V but lower than the output voltage setting for boost mode operation.
2. Connect the electronic load to J2.
3. Place the scope probes on the VOUT test point and other test points of interest.
4. Ensure the EN pin jumper (J4) is pulled up to V_{IN}.
5. Turn on the power supply. At the end of the soft-start sequence, the ISL9116B operates in Regulation mode at the default output voltage setting.

   Note: A minimum effective output capacitance of 6µF is required. Therefore, depending on the performance specifications of the capacitor, an additional output capacitor might be required for higher output voltage settings.
6. Monitor the output voltage start-up sequence on the scope. The waveforms should look similar to those shown in Figure 3.
7. Turn on the electronic load.
8. Measure the output voltage with the voltmeter. The voltage should regulate within the datasheet specification limits.
9. To determine efficiency, measure input and output voltages at the Kelvin sense test points (S+ and S-), which are part of the J1 and J2 headers. The bench power supply can be connected to the VIN and GND headers on J1. The electronic load can be connected to the VOUT and GND headers on J2. Measure the input and output currents. Calculate the efficiency based on these measurements.

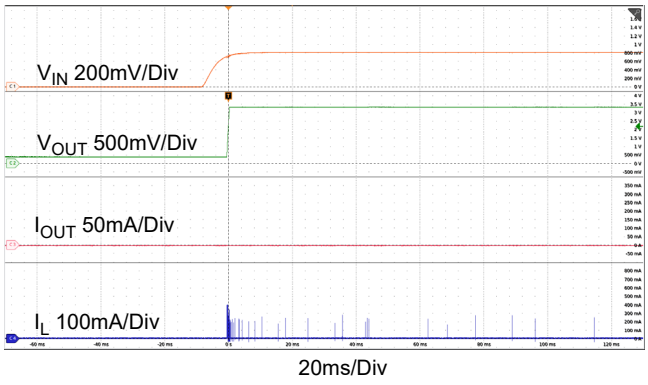

Figure 3. ISL9116B Start-Up with V_{IN} = 0.8V and V_{OUT} = 3.3V

1.3 Evaluation Software Installation and Use

The ISL9116B evaluation software and evaluation software manual are available for download from the Renesas website.

1. Save the evaluation software executable file and install the evaluation software (see the evaluation software manual). When the evaluation software launches (see the Setup and Configuration), connect the power supply, DC load, and other test equipment to the evaluation board; next, apply power.
2. The ISL9116B has various control registers. Refer to the *ISL9116B Datasheet* for detailed register descriptions.
3. Register **RO_REG1** (Address: 0x02) provides chip identification information. The **Get IC INFO_RO_REG1** button reads from this read-only register.

4. Use the **VSET Control** slider in the **VSET** register (Address: 0x11) panel to change the output voltage and perform a Write REG operation. The output voltage ramps up at the slew rate specified in the **DVSRATE** setting of the **CONV_CFG** register. If the modified output voltage is lower than the initial value, its ramp-down rate depends on the applied load and output capacitance. The **Read REG** button provides the contents of the register, so adjust the slider accordingly.
5. Register **INTFLG_REG** (Address: 0x03) contains the fault flags. The background color changes from green to red: when (1) a fault occurs and (2) this register is read using either the **Check Fault** button or the **READ ALL** button. Each bit is set by a fault event and cleared when read. When the bit is cleared after reading, the background color changes from red to green.
6. Register **CONV_CFG** (Address: 0x12) contains crucial converter configuration bits. Selecting the **Write** (or **Read)** button writes (or reads) the entire **CONV_CFG** register in one go.
7. Use the **DVSRATE** drop-down list to modify the dynamic voltage scaling rate for voltage ramp-up when the output voltage is modified using the **VSET** register.
8. Use the **FMODE** drop-down list to select one of the operating modes: **Normal** (Auto-PFM, default) and **Forced PWM.**
9. Use the **CTRL Type** drop-down list to select the control mode between **Type I** and **Type II** error amplifier.

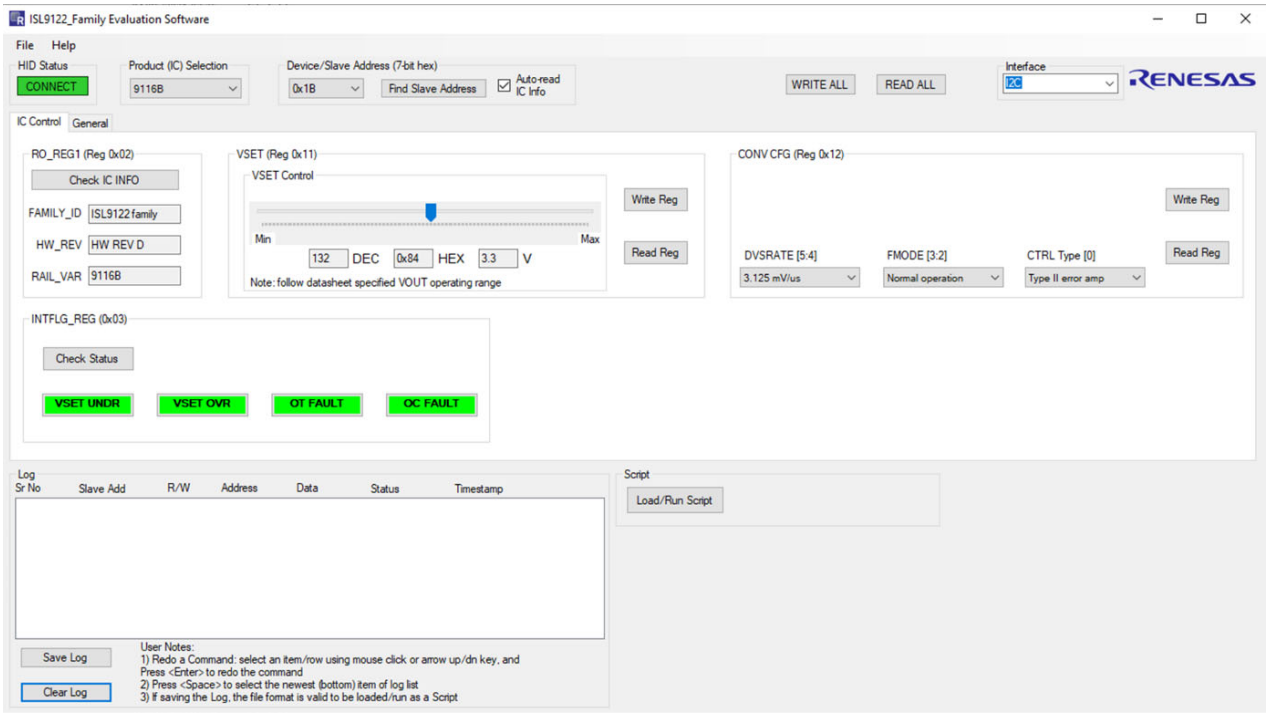

Figure 4. ISL9116B Evaluation Software Window

2. Board Design

2.1 ISL9116BIRN-EVZ

2.1.1 Board Image

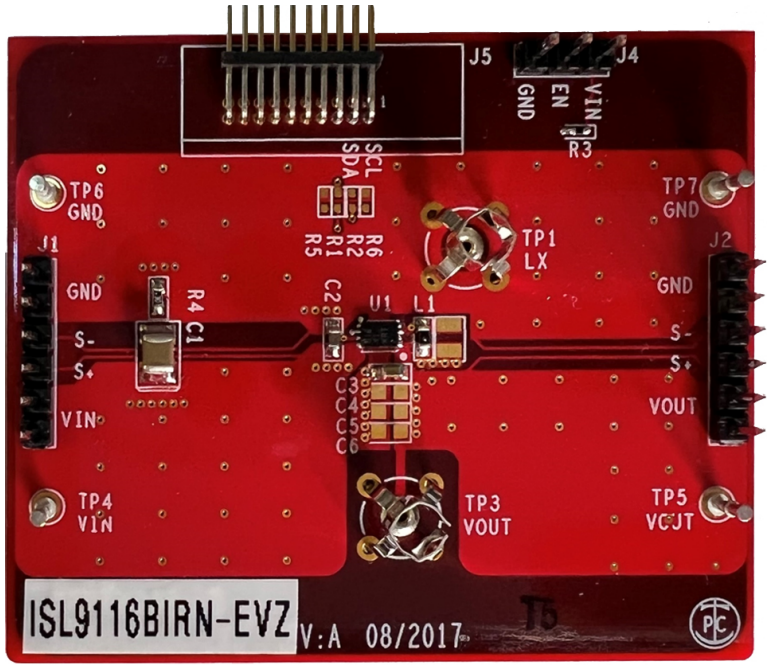

Figure 5. ISL9116BIRN-EVZ Evaluation Board (Top)

2.1.2 Circuit Schematic

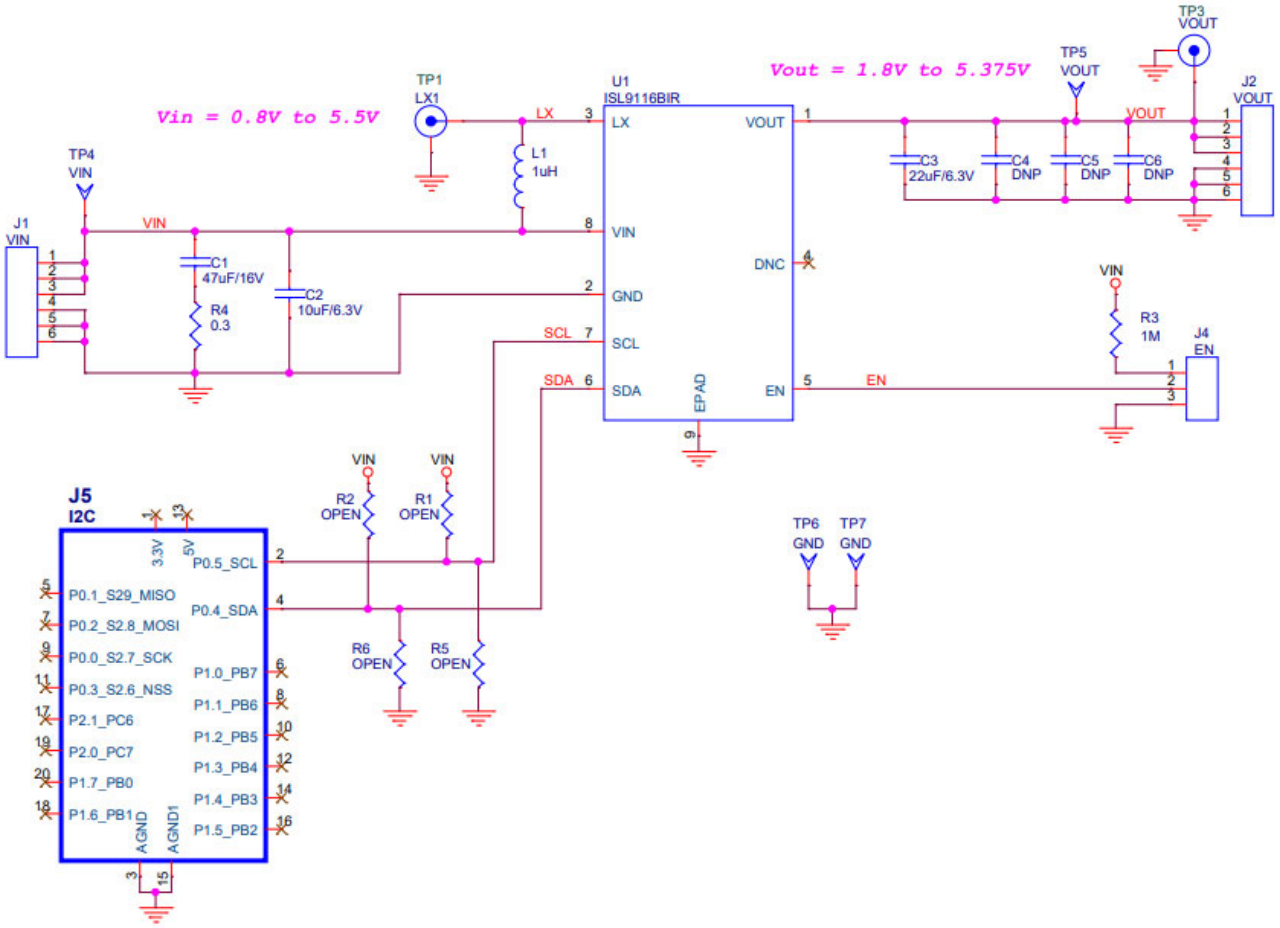

Figure 6. ISL9116BIRN-EVZ Circuit Schematic

2.1.3 Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
1	-	WB-PCB, ISL9116BIRN-EVZ, REVA, ROHS	MTL (Multilayer PCB International)	ISL9116BIRN-EVZREVAPCB
1	C1	CAP, SMD, 1210, 47µF, 16V, 20%, ROHS	Murata	GRM32ER61C476ME15L
1	C2	CAP, SMD, 0603, 10µF, 6.3V, 20%, X5R, ROHS	TDK	C1608X5R0J106M
1	C3	CAP, SMD, 0603, 22µF, 6.3V, 20%, X5R, ROHS	TDK	C1608X5R0J226M
0	C4, C5, C6	CAP, SMD, 0603, DNP-PLACE HOLDER, ROHS	-	-
1	L1	COIL-PWR INDUCTOR, SMD, 0603, 1µH, 20%1.7A, 128mΩ, ROHS	Murata	DFE18SAN1R0MG0L
2	TP1, TP3	CONN-SCOPE PROBE TEST PT, COMPACT, PCB MNT, ROHS	Tektronix	131-5031-00

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
4	TP4, TP5, TP6, TP7	CONN-TURRET, TH, SWAGE MNT, 0.230 LENGTH, ROHS	MILL-MAX	2110-2-00-80-00-00-07-0
1	J4	CONN-HEADER, 1×3, BREAKAWY 1×36, 2.54mm, ROHS	BERG/FCI	68000-236HLF
2	J1, J2	CONN-HEADER, 1×6, BRKAWY 1×36, 2.54mm, ROHS	BERG/FCI	68000-236HLF
1	J5	CONN-HEADER, TH, 2×10, 1.27mm PITCH, R/A, ROHS	Harwin Inc	M50-3901042
1	R3	RES, SMD, 0402, 1MEG, 1/16W, 1%, TF, ROHS	Pansonic	ERJ-2RKF1004X
0	R1, R2	RES, SMD, 0402, DNP, DNP, DNP, TF, ROHS	-	-
1	R4	RES, SMD, 0603, 0.3Ω, 1/10W, 1%, TF, ROHS	Yageo	RL0603FR-070R3L
0	R5, R6	RES, SMD, 0603, DNP-PLACE HOLDER, ROHS	-	-
1	U1	Ultra Low IQ Boost Regulator w/ Bypass, 8LD DFN 2×3, T&R Pb-Free w/ Anneal	Renesas Electronics America	ISL9116BIRNZ-T

2.1.4 Board Layout

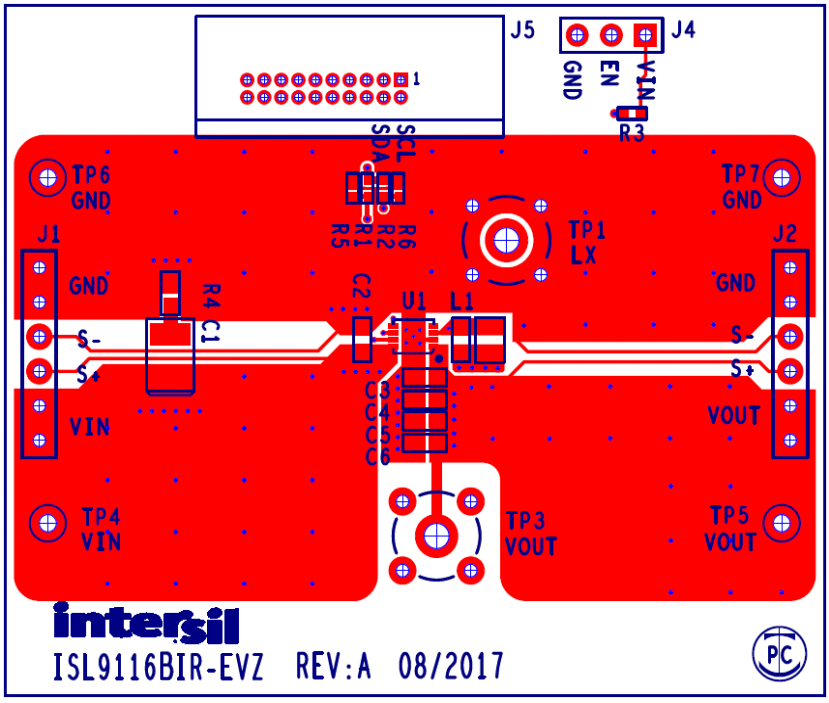

Figure 7. Top Layer Silk Screen

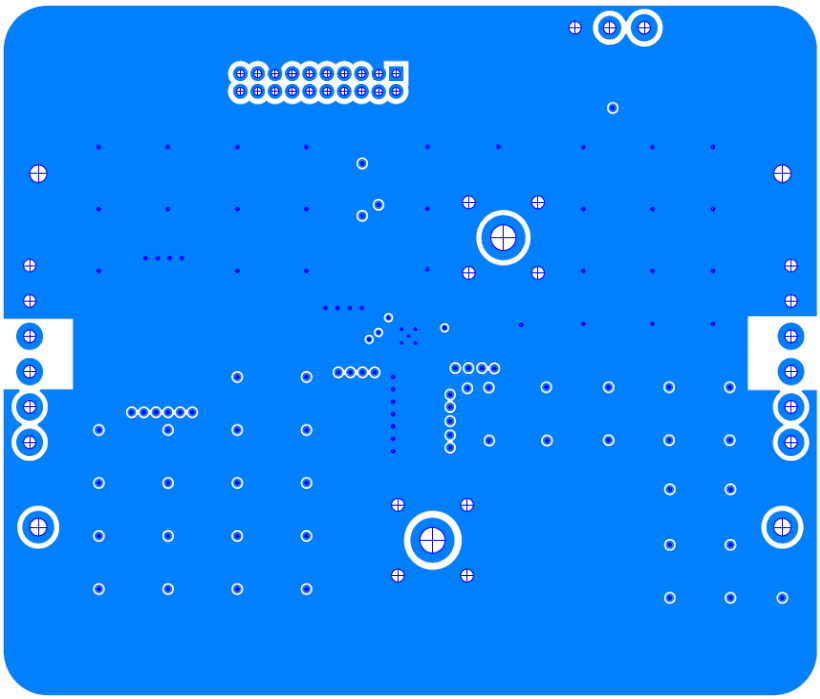

Figure 8. Inner Layer 2

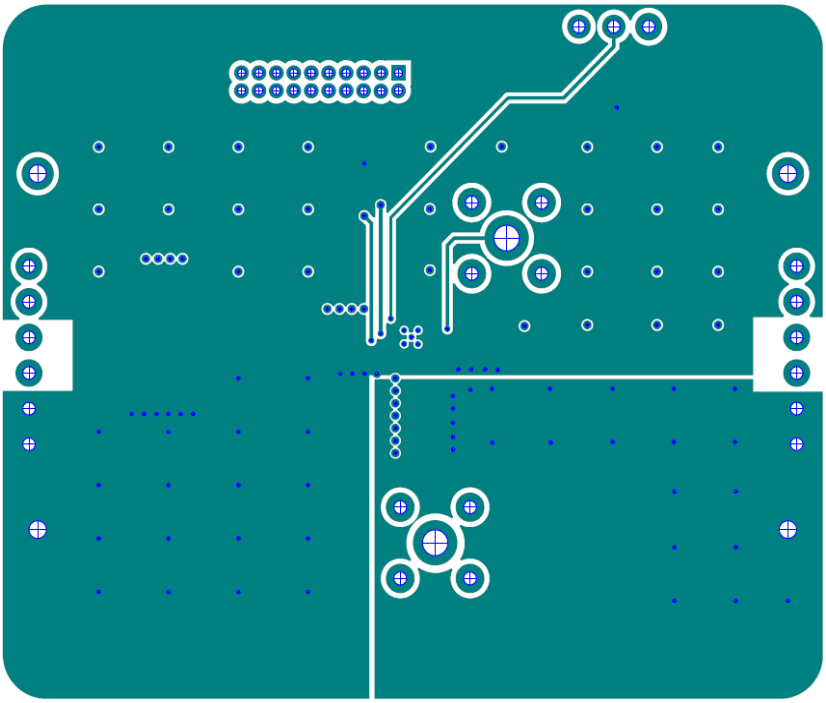

Figure 9. Inner Layer 3

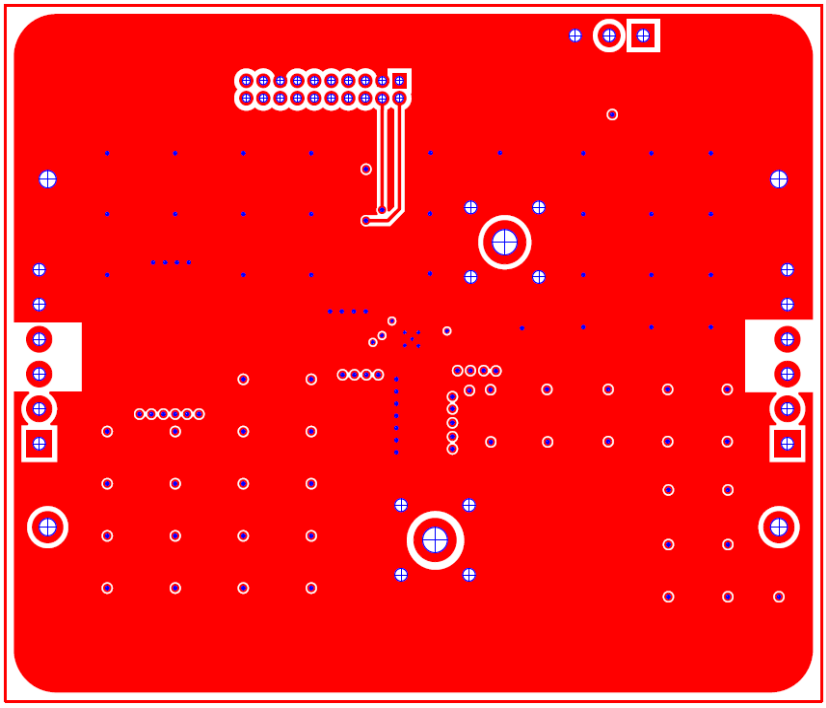

Figure 10. Bottom Layer Silk Screen

2.2 Layout Guidelines

The ISL9116BIRN-EVZ PCB layouts are optimized for electrical and thermal performance.

- Position the input and output capacitors as close to the IC as possible. The output currents are discontinuous in a boost converter; therefore, it is important to place the output capacitors as close as possible.
- Keep the ground connections of the input and output capacitors as short as possible and on the component layer to avoid problems that are caused by high-switching currents flowing through PCB vias. If it is necessary to use the vias, use multiple vias to minimize the effective trace inductance.
- It is strongly advised that the second layer be a clean GND to mitigate problems that arise from long GND traces and subsequent parasitic inductive components. Also, a clean GND shields the intermediate layers from high power traces on the top layer.
- After placing short input and output loops, place an inductor as close as possible to the IC. While being cautious of any EMI concerns, ensure that the switch node traces (from LX to the inductor) are short and wide.
- Finally, EN, SCL, SDA traces can be routed, but they should be routed away from high energy and high dV/dt traces to prevent mis-triggering. These traces can be routed through the intermediate layers.

Note: C1 and R4 are on the evaluation board to stabilize the input supply with long test leads, and they are not required in actual system boards.

3. Ordering Information

Part Number	Description
ISL9116BIRN-EVZ	Evaluation board for ISL9116BIRNZ

4. Revision History

Revision	Date	Description
1.01	Sep 28, 2023	Updated Chapters/sections structure. Updated BOM.
1.00	Jun 7, 2023	Initial release

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use o any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:

www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.