

EV8833A-D-00A

1.5A Thermoelectric Cooler Controller **Evaluation Board**

DESCRIPTION

The EV8833A-D-00A is an evaluation board for the MP8833A, a monolithic thermoelectric cooler controller with built-in internal power MOSFETs. It achieves 1.5A of continuous output current from a 2.7V to 5.5V input voltage range, with a thermoelectric cooler (TEC) voltage range. The TEC voltage is linearly controlled by the analog voltage.

Features such as TEC voltage and current limiting are controlled by the 400kHz I2C serial interface. The MP8833A is ideal for TEC device applications, such as optical laser diodes and fiber communication networks.

Full protection features include internal soft start, over-current protection (OCP), overvoltage protection (OVP), and over-temperature protection (OTP). The MP8833A is available in a space-saving QFN-16 (2mmx3mm) package.

ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Value	Units
Input voltage	V _{IN}	2.7 to 5.5	V
Output current	lout	1.5	Α

FEATURES

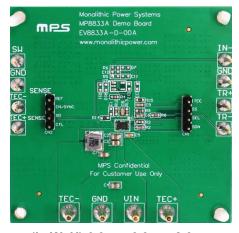
- 1% 2.5V REF Accuracy
- Wide 2.7V to 5.5V Operating Input Range
- Up to 1.5A TEC Current
- **High-Accuracy TEC Current Monitor**
- One-Time Programmable Frequency
- $30m\Omega$ Internal MOSFETs for PWM Switches and Linear Switches
- Default 1MHz Switching Frequency
- **External SYNC Function**
- EN/SD for Power Sequencing
- Available in a QFN-16 (2mmx3mm) Package

APPLICATIONS

- **Optical Laser Diode Modules**
- Fiber Communication Networks
- Required TEC Device Applications

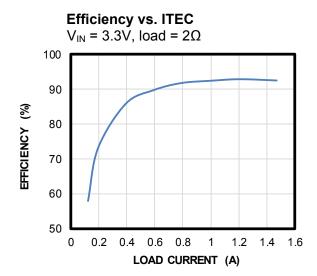
All MPS parts are lead-free halogen-free and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. "MPS", the MPS logo, and "Simple, Easy Solutions" are registered trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

EVALUATION BOARD



(LxWxH) 6.3cmx6.3cmx2.0cm

Board Number	MPS IC Number	
EV8833A-D-00A	MP8833AGD	



1



QUICK START GUIDE

The EV8833A-D-00A can work with the EV8833-Base-00A to get a closed-loop system. Refer to the MP8833A and EV8833-Base-Board datasheets for more details.

To operate the EV8833A-D-00A in open loop operation, follow the steps below:

- 1. Preset the power supply (V_{IN}) between 2.7V and 5.5V.
- 2. Turn the power supply off.
- 3. Connect the power supply terminals to:
 - a. Positive (+): VIN
 - b. Negative (-): GND
- 4. Connect the load to:
 - a. Positive (+): TEC+
 - b. Negative (-): TEC-
- 5. Turn the power supply on after making the connections. The board should start up automatically.
- 6. To adjust the TEC voltage and direction, connect the CTL pin to a voltage between 0V and 5V.



EVALUATION BOARD SCHEMATIC

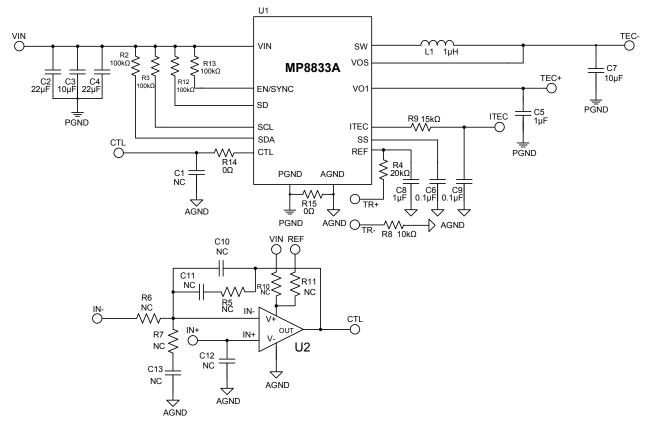


Figure 1: Typical Application Circuit for the MP8833AGD



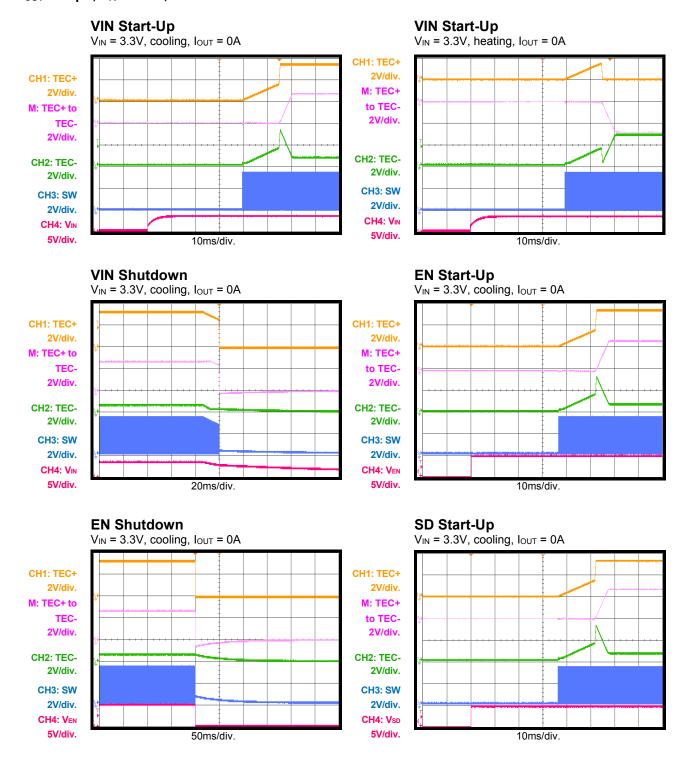
BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer P/N
2	C6, C9	100nF	Ceramic capacitor, 25V, X7R	0603	Murata	GRM188R71E104KA01D
2	C3, C7	10μF	Ceramic capacitor, 25V, X7S	0805	Murata	GRM21BC71E106KE11L
2	C2, C4	22µF	Ceramic capacitor, 25V, X5R	0805	Murata	GRM21BR61E226ME44L
2	C5, C8	1µF	Ceramic capacitor, 25V, X7R	0603	Murata	GRM188R71E105KA12D
4	R2, R3, R12, R13	100kΩ	Film resistor, 1%, 0603, $100k\Omega$	0603	Yageo	RC0603FR-07100KL
1	R9	15kΩ	Film resistor, 1%, 0603, 15kΩ	0603	Yageo	RC0603FR-0715KL
2	R14, R15	0Ω	Film resistor, 1%, 0603, 0R	0603	Yageo	RC0603FR-070RL
1	L1	1µH	Inductor, $R_{DC} = 27m\Omega$, $I_{SAT} = 9.0A$	4020	Wurth	74437324010
1	R4	20kΩ	Film resistor, 1%, 0603, $20k\Omega$	0603	Yageo	RC0603FR-0720KL
1	R8	10kΩ	Film resistor, 1%, 0603, $10k\Omega$	0603	Yageo	RC0603FR-0710KL
1	U1	MP8833A	1.5A thermoelectric cooler controller	QFN-16 (2mmx3mm)	MPS	MP8833AGD
0	C1, C10, C11, C12, C13	NC				
0	R5, R6, R7, R10, R11	NC				
0	U2	NC				



EVB TEST RESULTS

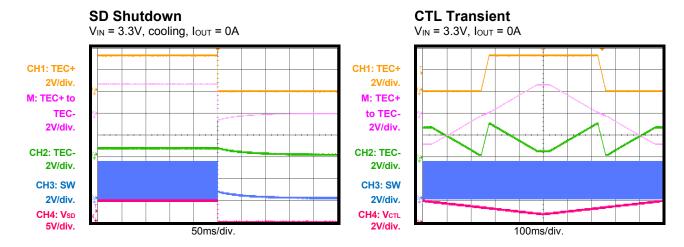
Performance curves and waveforms are tested on the evaluation board. V_{IN} = 3.3V, L = 1 μ H, C_{OUT} = 10 μ F, T_A = 25°C, unless otherwise noted.





EVB TEST RESULTS (continued)

Performance curves and waveforms are tested on the evaluation board. V_{IN} = 3.3V, L = 1 μ H, C_{OUT} = 10 μ F, T_A = 25°C, unless otherwise noted.





PCB LAYOUT

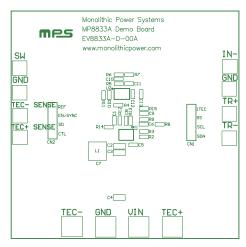


Figure 2: Top Silk Layer

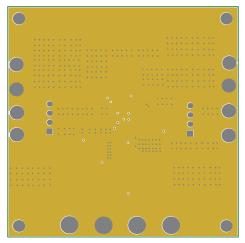


Figure 4: Mid-Layer 1

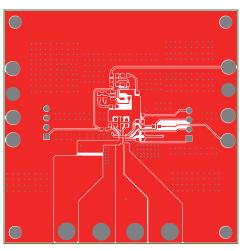


Figure 3: Top Layer

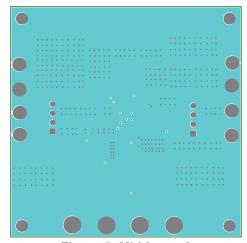


Figure 5: Mid-Layer 2

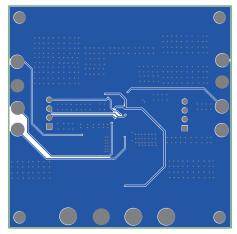


Figure 6: Bottom Layer

Notice: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third-party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.