



UFS Memory

MTFC32GAZAO, MTFC64GAZAO, MTFC128GAZAO, MTFC256GAZAO

Features

- Universal flash storage (UFS) controller and NAND Flash
- V_{CC} : 2.7–3.6V
- V_{CCQ2} : 1.7–1.95V
- JEDÉC/UFS specification version 2.1-compliant¹
 - Advanced 6-signal interface
 - Differential I/O pins
 - 2 lanes supported
 - High speed: Gear 1/2/3 supported
 - Permanent and power-on write protection
 - Boot operation (high-speed boot)
 - Sleep mode
 - Replay-protected memory block (RPMB)
 - Background operation
 - Reliable write
 - Discard/Erase
 - Command queuing
 - FFU
 - Cache
- JEDEC/UFS specification version 3.0-features²
 - REFRESH operation
 - Temperature event notification
- Package compliance:
 - RoHS certification
 - BGA, MSL3

| Options | Marking |
|---|----------------------------|
| • Density <ul style="list-style-type: none"> – 32GB – 64GB – 128GB – 256GB | 32G 64G 128G 256G |
| • NAND component <ul style="list-style-type: none"> – 256Gb | AZ |
| • Controller | AO |
| • Packages <ul style="list-style-type: none"> – 153-ball JEDEC-5V_{SS} TFBGA | TD |
| • Automotive and Functional Safety <ul style="list-style-type: none"> – AEC-Q104 – Automotive SPICE, Level 1 – PPAP – FMEDA (ISO 26262-5:2018, cl. 8, 9) – Safety Application Note | A ⁴ |
| • Operating temperature ranges ³ <ul style="list-style-type: none"> – From -40°C to +95°C – From -40°C to +105°C | IT AT |

Notes:

- The JEDEC specification is available at <https://www.jedec.org/sites/default/files/docs/JESD220C.pdf>.
- The JEDEC specification is available at <https://www.jedec.org/sites/default/files/docs/JESD220D.pdf>.
- Operating temperature (T_{OPER}) is the case surface temperature on the center/top of the package.
- For functional safety documentation, contact Micron sales representative.



Part Numbering Information

Micron® UFS memory devices are available in different configurations and densities.

Figure 1: UFS Part Numbering

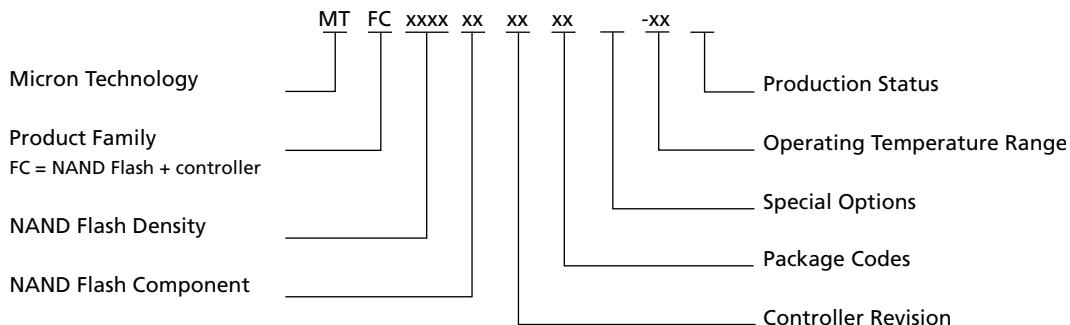


Table 1: Ordering Information

| Base Part Number | Density | Package | Notes |
|--|---------|--|-------|
| MTFC32GAZAOTD-AIT MTFC32GAZAOTD-AAT | 32GB | 153-ball JEDEC-5V _{SS} TFBGA 11.5mm × 13mm × 1.2mm | 1, 2 |
| MTFC64GAZAOTD-AIT MTFC64GAZAOTD-AAT | 64GB | 153-ball JEDEC-5V _{SS} TFBGA 11.5mm × 13mm × 1.2mm | 1, 2 |
| MTFC128GAZAOTD-AIT MTFC128GAZAOTD-AAT | 128GB | 153-ball JEDEC-5V _{SS} TFBGA 11.5mm × 13mm × 1.2mm | 1, 2 |
| MTFC256GAZAOTD-AIT MTFC256GAZAOTD-AAT | 256GB | 153-ball JEDEC-5V _{SS} TFBGA 11.5mm × 13mm × 1.2mm | 1, 2 |

Notes: 1. All the above MPNs can be ordered in the shipping form of tray and tape and reel.
 2. Products and specifications discussed herein are for evaluation and reference purposes only and are subject to change by Micron without notice. Products are only warranted by Micron to meet Micron's production data sheet specifications.

Device Marking

Due to the size of the package, the Micron-standard part number is not printed on the top of the device. Instead, an abbreviated device mark consisting of a 5-digit alphanumeric code is used. The abbreviated device marks are cross-referenced to the Micron part numbers at the FBGA Part Marking Decoder site: www.micron.com/decoder.



Contents

| | |
|---|----|
| Important Notes and Warnings | 6 |
| Functional Safety Notes | 7 |
| General Description | 8 |
| UFS Performance and Current Consumption | 8 |
| Signal Descriptions | 9 |
| Signal Assignments | 10 |
| Package Dimensions | 11 |
| Architecture | 12 |
| UFS M-PHY Attributes | 13 |
| UPIU Transaction Codes | 15 |
| UFS Descriptors | 15 |
| UFS Flags, Attributes, and Commands | 32 |
| UFS Supported Pages | 38 |
| UFS Vital Product Data Parameters | 44 |
| Electrical Specifications | 51 |
| Revision History | 52 |
| Rev. E – 04/2022 | 52 |
| Rev. D – 03/2022 | 52 |
| Rev. C – 01/2021 | 52 |
| Rev. B – 11/2020 | 52 |
| Rev. A – 05/2020 | 52 |



List of Figures

| | |
|---|----|
| Figure 1: UFS Part Numbering | 2 |
| Figure 2: 153-Ball JEDEC - 5V _{SS} (Top View, Ball Down) | 10 |
| Figure 3: 153-Ball TFBGA – 11.5mm × 13.0mm × 1.2mm (Package Code: TD) | 11 |
| Figure 4: UFS Functional Block Diagram..... | 12 |



List of Tables

| | |
|--|----|
| Table 1: Ordering Information | 2 |
| Table 2: Performance | 8 |
| Table 3: Active Current Consumption | 8 |
| Table 4: Low-Power Mode | 9 |
| Table 5: Signal Descriptions | 9 |
| Table 6: Recommended Capacitor Values | 12 |
| Table 7: PHY M-TX Capability Attributes | 13 |
| Table 8: PHY M-RX Capability Attributes | 13 |
| Table 9: UPIU Transaction Codes | 15 |
| Table 10: Descriptor Identification Values | 15 |
| Table 11: Configuration Descriptor | 15 |
| Table 12: Device Descriptor | 16 |
| Table 13: Geometry Descriptor | 20 |
| Table 14: Unit Descriptor | 24 |
| Table 15: RPMB Unit Descriptor | 26 |
| Table 16: Power Parameters Descriptor | 27 |
| Table 17: Interconnect Descriptor | 27 |
| Table 18: Manufacturer Name String Descriptor | 28 |
| Table 19: Product Name String Descriptor | 28 |
| Table 20: OEM ID String Descriptor | 30 |
| Table 21: Serial Number String Descriptor | 30 |
| Table 22: Product Revision Level String Descriptor | 30 |
| Table 23: Device Health Descriptor | 31 |
| Table 24: Flags | 32 |
| Table 25: Attributes | 33 |
| Table 26: SCSI Commands | 37 |
| Table 27: UFS Supported Pages | 38 |
| Table 28: Control Mode Page | 38 |
| Table 29: Read – Write Error Recovery Mode Page | 40 |
| Table 30: Caching Mode Page | 41 |
| Table 31: Supported VPD Pages | 44 |
| Table 32: Unit Serial Number VPD Page | 44 |
| Table 33: Device Identification VPD Page | 45 |
| Table 34: Mode Page Policy VPD Page | 46 |
| Table 35: Block Limits VPD Page | 47 |
| Table 36: Block Device Characteristics | 48 |
| Table 37: Logical Block Provisioning | 49 |
| Table 38: Standard Inquiry Data | 49 |
| Table 39: Power Supply Parameters | 51 |
| Table 40: Reference Clock Parameters ¹ | 51 |



Important Notes and Warnings

Micron Technology, Inc. ("Micron") reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions. This document supersedes and replaces all information supplied prior to the publication hereof. You may not rely on any information set forth in this document if you obtain the product described herein from any unauthorized distributor or other source not authorized by Micron.

Automotive Applications. Products are not designed or intended for use in automotive applications unless specifically designated by Micron as automotive-grade by their respective data sheets. Distributor and customer/distributor shall assume the sole risk and liability for and shall indemnify and hold Micron harmless against all claims, costs, damages, and expenses and reasonable attorneys' fees arising out of, directly or indirectly, any claim of product liability, personal injury, death, or property damage resulting directly or indirectly from any use of non-automotive-grade products in automotive applications. Customer/distributor shall ensure that the terms and conditions of sale between customer/distributor and any customer of distributor/customer (1) state that Micron products are not designed or intended for use in automotive applications unless specifically designated by Micron as automotive-grade by their respective data sheets and (2) require such customer of distributor/customer to indemnify and hold Micron harmless against all claims, costs, damages, and expenses and reasonable attorneys' fees arising out of, directly or indirectly, any claim of product liability, personal injury, death, or property damage resulting from any use of non-automotive-grade products in automotive applications.

Critical Applications. Products are not authorized for use in applications in which failure of the Micron component could result, directly or indirectly in death, personal injury, or severe property or environmental damage ("Critical Applications"). Customer must protect against death, personal injury, and severe property and environmental damage by incorporating safety design measures into customer's applications to ensure that failure of the Micron component will not result in such harms. Should customer or distributor purchase, use, or sell any Micron component for any critical application, customer and distributor shall indemnify and hold harmless Micron and its subsidiaries, subcontractors, and affiliates and the directors, officers, and employees of each against all claims, costs, damages, and expenses and reasonable attorneys' fees arising out of, directly or indirectly, any claim of product liability, personal injury, or death arising in any way out of such critical application, whether or not Micron or its subsidiaries, subcontractors, or affiliates were negligent in the design, manufacture, or warning of the Micron product.

Customer Responsibility. Customers are responsible for the design, manufacture, and operation of their systems, applications, and products using Micron products. ALL SEMICONDUCTOR PRODUCTS HAVE INHERENT FAILURE RATES AND LIMITED USEFUL LIVES. IT IS THE CUSTOMER'S SOLE RESPONSIBILITY TO DETERMINE WHETHER THE MICRON PRODUCT IS SUITABLE AND FIT FOR THE CUSTOMER'S SYSTEM, APPLICATION, OR PRODUCT. Customers must ensure that adequate design, manufacturing, and operating safeguards are included in customer's applications and products to eliminate the risk that personal injury, death, or severe property or environmental damages will result from failure of any semiconductor component.

Limited Warranty. In no event shall Micron be liable for any indirect, incidental, punitive, special or consequential damages (including without limitation lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort, warranty, breach of contract or other legal theory, unless explicitly stated in a written agreement executed by Micron's duly authorized representative.



Functional Safety Notes

This automotive UFS product family has been developed under an IATF 16949-compliant Quality Management System (QMS) to provide a level of systematic fault coverage as per ISO 26262 QM definition. Additional support may be available to customers who need to integrate Micron's products in their functional safety-related applications. This support may include Safety Analysis Report, reporting FMEDA results and metrics, Safety Application Note and Pin FMEA Report, providing guidelines and instructions for using Micron products in safety-related applications. Contact a Micron sales representative to initiate the process required to obtain the functional safety documentation.



General Description

Micron universal flash storage (UFS) is a communication and mass data storage device that includes an M-PHY interface, one or more NAND Flash components, and a controller on an advanced 6-signal bus, which is compliant with the UFS system specification. Its cost per bit, small package sizes, and high reliability make it an ideal choice for automotive applications, including information and entertainment, navigation tools, advanced driving assistance systems, and a variety of other industrial and portable products.

UFS Performance and Current Consumption

Table 2: Performance

| Condition ¹ | | Typical Values | | | | Unit |
|------------------------|-------|----------------|--------|--------|--------|------|
| | | 32GB | 64GB | 128GB | 256GB | |
| Sequential | Write | 130 | 250 | 500 | 625 | MB/s |
| | Read | 500 | 940 | 950 | 950 | MB/s |
| Random | Write | 24,000 | 49,000 | 65,000 | 65,000 | IOPS |
| | Read | 26,000 | 47,000 | 70,000 | 70,000 | IOPS |

Notes: 1. Two lanes, high-speed mode gear 3; Sequential access of 512KB chunk; Random access of 4KB chunk; Command queue depth = 32; Burst performance.
Additional performance data is provided in a separate document upon customer request, such as sustained and system performance on a specific application board, in system programming performance in manufacturing environment with Micron proprietary solution.

Table 3: Active Current Consumption

| Condition | Typical Values (I_{CC}/I_{CCQ2}) ^{1,3} | | | | Peak Values (I_{CC}/I_{CCQ2}) ^{2,3} | | | | Unit |
|-----------|---|---------|---------|---------|--|---------|---------|---------|------|
| | 32GB | 64GB | 128GB | 256GB | 32GB | 64GB | 128GB | 256GB | |
| Write | 60/365 | 105/365 | 150/365 | 255/365 | 250/560 | 400/560 | 550/560 | 700/560 | mA |
| Read | 50/465 | 105/465 | 115/465 | 130/465 | 200/560 | 360/560 | 450/560 | 510/560 | mA |

Notes: 1. Two lanes, high-speed mode gear 3; $V_{CC} = 3.3V$; $V_{CCQ2} = 1.8V$; $T_{OPER} = 85^{\circ}C$, measurements done as average RMS current consumption.
2. Two lanes, high-speed mode gear 3; $V_{CC} = 3.3V$; $V_{CCQ2} = 1.8V$; $T_{OPER} = 85^{\circ}C$, measurements done as maximum of average values in any 4 μ s operation windows.
3. Refer to electrical addendum for additional measurements results and conditions.

**Table 4: Low-Power Mode**

| Condition ^{1,2} | Typical Values (I _{CC} /I _{CCQ2}) | | | | Maximum Values (I _{CC} /I _{CCQ2}) | | | | Unit |
|--------------------------|--|--------|--------|---------|--|---------|---------|---------|------|
| | 32GB | 64GB | 128GB | 256GB | 32GB | 64GB | 128GB | 256GB | |
| Sleep | 35/500 | 45/500 | 70/500 | 120/500 | 70/650 | 100/650 | 150/650 | 300/650 | µA |
| Idle | 35/500 | 45/500 | 70/500 | 120/500 | 70/650 | 100/650 | 150/650 | 300/650 | µA |

Notes: 1. Two lanes, low-speed mode PWM gear 1, M-PHY in Hibernate; V_{CC} = 3.3V; V_{CCQ2} = 1.8V; T_{OPER} = 25°C.

2. Refer to electrical addendum for additional measurements results and conditions.

Signal Descriptions

Table 5: Signal Descriptions

| Symbol | Type | Description |
|--|--------------|---|
| REF_CLK | Input | Reference clock: When not active, this signal should be pull-down or driven LOW by the host SoC |
| RST_n | Input | Hardware reset signal |
| D _{IN0_t} , D _{IN0_c} | Input | Downstream data lane 0: Differential input signals into UFS device from the host |
| D _{IN1_t} , D _{IN1_c} | Input | Downstream data lane 1: Differential input signals into UFS device from the host |
| D _{OUT0_t} , D _{OUT0_c} | Output | Upstream data lane 0: Differential output signals from the UFS device to the host |
| D _{OUT1_t} , D _{OUT1_c} | Output | Upstream data lane 1: Differential output signals from the UFS device to the host |
| VSF[9:1] | Input/Output | Vendor specific function: VSF[9:1] must be left floating; VSF2 is not used. Exposing VSF balls on test points is recommended. |
| V _{CC} | Supply | Supply voltage for the NAND memory device |
| V _{CCQ2} | Supply | Supply voltage used for the M-PHY interface and the memory controller |
| V _{DDIQ} | Input | Input terminal to provide bypass capacitor for internal regulator related to the memory controller |
| V _{SS} | Supply | Ground |
| NC | – | No connect: NC pins must be connected to ground or left floating |
| RFU | – | Reserved for future use: RFU pins must be left floating |



Signal Assignments

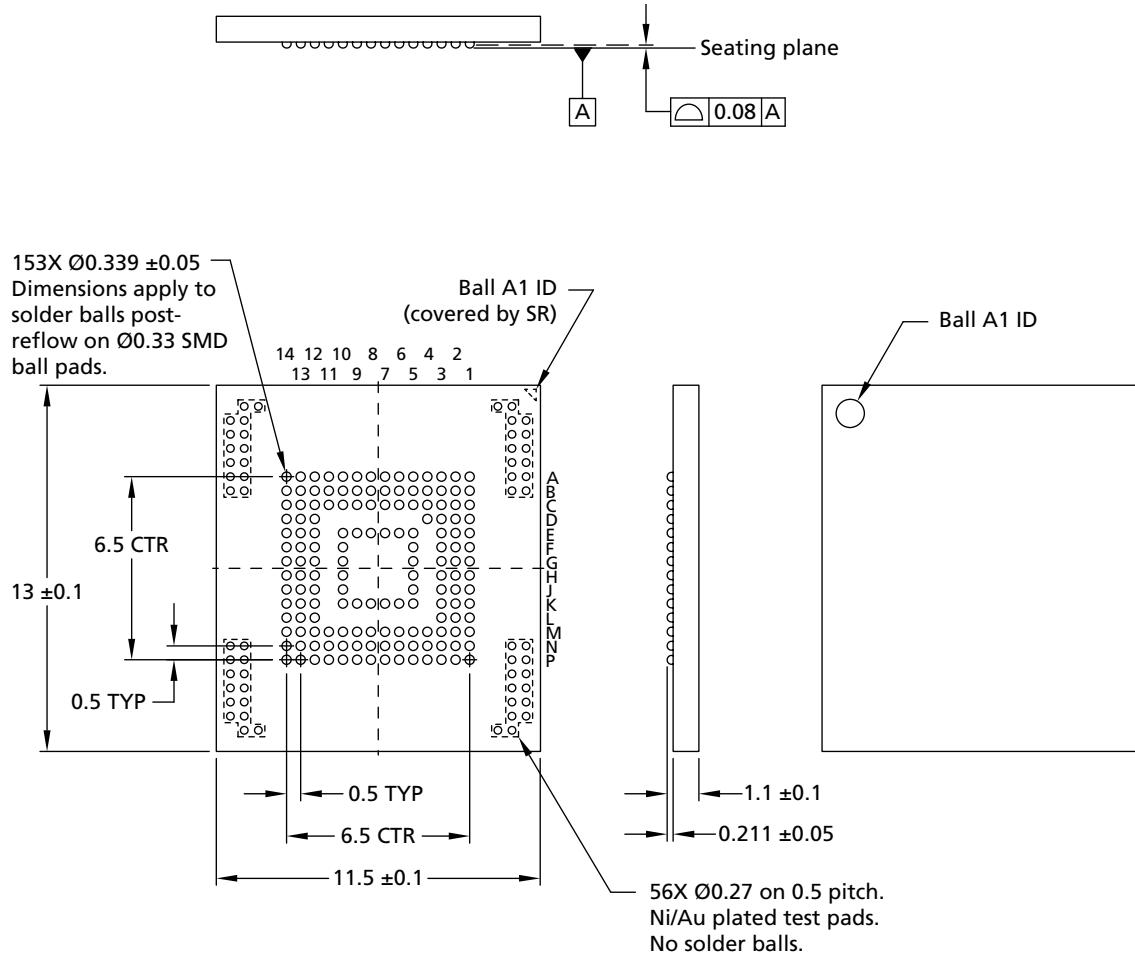
Figure 2: 153-Ball JEDEC - 5V_{SS} (Top View, Ball Down)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | | |
|---|----------------------|---------------------|-------------------|-----------------|-----------------|-------------------|-------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|---|
| A | NC | NC | V _{DDiQ} | NC | NC | V _{CCQ2} | V _{CCQ2} | NC | A | |
| B | NC | V _{SS} | RFU | NC | NC | V _{CCQ2} | V _{CCQ2} | V _{CC} | V _{CC} | NC | V _{SS} | V _{SS} | RFU | NC | B | |
| C | NC | V _{SS} | V _{SS} | NC | NC | V _{CCQ2} | V _{CCQ2} | V _{CC} | V _{CC} | RFU | V _{SS} | V _{SS} | RFU | RFU | C | |
| D | D _{IN1-t} | D _{IN1-c} | V _{SS} | NC | | | | | | | | | V _{SS} | V _{SS} | V _{SS} | D |
| E | NC | V _{SS} | V _{SS} | | NC | VSF1 | NC | V _{CC} | VSF3 | VSF4 | | | V _{SS} | RFU | RFU | E |
| F | D _{IN0-t} | D _{IN0-c} | V _{SS} | | NC | | | | | VSF5 | | | V _{SS} | V _{SS} | V _{SS} | F |
| G | NC | V _{SS} | V _{SS} | | VSF6 | | | | | V _{SS} | | | V _{SS} | RFU | RFU | G |
| H | REF_CLK | RST_n | V _{SS} | | V _{SS} | | | | | V _{SS} | | | V _{SS} | V _{SS} | V _{SS} | H |
| J | NC | V _{SS} | V _{SS} | | V _{SS} | | | | | VSF7 | | | V _{SS} | RFU | RFU | J |
| K | D _{OUT0-c} | D _{OUT0-t} | V _{SS} | | V _{SS} | V _{CCQ2} | V _{CCQ2} | V _{CC} | NC | VSF8 | | | V _{SS} | V _{SS} | V _{SS} | K |
| L | NC | V _{SS} | V _{SS} | | | | | | | | | | V _{SS} | RFU | RFU | L |
| M | D _{OUT1-c} | D _{OUT1-t} | V _{SS} | V _{SS} | V _{SS} | RFU | RFU | NC | NC | RFU | NC | V _{SS} | V _{SS} | V _{SS} | M | |
| N | NC | V _{SS} | V _{SS} | V _{SS} | V _{SS} | RFU | RFU | V _{CC} | V _{CC} | RFU | V _{SS} | V _{SS} | RFU | NC | N | |
| P | NC | NC | RFU | V _{SS} | V _{SS} | RFU | RFU | V _{CC} | V _{CC} | VSF9 | V _{SS} | V _{SS} | NC | NC | P | |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | | |
| | Top View (ball down) | | | | | | | | | | | | | | | |

Note: 1. The following balls are not connected in this product family, although specified by JEDEC Standard No. 21-C: A[5:4], A[12:8], B[5:4], B10, C[5:4], E5, E7, F5, C1, E1, G1, J1, L1.

Package Dimensions

Figure 3: 153-Ball TFBGA – 11.5mm x 13.0mm x 1.2mm (Package Code: TD)



Notes:

1. Dimensions are in millimeters.
2. For optimal solder join reliability (SJR) performance refer to CSN33 for recommended PCB pad dimension to align to the SMD ball pad size of the package.
3. In the whole UFS package area, solder mask is recommended to cover the via pad in the PCB in order to avoid possible contact with Ni/Au plated test pads on the UFS package. The Ni/Au plated test pads are reserved for Micron internal use only.

Architecture

Figure 4: UFS Functional Block Diagram

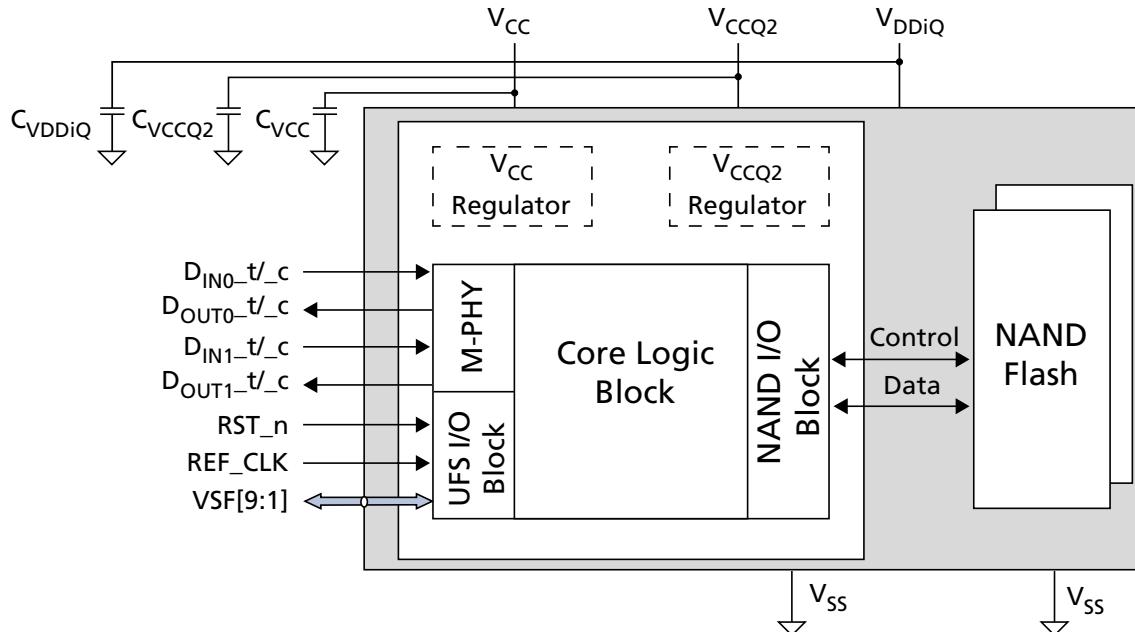


Table 6: Recommended Capacitor Values

| Parameters | Symbol | Min | Typ | Max | Unit |
|--|--------------------|-----|-----|-----|------|
| V _{CC} capacitor | C _{VCC} | 1.0 | 4.7 | – | μF |
| V _{CCQ2} capacitor | C _{VCCQ2} | 1.0 | 4.7 | – | μF |
| V _{DDiQ} capacitor ² | C _{VDDiQ} | 0 | 4.7 | – | μF |

Notes:

1. An additional capacitor on each of the three lines can be added with a value about 1/10th that of the current capacitors.
2. V_{DDiQ} capacitor is optional.



UFS M-PHY Attributes

Micron device supports 2 lanes configuration.

Table 7: PHY M-TX Capability Attributes

| Name | ID | Value Lane 0 Lane 1 | Type | Notes |
|--|-----|---------------------------|------|--|
| TX_HSMODE_Capability | 01h | 01h | R | FALSE = 0, TRUE = 1 |
| TX_HSGEAR_Capability | 02h | 03h | R | HS_G1_TO_G4 = 4 |
| TX_PWMG0_Capability | 03h | 00h | R | 0 = NO, 1 = YES |
| TX_PWMGEAR_Capability | 04h | 07h | R | Range from PWM_G1 to PWM_G7 |
| TX_Amplitude_Capability | 05h | 03h | R | SA = 1, LA = 2, BOTH = 3 |
| TX_ExternalSYNC_Capability | 06h | 01h | R | FALSE = 0, TRUE = 1 |
| TX_HS_Underminated_LINE_Drive_Capability | 07h | 01h | R | 0 = NO, 1 = YES |
| TX_LS_Terminated_LINE_Drive_Capability | 08h | 01h | R | 0 = NO, 1 = YES |
| TX_Min_SLEEP_NoConfig_Time_Capability | 09h | 08h | R | 1 to 15 |
| TX_Min_STALL_NoConfig_Time_Capability | 0Ah | 80h | R | 1 to 255 |
| TX_Min_SAVE_Config_Time_Capability | 0Bh | 7Fh | R | 1 to 250 |
| TX_REF_CLOCK_SHARED_Capability | 0Ch | 01h | R | 0 = NO, 1 = YES |
| TX_PHY_MajorMinor_Release_Capability | 0Dh | 30h | R | Bit[7:4]: Major version number Bit[3:0]: Minor version number |
| TX_PHY_Editorial_Release_Capability | 0Eh | 01h | R | Bit[7:0] = 1 to 99 |
| TX_Hibern8Time_Capability | 0Fh | 01h | R/W | 1 to 128 |
| TX_Advanced_Granularity_Capability | 10h | 05h | R/W | Bit[2:1]: Step size Bit[0]: Supports fine granularity steps |
| TX_Advanced_Hibern8Time_Capability | 11h | 07h | R/W | 1 to 128 |
| TX_HS_Equalizer_Setting_Capability | 12h | 03h | R | Bit[1:0] |

Table 8: PHY M-RX Capability Attributes

| Name | ID | Value Lane 0 Lane 1 | Type | Notes |
|--|-----|---------------------------|------|-----------------------------|
| RX_HSMODE_Capability | 81h | 01h | R | 0 = NO, 1 = YES |
| RX_HSGEAR_Capability | 82h | 03h | R | HS_G1_TO_G4 = 4 |
| RX_PWMG0_Capability | 83h | 00h | R | 0 = NO, 1 = YES |
| RX_PWMGEAR_Capability | 84h | 07h | R | Range from PWM_G1 to PWM_G7 |
| RX_HS_Underminated_LINE_Drive_Capability | 85h | 00h | R | 0 = NO, 1 = YES |

**Table 8: PHY M-RX Capability Attributes (Continued)**

| Name | ID | Value Lane 0 Lane 1 | Type | Notes |
|---|-----|---------------------------|------|---|
| RX_LS_Terminated_LINE_Drive_Capability | 86h | 01h | R | 0 = NO, 1 = YES |
| RX_Min_SLEEP_NoConfig_Time_Capability | 87h | 0Fh | R | 1-15 |
| RX_Min_STALL_NoConfig_Time_Capability | 88h | FAh | R | 1-255 |
| RX_Min_SAVE_Config_Time_Capability | 89h | FAh | R | 1-250 |
| RX_REF_CLOCK_SHARED_Capability | 8Ah | 01h | R/W | 0 = NO, 1 = YES |
| RX_HS_G1_SYNC_LENGTH_Capability | 8Bh | 49h | R/W | Bit[7:6]: SYNC_range FINE = 0, COARSE = 1 Bit[5:0]: SYNC-length 1 to 15 for FINE, 0 to 15 for COARSE |
| RX_HS_G1_PREPARE_LENGTH_Capability | 8Ch | 0Fh | R | 0-15 |
| RX_LS_PREPARE_LENGTH_Capability | 8Dh | 06h | R | 0-15 |
| RX_PWM_Burst_Closure_Length_Capability | 8Eh | 1Fh | R/W | 0-31 |
| RX_Min_ActivateTime_Capability | 8Fh | 04h | R/W | 1-9 |
| RX_PHY_MajorMinor_Release_Capability | 90h | 30h | R | Bit[7:4]: Major version number Bit[3:0]: Minor version number |
| RX_PHY_Editorial_Release_Capability | 91h | 01h | R | 1-99 |
| RX_Hibern8Time_Capability | 92h | 01h | R/W | 1-128 |
| RX_PWM_G6_G7_SYNC_LENGTH_Capability | 93h | 0Fh | R/W | Bit[7:6]: SYNC_range FINE = 0, COARSE = 1 Bit[5:0]: SYNC-length 0 to 15 |
| RX_HS_G2_SYNC_LENGTH_Capability | 94h | 4Ah | R/W | Bit[7:6]: SYNC_range FINE = 0, COARSE = 1 Bit[5:0]: SYNC-length 1 to 15 for FINE, 0 to 15 for COARSE |
| RX_HS_G3_SYNC_LENGTH_Capability | 95h | 4Bh | R/W | Bit[7:6]: SYNC_range FINE = 0, COARSE = 1 Bit[5:0]: SYNC-length 1 to 15 for FINE, 0 to 15 for COARSE |
| RX_HS_G2_PREPARE_LENGTH_Capability | 96h | 0Fh | R/W | Bit[3:0]: 0 to 15 |
| RX_HS_G3_PREPARE_LENGTH_Capability | 97h | 0Fh | R/W | Bit[3:0]: 0 to 15 |
| RX_Advanced_Granularity_Capability | 98h | 07h | R/W | Bit[2:1]: Step size Bit[0]: Supports fine granularity steps |
| RX_Advanced_Hibern8Time_Capability | 99h | 04h | R/W | 1-128 |
| RX_Advanced_Min_ActivateTime_Capability | 9Ah | 0Bh | R/W | Bit[3:0]: 1-14 |



UPIU Transaction Codes

Micron devices support the following UPIU transaction codes. For detailed information, refer to JEDEC UFS 2.1 specification.

Table 9: UPIU Transaction Codes

| Initiator to Target | Transaction Code | Target to Initiator | Transaction Code |
|-------------------------|------------------|--------------------------|------------------|
| NOP OUT | 00h | NOP IN | 20h |
| COMMAND | 01h | RESPONSE | 21h |
| DATA OUT | 02h | DATA IN | 22h |
| TASK MANAGEMENT REQUEST | 04h | TASK MANAGEMENT RESPONSE | 24h |
| Reserved | 11h | READY TO TRANSFER | 31h |
| QUERY REQUEST | 16h | QUERY RESPONSE | 36h |

UFS Descriptors

Descriptors are blocks or pages of parameters that describe something about the device. Descriptors are classified into types: device descriptors, configuration descriptors, unit descriptors and so forth. Micron devices support the following UFS descriptors. For detailed information, refer to the JEDEC UFS specification.

Table 10: Descriptor Identification Values

| Descriptor Type | Descriptor IDN |
|-----------------|----------------|
| Device | 00h |
| Configuration | 01h |
| Unit | 02h |
| Reserved | 03h |
| Interconnect | 04h |
| String | 05h |
| Reserved | 06h |
| Geometry | 07h |
| Power | 08h |
| Reserved | 09h...FFh |

Table 11: Configuration Descriptor

| Offset | Size | Name | Default Value | Description |
|--------|------|----------------|---------------|--|
| 00h | 1 | bLength | 90h | Size of this descriptor |
| 01h | 1 | bDescriptorIDN | 01h | Configuration descriptor type identifier |

**Table 11: Configuration Descriptor (Continued)**

| Offset | Size | Name | Default Value | Description |
|--------|------|---------------------|---------------|--|
| 02h | 1 | bConfDescContinue | 00h | 00h: This value indicates that this is the last configuration descriptor in a sequence of write descriptor query requests. Device shall perform internal configuration based on received configuration descriptor(s). 01h: This value indicates that this is not the last configuration descriptor in a sequence of write descriptor query requests. Other configuration descriptors will be sent by host. Therefore the device should not perform the internal configuration yet. |
| 03h | 1 | bBootEnable | 00h | Enables to boot feature. |
| 04h | 1 | bDescrAccessEn | 00h | Enables access to the device descriptor after the partial initialization phase of the boot sequence. |
| 05h | 1 | bInitPowerMode | 01h | Configures the power mode after device initialization or hardware reset. |
| 06h | 1 | bHighPriorityLUN | 7Fh | Configures the high priority logical unit. |
| 07h | 1 | bSecureRemoval-Type | 00h | Configures the secure removal type. |
| 08h | 1 | bInitActiveCCLevel | 00h | Configures the I _{CC} level in active mode after device initialization or hardware reset. |
| 09h | 2 | wPeriodicRTCUpdate | 00h | Frequency and method of real-time clock update (see Device Descriptor). |
| 0Bh | 1 | Reserved | – | |
| 0Ch | 1 | bRPMBRegionEnable | 00h | RPMB Region Enable Configures which RPMB regions are enabled in RPMB well known logical unit. |
| 0Dh | 1 | bRPMBRegion1Size | 00h | RPMB Region 1 Size Configures the size of RPMB region 1 if RPMB region 1 is enabled. |
| 0Eh | 1 | bRPMBRegion2Size | 00h | RPMB Region 2 Size Configures the size of RPMB region 2 if RPMB region 2 is enabled. |
| 0Fh | 1 | bRPMBRegion3Size | 00h | RPMB Region 3 Size Configures the size of RPMB region 3 if RPMB region 3 is enabled. |

Table 12: Device Descriptor

| Offset | Size | Name | Default Value | Description |
|--------|------|----------------|---------------|--|
| 00h | 1 | bLength | 40h | Size of this descriptor |
| 01h | 1 | bDescriptorIDN | 00h | Device descriptor type identifier |
| 02h | 1 | bDevice | 00h | Device type: 00h Others: Reserved |
| 03h | 1 | bDeviceClass | 00h | UFS device class: Mass storage: 00h |

**Table 12: Device Descriptor (Continued)**

| Offset | Size | Name | Default Value | Description |
|--------|------|--------------------|---------------|--|
| 04h | 1 | bDeviceSubClass | 00h | UFS mass storage subclass: Bits (0/1) specify as follows: Bit 0: Bootable/non-bootable Bit 1: Embedded/removable Bit 2: Reserved (for unified memory extension specification) Others: Reserved |
| 05h | 1 | bProtocol | 00h | Protocol supported by UFS device: SCSI: 00h |
| 06h | 1 | bNumberLU | 00h | Number of logical units (user configurable): bNumberLU does not include well known logical units. |
| 07h | 1 | bNumberWLU | 04h | Number of well known logical units |
| 08h | 1 | bBootEnable | 00h | Boot enable indicates whether the device is enabled for boot (user configurable): 00h: Boot feature disabled 01h: Bootable feature enabled |
| 09h | 1 | bDescrAccessEN | 00h | Descriptor access enable indicates whether the device descriptor can be read after the partial initialization phase of the boot sequence (user configurable): 00h: Device descriptor access disabled 01h: Device descriptor access enabled |
| 0Ah | 1 | bInitPowerMode | 01h | Initial power mode defines the power mode after device initialization or hardware reset (user configurable): 00h: UFS-sleep mode 01h: Active mode |
| 0Bh | 1 | bHighPriorityLUN | 7Fh | High priority LUN defines the high priority logical unit (user configurable): Valid values are from 0 to the number of logical units specified by bMaxNumberLU, and 7Fh. If the value is 7Fh, all logical units have the same priority. |
| 0Ch | 1 | bSecureRemovalType | 00h | Secure removal type (user configurable): 00h: Information removed by an erase of the physical memory 01h: Information removed by overwriting the addressed locations with a single character followed by an erase 02h: Information removed by overwriting the addressed locations with a character, its complement, then a random character 03h: Information removed using a vendor define mechanism Others: Reserved |
| 0Dh | 1 | bSecurityLU | 01h | Support for security LU: 00h: Not supported 01h: RPMB Others: Reserved |

**Table 12: Device Descriptor (Continued)**

| Offset | Size | Name | Default Value | Description |
|--------|------|-----------------------|---------------|---|
| 0Eh | 1 | bBackgroundOpsTermLat | 05h | Background operations termination latency defines the maximum latency for the termination of ongoing background operations. When the device receives a COMMAND UPIU with a transfer request, the device shall start the data transfer and send a DATA IN UPIU or an RTT UPIU within the latency declared in bBackgroundOpsTermLat. The latency is expressed in units of 10ms (for example, 01h = 10ms, FFh = 2550ms). The latency is undefined if the value of this parameter is 0. |
| 0Fh | 1 | bInitActiveICCLevel | 00h | Initial active I_{CC} level defines the bActiveICCLevel value after power-on or reset (user configurable): Valid range from 00h to 0Fh |
| 10h | 2 | wSpecVersion | 0210h | Specification version: Bits[15:8] = major version in BCD format Bits[7:4] = minor version in BCD format Bits[3:0] = version suffix in BCD format Example: 3.21 = 0321h |
| 12h | 2 | wManufactureDate | – | Manufacturing date: BCD version of the device manufacturing date Example: August 2010 = 0810h |
| 14h | 1 | iManufactureName | 00h | Manufacturer name: Index to the string which contains the manufacturer name |
| 15h | 1 | iProductName | 01h | Product name: Index to the string which contains the product name |
| 16h | 1 | iSerialNumber | 02h | Serial number: Index to the string which contains the serial number |
| 17h | 1 | iOEMID | 03h | OEM ID: Index to the string which contains the OEM ID |
| 18h | 2 | wManufactureID | 12Ch | Manufacturer ID: Manufacturer ID as defined in JEDEC standard JEP106 "Standard Manufacturer's Identification Code" |
| 1Ah | 1 | bUD0BaseOffset | 10h | Unit descriptor 0 base offset |
| 1Bh | 1 | bUDConfigPLength | 10h | Unit descriptor configuration parameter length: Total size of the configurable unit descriptor parameters |
| 1Ch | 1 | bDeviceRTTCap | 02h | RTT capability of device: Maximum number of outstanding RTTs supported by device. The minimum value is 2. |



Table 12: Device Descriptor (Continued)

| Offset | Size | Name | Default Value | Description |
|--------|------|---------------------|---------------|--|
| 1Dh | 2 | wPeriodicRTCUpdate | 0000h | <p>Frequency and method of real-time clock update (user configurable): Bits[15:10]: Reserved Bit[9]: TIME_BASELINE 0h: Time elapsed from the previous dSecondsPassed update 1h: Absolute time elapsed from January 1st 2010 00:00 NOTE if the host device has a real-time clock it should use TIME_BASELINE = 1. If the host device has no real-time clock it should use TIME_BASELINE = 0.</p> <p>Bits[8:6]: TIME_UNIT 000b = Undefined 001b = Months 010b = Weeks 011b = Days 100b = Hours 101b = Minutes 110b = Reserved 111b = Reserved</p> <p>Bits[5:0]: TIME_PERIOD If TIME_UNIT is 0, TIME_PERIOD is ignored and the period between RTC update is not defined. All fields are configurable by the host.</p> |
| 1Fh | 1 | bUFSFeaturesSupport | 7Fh | <p>UFS features support: This field indicates which features are supported by the device. A feature is supported if the related bit is set to 1.</p> <p>Bit[0]: Field firmware update (FFU) Bit[1]: Production state awareness (PSA) Bit[2]: Device life span Bit[3]: REFRESH operation (FFU) Bit[4]: TOO_HIGH_TEMPERATURE Bit[5]: TOO_LOW_TEMPERATURE Bit[6]: Extended temperature Others: Reserved Bit 0 shall be set to 1.</p> |
| 20h | 1 | bFFUTimeout | 0Ah | <p>Field firmware update timeout: The maximum time, in seconds, that access to the device is limited or not possible through any ports associated due to execution of a WRITE BUFFER command. A value of 0 indicates that no timeout is provided.</p> |
| 21h | 1 | bQueueDepth | 20h | <p>Queue depth: 0: The device implements the per-LU queuing architecture 1.. 255: The device implements the shared queuing architecture. This parameter indicates the depth of the shared queue. If bLUQueueDepth > 0 for any LU (except RPMB LU), then bQueueDepth shall be 0.</p> |
| 22h | 2 | wDeviceVersion | - | <p>Device version: This field provides the device version.</p> |

**Table 12: Device Descriptor (Continued)**

| Offset | Size | Name | | Default Value | Description |
|--------|------|-----------------------|-------|---------------|---|
| 24h | 1 | bNumSecureWPArea | | 20h | Number of secure write protect areas: This value specifies the total number of secure write protect areas supported by the device. The value shall be equal to or greater than bNumberLU and shall not exceed 32 (bNumberLU ≤ bNumSecureWPArea ≤ 32). |
| 25h | 4 | dPSAMaxDataSize | 32GB | 6C0AC0h | PSA maximum data size: This parameter specifies the maximum amount of data that may be written during the pre-soldering phase of the PSA flow. The value indicates the total amount of data for all logical units with bPSASensitive = 01h. Value expressed in units of 4KB. |
| | | | 64GB | D81580h | |
| | | | 128GB | 1B01540h | |
| | | | 256GB | 36014C0h | |
| 29h | 1 | bPSAStateTimeout | | 12h | PSA state timeout: This parameter specifies the command maximum timeout for a change in bPSAState state. 00h means undefined. Otherwise, the formula to calculate the maximum timeout value is: Production state timeout = $100\mu\text{s} \times 2^{\text{bPSAStateTimeout}}$ For example: 01h means $100\mu\text{s} \times 2^1 = 200\mu\text{s}$ 02h means $100\mu\text{s} \times 2^2 = 400\mu\text{s}$ 17h means $100\mu\text{s} \times 2^{23} = 838.86\text{s}$. |
| 2Ah | 1 | iProductRevisionLevel | | 04h | Product revision level: Index to the string which contains the product revision level |
| 2Bh | 5 | Reserved | | – | Reserved |
| 30h | 16 | Reserved | | – | Reserved for Unified Memory Extension specification |

Notes: 1. Some fields are user configurable as they can be configured by the user writing the configuration descriptor.
2. The reported values are referred to a fully provisioned device.

Table 13: Geometry Descriptor

| Offset | Size | Name | | Default Value | Description |
|--------|------|--------------------------|-------|---------------|--|
| 00h | 1 | bLength | | 48h | Size of this descriptor |
| 01h | 1 | bDescriptorIDN | | 07h | Geometry descriptor type identifier |
| 02h | 1 | bMediaTechnology | | 00h | Reserved |
| 03h | 1 | Reserved | | 00h | Reserved |
| 04h | 8 | qTotalRawDevice-Capacity | 32GB | 3B9C000h | Total raw device capacity: Total memory quantity available to the user to configure the device logical units (RPMB excluded). It is expressed in unit of 512 bytes. |
| | | | 64GB | 7738000h | |
| | | | 128GB | EE64000h | |
| | | | 256GB | 1DCBC000h | |
| 0Ch | 1 | bMaxNumberLU | | 01h | Maximum number of logical unit supported by the UFS device: 01h: 32 logical units |
| 0Dh | 4 | dSegmentSize | | 2000h | Segment size: Value expressed in unit of 512 bytes |

**Table 13: Geometry Descriptor (Continued)**

| Offset | Size | Name | Default Value | Description |
|--------|------|---------------------------------|---------------|--|
| 11h | 1 | bAllocationUnitSize | 01h | Allocation unit size: Value expressed in number of segments. Each logical unit can be allocated as a multiple of allocation units. |
| 12h | 1 | bMinAddrBlockSize | 08h | Minimum addressable block size: Value expressed in unit of 512 bytes. Its minimum value is 08h, which corresponds to 4KB. |
| 13h | 1 | bOptimalReadBlockSize | 40h | Optimal read block size: Value expressed in unit of 512 bytes. This is optional parameter, 0 = not available. |
| 14h | 1 | bOptimalWriteBlockSize | 40h | Optimal write block size: Value expressed in unit of 512 bytes |
| 15h | 1 | bMaxInBufferSize | 40h | Maximum data-in buffer size: Value expressed in unit of 512 bytes. Its minimum value is 08h, which corresponds to 4KB. |
| 16h | 1 | bMaxOutBufferSize | 40h | Maximum data-out buffer size: Value expressed in unit of 512 bytes. Its minimum value is 08h, which corresponds to 4KB. |
| 17h | 1 | bRPMB_ReadWriteSize | 20h | Maximum number of RPMB frames (256-byte of data) allowed in security protocol in and security protocol out (for example, associated with a single command UPIU). If the data to be transferred is larger than bRPMB_Read-WriteSize x 256 bytes, the host will transfer it using multiple SECURITY PROTOCOL IN/OUT commands. |
| 18h | 1 | bDynamicCapacityResource Policy | 01h | Dynamic capacity resource policy: This parameter specifies the device spare blocks resource management policy. 00h: Spare blocks resource management policy is per logical unit. The host should release amount of logical blocks from each logical unit as asked by the device. 01h: Spare blocks resource management policy is per memory type. The host may deallocate the required amount of logical blocks from any logical units with the same bMemoryType. |
| 19h | 1 | bDataOrdering | 00h | Support for out-of-order data transfer: 00h: Out-of-order data transfer is not supported by the device, in-order data transfer is required. 01h: Out-of-order data transfer is supported by the device. Others: Reserved |
| 1Ah | 1 | bMaxContextIDNumber | 20h | Maximum available number of contexts which are supported by the device: Minimum number of supported contexts shall be 5. |
| 1Bh | 1 | bSysDataTagUnitSize | 00h | bSysDataTagUnitSize provides system data tag unit size, which can be calculated as in the following (in bytes): Tag unit size = $2^{(bSysDataTagUnitSize)} \times bMinAdrBlockSize \times 512$ |

**Table 13: Geometry Descriptor (Continued)**

| Offset | Size | Name | Default Value | Description |
|--------|------|-----------------------|---------------|--|
| 1Ch | 1 | bSysDataTagResSize | 06h | Maximum storage area size in bytes allocated by the device to handle system data by the tagging mechanism: Valid range from 0 to 6 |
| 1Dh | 1 | bSupportedSecRTypes | 09h | Bit map which represents the supported secure removal types: Bit 0: Information removed by an erase of the physical memory Bit 1: Information removed by overwriting the addressed locations with a single character followed by an erase Bit 2: Information removed by overwriting the addressed locations with a character, its complement, then a random character. Bit 3: Information removed using a vendor define mechanism Others: Reserved A value of 1 means that the corresponding secure removal type is supported. |
| 1Eh | 2 | wSupportedMemoryTypes | 8009h | Bit map which represents the supported memory types: Bit 0: normal memory type Bit 1: System code memory type Bit 2: Non-persistent memory type Bit 3: Enhanced memory type 1 Bit 4: Enhanced memory type 2 Bit 5: Enhanced memory type 3 Bit 6: Enhanced memory type 4 Bit 7: Reserved ... Bit 14: Reserved Bit 15: RPMB memory type A value 1 means that the corresponding memory type is supported. Bit 0 and Bit 15 shall be 1 for all UFS device. |
| 20h | 4 | dSystemCodeMaxNAllocU | 0h | Maximum number of allocation units for the system code memory type: Maximum available quantity of system code memory type for the entire device. Value expressed in number of allocation unit. |
| 24h | 2 | wSystemCodeCapAdjFac | 0h | Capacity adjustment factor for the system code memory type: This parameter is the ratio between the capacity obtained with the normal memory type and the capacity obtained with the system code memory type for the same amount of allocation units. CapacityAdjFactor = CapacityNormalMem/CapacitySystemCode wSystemCodeCapAdjFac = INTEGER(256 × CapacityAdjFactor) |

**Table 13: Geometry Descriptor (Continued)**

| Offset | Size | Name | | Default Value | Description |
|--------|------|-----------------------|-------|---------------|--|
| 26h | 4 | dNonPersistMaxNAllocU | | 0h | Maximum number of allocation units for the non-persistent memory type: Maximum available quantity of non-persistent memory type for the entire device. Value expressed in number of allocation unit. |
| 2Ah | 2 | wNonPersistCapAdjFac | | 0h | Capacity adjustment factor for the non-persistent memory type: This parameter is the ratio between the capacity obtained with the normal memory type and the capacity obtained with the non-persistent memory type for the same amount of allocation units. CapacityAdjFactor = CapacityNormalMem/CapacityNon-Persist wNonPersistCapAdjFac = INTEGER(256 × CapacityAdjFactor) |
| 2Ch | 4 | dEnhanced1MaxNAllocU | 32GB | 1DCEh | Maximum number of allocation units for the enhanced memory type 1 |
| | | | 64GB | 3B9Ch | |
| | | | 128GB | 7732h | |
| | | | 256GB | EE5Eh | |
| 30h | 2 | wEnhanced1CapAdjFac | | 0300h | Capacity adjustment factor for the enhanced memory type 1 |
| 32h | 4 | dEnhanced2MaxNAllocU | | 00000000h | Maximum number of allocation units for the enhanced memory type 2: Maximum available quantity of enhanced memory type 2 for the entire device Value expressed in number of allocation unit. |
| 36h | 2 | wEnhanced2CapAdjFac | | 0h | Capacity adjustment factor for the enhanced memory type 2: This parameter is the ratio between the capacity obtained with the normal memory type and the capacity obtained with the enhanced memory type 2 for the same amount of allocation units. CapacityAdjFactor = CapacityNormalMem/CapacityEnhanced2 wEnhanced2CapAdjFac = INTEGER(256 × CapacityAdjFactor). |
| 38h | 4 | dEnhanced3MaxNAllocU | | 0h | Maximum number of allocation units for the enhanced memory type 3: Maximum available quantity of enhanced memory type 3 for the entire device Value expressed in number of allocation unit. |

**Table 13: Geometry Descriptor (Continued)**

| Offset | Size | Name | Default Value | Description |
|--------|------|--------------------------|---------------|---|
| 3Ch | 2 | wEnhanced2CapAdjFac | 0h | Capacity adjustment factor for the enhanced memory type 3: This parameter is the ratio between the capacity obtained with the normal memory type and the capacity obtained with the enhanced memory type 3 for the same amount of allocation units. CapacityAdjFactor = CapacityNormalMem/CapacityEnhanced3 wEnhanced3CapAdjFac = INTEGER(256 × CapacityAdjFactor). |
| 3Eh | 4 | dEnhanced4MaxNAllocU | 0h | Maximum number of allocation units for the enhanced memory type 4: Maximum available quantity of enhanced memory type 4 for the entire device Value expressed in number of Allocation Unit. |
| 42h | 2 | wEnhanced4CapAdjFac | 0h | Capacity adjustment factor for the enhanced memory type 4: This parameter is the ratio between the capacity obtained with the normal memory type and the capacity obtained with the enhanced memory type 4 for the same amount of allocation units. CapacityAdjFactor = CapacityNormalMem/CapacityEnhanced4 wEnhanced4CapAdjFac = INTEGER(256 × CapacityAdjFactor). |
| 44h | 2 | dOptimalLogicalBlockSize | 0h | Optimal logical block size: Bit [3:0]: Normal memory type Bit [7:4]: System code memory type Bit [11: 8]: Non-persistent memory type Bit [15:12]: Enhanced memory type 1 Bit [19:16]: Enhanced memory type 2 Bit [23:20]: Enhanced memory type 3 Bit [27:24]: Enhanced memory type 4 Bit [31:28]: Reserved The optimal logical block size for each memory type can be calculated from the related dOptimalLogicalBlockSize field as indicated in the following: Optimal logical block size = $2^{\text{(dOptimalLogicalBlockSize field)}} \times \text{bMinAddrBlockSize} \times 512$ byte. |

Table 14: Unit Descriptor

| Offset | Size | Name | Value | Description |
|--------|------|----------------|------------|---------------------------------|
| 00h | 1 | bLength | 23h | Size of this descriptor |
| 01h | 1 | bDescriptorIDN | 02h | Unit descriptor type identifier |
| 02h | 1 | bUnitIndex | 00h to 1Fh | Unit index |

**Table 14: Unit Descriptor (Continued)**

| Offset | Size | Name | Value | Description |
|--------|------|--------------------|-------|--|
| 03h | 1 | bLUEnable | 00h | Logical unit enable (user configurable): 00h: Logical unit disabled 01h: Logical unit enabled Others: Reserved |
| 04h | 1 | bBootLunID | 00h | Boot LUN ID (user configurable): 00h: Not bootable 01h: Boot LU A 02h: Boot LU B Others: Reserved |
| 05h | 1 | BLUWriteProtect | 00h | Logical unit write protect (user configurable): 00h: LU not write protected 01h: LU write protected when fPowerOnWPEn = 1 02h: LU permanently write protected when fPermanentWPEn = 1 03h: Reserved (for UFS Security Extension specification) Others: Reserved |
| 06h | 1 | bLUQueueDepth | 00h | Logical unit queue depth: Queue depth available in this LU. Queue depth of 0 means best effort by device to service the command task. |
| 07h | 1 | bPSASensitive | 01h | 00h: LU is not sensitive to soldering 01h: LU is sensitive to soldering Others: Reserved |
| 08h | 1 | bMemoryType | 00h | Memory type defines the logical unit memory type (user configurable): 00h: Normal memory 01h: System code memory type 02h: Non-persistent memory type 03h: Enhanced memory type 1 04h: Enhanced memory type 2 05h: Enhanced memory type 3 06h: Enhanced memory type 4 Others: Reserved |
| 09h | 1 | bDataReliability | 00h | Data reliability (user configurable): 00h: The logical unit is not protected. Logical unit's entire data might be lost as a result of a power failure during a WRITE operation. 01h: The logical unit is protected. Logical unit's data is protected against power failure. Others: Reserved |
| 0Ah | 1 | bLogicalBlockSize | 0Ch | Logical block size (user configurable): 0Ch (minimum value which corresponds to 4KB)–0Fh |
| 0Bh | 8 | qLogicalBlockCount | 00h | Logical block count (user configurable): Total number of addressable logical blocks in the LU in logical block size unit |
| 13h | 4 | dEraseBlockSize | 00h | Erase block size: In number of logical blocks |
| 17h | 1 | bProvisioningType | 00h | Provisioning type (user configurable): 00h: Thin provisioning is disabled. (default) 02h: Thin provisioning is enabled and TPRZ = 0. 03h: Thin provisioning is enabled and TPRZ = 1. Others: Reserved |

**Table 14: Unit Descriptor (Continued)**

| Offset | Size | Name | Value | Description |
|---------|------|--------------------------|-------|---|
| 18h:1Fh | 8 | qPhyMemResource-Count | 00h | Physical memory resource count: Total physical memory resource available in the logical unit |
| 20h | 2 | wContextCapabilities | 00h | (User configurable) Bits[3:0]: MaxContextID is the maximum amount of contexts that the LU supports simultaneously. The sum of all MaxContextID must not exceed bMaxContextIDNumber. Bits[6:4]: LARGE_UNIT_MAX_MULTIPLIER_M1 Bits[15:7]: Reserved |
| 22h | 1 | bLargeUnitGranularity_M1 | 00h | Granularity of the large unit, minus 1: Large unit granularity = 1MB (bLargeUnitGranularity_M1 + 1) |

Notes: 1. Some fields are user configurable as they can be configured by the user writing the configuration descriptor.

Table 15: RPMB Unit Descriptor

| Offset | Size | Name | Value | Description |
|--------|------|--------------------|--------|--|
| 00h | 1 | bLength | 23h | Size of this descriptor |
| 01h | 1 | bDescriptorIDN | 02h | Unit descriptor type identifier |
| 02h | 1 | bUnitIndex | C4h | Unit index |
| 03h | 1 | bLUEnable | 01h | Logical unit enable 01h: Logical unit enabled. |
| 04h | 1 | bBootLunID | 00h | Boot LUN ID 00h: Not bootable. |
| 05h | 1 | bLUWriteProtect | 00h | Logical unit write protect 00h: LU not write protected. |
| 06h | 1 | bLUQueueDepth | 00h | Logical unit queue depth: 0: RPMB LU queue not available (shared queuing is used) 1: Queue depth available in RPMB LU. Only 1 task may be queued at any given time |
| 07h | 1 | bPSASensitive | 01h | 00h: LU is not sensitive to soldering 01h: LU is sensitive to soldering Others: Reserved |
| 08h | 1 | bMemoryType | 0Fh | Memory type 0Fh: RPMB memory type |
| 09h | 1 | bRPMBRegionEnable | 0h | RPMB region enable: Bit 0: Don't care. RPMB region 0 is always enabled independent of this bit value. Bit 1: If set to 1, RPMB region 1 is enabled. Bit 2: If set to 1, RPMB region 2 is enabled. Bit 3: If set to 1, RPMB region 3 is enabled. Bit 4 to Bit 7: Reserved. |
| 0Ah | 1 | bLogicalBlockSize | 08h | Logical block size The size of addressable logical blocks is equal to the result of exponentiation with as base the number two and as exponent the bLogicalBlockSize value: $2^{(bLogicalBlockSize)}$ (for example, bLogicalBlockSize = 08h corresponds to 256 byte logical block size) |
| 0Bh | 8 | qLogicalBlockCount | 10000h | Logical block count |
| 13h | 1 | bRPMBRegion0Size | 00h | (User configurable) RPMB region 0 size |

**Table 15: RPMB Unit Descriptor (Continued)**

| Offset | Size | Name | Value | Description |
|---------|------|-----------------------|--------|--|
| 14h | 1 | bRPMBRegion1Size | 00h | (User configurable) RPMB region 1 size |
| 15h | 1 | bRPMBRegion2Size | 00h | (User configurable) RPMB region 2 size |
| 16h | 1 | bRPMBRegion3Size | 00h | (User configurable) RPMB region 3 size |
| 17h | 1 | bProvisioningType | 00h | Provisioning type |
| 18h:1Fh | 8 | qPhyMemResource-Count | 10000h | Physical memory resource count |
| 20h:22h | 3 | Reserved | 0h | Reserved |

Table 16: Power Parameters Descriptor

| Offset | Size | Name | Value | Description |
|--------|------|----------------------------|-------|---|
| 00h | 1 | bLength | 62h | Size of this descriptor |
| 01h | 1 | bDescriptorIDN | 08h | Power parameters descriptor type identifier |
| 02h | 2 | wActiveICCLevelsVCC[0] | 82BCh | Maximum V_{CC} current value for bActiveICCLevel = 0 |
| 04h | 2 | wActiveICCLevelsVCC[1] | 82BCh | Maximum V_{CC} current value for bActiveICCLevel = 1 |
| ... | ... | ... | ... | ... |
| 20h | 2 | wActiveICCLevelsVCC[15] | 82BCh | Maximum V_{CC} current value for bActiveICCLevel = 15 |
| 22h | 2 | wActiveICCLevelsVCCQ[0] | 0h | Maximum V_{CCQ} current value for bActiveICCLevel = 0 |
| 24h | 2 | wActiveICCLevelsVCCQ[1] | 0h | Maximum V_{CCQ} current value for bActiveICCLevel = 1 |
| ... | ... | ... | ... | ... |
| 40h | 2 | wActiveICCLevelsVCCQ[15] | 0h | Maximum V_{CCQ} current value for bActiveICCLevel = 15 |
| 42h | 2 | wActiveICCLevelsVC-CQ2[0] | 82BCh | Maximum V_{CCQ2} current value for bActiveICCLevel = 0 |
| 44h | 2 | wActiveICCLevelsVC-CQ2[1] | 82BCh | Maximum V_{CCQ2} current value for bActiveICCLevel = 1 |
| ... | ... | ... | ... | ... |
| 60h | 2 | wActiveICCLevelsVC-CQ2[15] | 82BCh | Maximum V_{CCQ2} current value for bActiveICCLevel = 15 |

Table 17: Interconnect Descriptor

| Offset | Name | Value | Description |
|--------|------------------|-------|--|
| 00h | bLength | 06h | Size of this descriptor |
| 01h | bDescriptorIDN | 04h | Interconnect descriptor type identifier |
| 02h | bcdUniproVersion | 0160h | MIPI UniPro version number in BCD format (for example, version 3.21 = 0321h) |

**Table 17: Interconnect Descriptor (Continued)**

| Offset | Name | Value | Description |
|--------|----------------|-------|---|
| 04h | bcdMphyVersion | 0300h | MIPI M-PHY version number in BCD format (for example, version 3.21 = 0321h) |

Table 18: Manufacturer Name String Descriptor

| Offset | Size | Name | Value | Description |
|--------|------|----------------|-------|-----------------------------------|
| 00h | 1 | bLength | 12h | Size of this descriptor |
| 01h | 1 | bDescriptorIDN | 05h | String descriptor type identifier |
| 02h | 2 | UC[0] | 004Dh | Unicode string character |
| 04h | 2 | UC[1] | 0049h | Unicode string character |
| 06h | 2 | UC[2] | 0043h | Unicode string character |
| 08h | 2 | UC[3] | 0052h | Unicode string character |
| 0Ah | 2 | UC[4] | 004Fh | Unicode string character |
| 0Ch | 2 | UC[5] | 004Eh | Unicode string character |
| 0Eh | 2 | UC[6] | 0020h | Unicode string character |
| 10h | 2 | UC[7] | 0020h | Unicode string character |

Table 19: Product Name String Descriptor

| Offset | Size | Name | Value | Description |
|--------|------|----------------|--------------------------------|-----------------------------------|
| 00h | 1 | bLength | 22h | Size of this descriptor |
| 01h | 1 | bDescriptorIDN | 05h | String descriptor type identifier |
| 02h | 2 | UC[0] | 32GB 64GB 128GB 256GB | 004Dh 004Dh 004Dh 004Dh |
| 04h | 2 | UC[1] | 32GB 64GB 128GB 256GB | 0054h 0054h 0054h 0054h |
| 06h | 2 | UC[2] | 32GB 64GB 128GB 256GB | 0030h 0030h 0031h 0032h |
| 08h | 2 | UC[3] | 32GB 64GB 128GB 256GB | 0033h 0036h 0032h 0035h |

**Table 19: Product Name String Descriptor (Continued)**

| Offset | Size | Name | Value | Description |
|--------|------|--------|-------|-------------|
| 0Ah | 2 | UC[4] | 32GB | 0032h |
| | | | 64GB | 0034h |
| | | | 128GB | 0038h |
| | | | 256GB | 0036h |
| 0Ch | 2 | UC[5] | 32GB | 0047h |
| | | | 64GB | 0047h |
| | | | 128GB | 0047h |
| | | | 256GB | 0047h |
| 0Eh | 2 | UC[6] | 32GB | 0041h |
| | | | 64GB | 0041h |
| | | | 128GB | 0041h |
| | | | 256GB | 0041h |
| 10h | 2 | UC[7] | 32GB | 005Ah |
| | | | 64GB | 005Ah |
| | | | 128GB | 005Ah |
| | | | 256GB | 005Ah |
| 12h | 2 | UC[8] | 32GB | 0041h |
| | | | 64GB | 0041h |
| | | | 128GB | 0041h |
| | | | 256GB | 0041h |
| 14h | 2 | UC[9] | 32GB | 004Fh |
| | | | 64GB | 004Fh |
| | | | 128GB | 004Fh |
| | | | 256GB | 004Fh |
| 16h | 2 | UC[10] | 32GB | 0031h |
| | | | 64GB | 0032h |
| | | | 128GB | 0034h |
| | | | 256GB | 0038h |
| 18h | 2 | UC[11] | 32GB | 0055h |
| | | | 64GB | 0055h |
| | | | 128GB | 0055h |
| | | | 256GB | 0055h |
| 1Ah | 2 | UC[12] | 32GB | 0032h |
| | | | 64GB | 0032h |
| | | | 128GB | 0032h |
| | | | 256GB | 0032h |

**Table 19: Product Name String Descriptor (Continued)**

| Offset | Size | Name | Value | Description |
|--------|------|--------|-------|-------------|
| 1Ch | 2 | UC[13] | 32GB | 0031h |
| | | | 64GB | 0031h |
| | | | 128GB | 0031h |
| | | | 256GB | 0031h |
| 1Eh | 2 | UC[14] | AIT | 0041h |
| | | | AAT | 0041h |
| 20h | 2 | UC[15] | AIT | 0049h |
| | | | AAT | 0041h |

Table 20: OEM ID String Descriptor

| Offset | Size | Name | Value | Description |
|--------|------|----------------|-------|-----------------------------------|
| 00h | 1 | bLength | 0Eh | Size of this descriptor |
| 01h | 1 | bDescriptorIDN | 05h | String descriptor type identifier |
| 02h | 2 | UC[0] | 004Dh | Unicode string character |
| 04h | 2 | UC[1] | 0049h | Unicode string character |
| 06h | 2 | UC[2] | 0043h | Unicode string character |
| 08h | 2 | UC[3] | 0052h | Unicode string character |
| 0Ah | 2 | UC[4] | 004Fh | Unicode string character |
| 0Ch | 2 | UC[5] | 004Eh | Unicode string character |

Table 21: Serial Number String Descriptor

| Offset | Size | Name | Value | Description |
|--------|------|----------------|-------|-----------------------------------|
| 00h | 1 | bLength | 12h | Size of this descriptor |
| 01h | 1 | bDescriptorIDN | 05h | String descriptor type identifier |
| 02h | 2 | UC[0] | – | Unicode string character |
| 04h | 2 | UC[1] | – | Unicode string character |
| 06h | 2 | UC[2] | – | Unicode string character |
| 08h | 2 | UC[3] | – | Unicode string character |
| 0Ah | 2 | UC[4] | – | Unicode string character |
| 0Ch | 2 | UC[5] | – | Unicode string character |
| 0Eh | 2 | UC[6] | – | Unicode string character |
| 10h | 2 | UC[7] | – | Unicode string character |

Table 22: Product Revision Level String Descriptor

| Offset | Size | Name | Value | Description |
|--------|------|---------|-------|-------------------------|
| 00h | 1 | bLength | 0Ah | Size of this descriptor |

**Table 22: Product Revision Level String Descriptor (Continued)**

| Offset | Size | Name | Value | Description |
|--------|------|----------------|-------|-----------------------------------|
| 01h | 1 | bDescriptorIDN | 05h | String descriptor type identifier |
| 02h | 2 | UC[0] | – | Unicode string character |
| 04h | 2 | UC[1] | – | Unicode string character |
| 06h | 2 | UC[2] | – | Unicode string character |
| 08h | 2 | UC[3] | – | Unicode string character |

Table 23: Device Health Descriptor

| Offset | Size | Name | Value | Description |
|--------|------|---------------------|-------|--|
| 00h | 1 | bLength | 2Dh | Size of this descriptor |
| 01h | 1 | bDescriptorIDN | 09h | Device health descriptor type identifier |
| 02h | 1 | bPreEOLInfo | 01h | Pre end-of-life information provides indication about device life time reflected by average reserved blocks: 01h: Normal |
| 03h | 1 | bDeviceLifeTimeEstA | 01h | This field provides an indication of the device life time based on the amount of performed PROGRAM/ERASE cycles. The calculation method is vendor specific and referred as method A. 01h: 0%–10% device life time used |
| 04h | 1 | bDeviceLifeTimeEstB | 01h | This field provides an indication of the device life time based on the amount of performed PROGRAM/ERASE cycles. The calculation method is vendor specific and referred as method B. 00h: Information not available |
| 05h | 32 | VendorPropInfo | 00h | Reserved for vendor proprietary health report |
| 25h | 4 | dRefreshTotalCount | 00h | Total refresh count: Indicate how many times the device complete refresh for the entire device. Incremented by 1 when dRefreshProgress reach 100000 (100.000%). |
| 29h | 4 | dRefreshProgress | 00h | Refresh progress: Indicate the refresh progress in percentage (%). dRefreshProgress indicates 0.000%~100.000% in dec. dRefreshProgress = 100000 (dec) when it completes 100.000%. dRefreshProgress = 1000 (dec) when it completes 1.000%. When this value reaches 100000 (100.000%) 1. Device stops refreshing even if it did not complete the number of units specified by bRefreshUnit 2. dRefreshProgress shall be reset to 0 3. dRefreshTotalCount shall be incremented by 1 When bRefreshMethod = 02h (Manual-selective), even though some of physical blocks are not refreshed by device choice, dRefreshProgress should be incremented just as much as bRefreshUnit. |

Note: 1. Micron offers proprietary solution for additional health status information.



UFS Flags, Attributes, and Commands

A flag is a single boolean value that represents 0 or 1 type of value. Flags are useful to enable or disable certain functions, modes, or states with the device.

Table 24: Flags

| IDN | Name | Type | Default Value | Description |
|-----|-----------------------|---------------------|---------------|---|
| 00h | Reserved | – | – | Reserved |
| 01h | fDeviceInit | Read/Set only | 00h | Device initialization: 0b: Device initialization completed or not started yet 1b: Device initialization in progress |
| 02h | fPermanentWPEn | Read/Write once | 00h | Permanent write protection enable: 00h: Permanent write protection disabled 01h: Permanent write protection enabled |
| 03h | fPowerOnWPEn | Read/Power on reset | 00h | Power-on write protection enable: 00h: Power-on write protection disabled 01h: Power-on write protection enabled |
| 04h | FBackgroundOpsEn | Read/Volatile | 01h | Background operations enable: 00h: Device is not permitted to run background operations 01h: Device is permitted to run background operations |
| 05h | fDeviceLifeSpanModeEn | Read/Volatile | 00h | Device life span mode: 0b: Device life span mode is disabled 1b: Device life span mode is enabled |
| 06h | fPurgeEnable | Write only/Volatile | 00h | PURGE enable: 00h: PURGE operation is disabled 01h: PURGE operation is enabled |
| 07h | fRefreshEnable | Write only/Volatile | 00h | Refresh enable 0b: REFRESH operation is disabled. 1b: REFRESH operation is enabled. This flag shall only be set when the command queue of all logical units are empty and the bRefreshStatus is 00h (idle). fRefreshEnable is automatically cleared by the UFS device when the operation completes or an error condition occurs. fRefreshEnable can be cleared by the host to interrupt an ongoing REFRESH operation |
| 08h | fPhyResourceRemoval | Read/Persistent | 00h | Physical resource removal: The host sets this flag to 1 to indicate that the dynamic capacity operation commences upon device EndPointReset or hardware reset. The device resets this flag to 0 after completion of dynamic capacity operation. The host cannot reset this flag. |
| 09h | fBusyRTC | Read only | 00h | Busy real-time clock: 00h: Device is not executing internal operation related to RTC 01h: Device is executing internal operation related to RTC |



32GB, 64GB, 128GB, 256GB: Automotive UFS Memory UFS Flags, Attributes, and Commands

Table 24: Flags (Continued)

| IDN | Name | Type | Default Value | Description |
|-----|-----------------------------|-----------------|---------------|---|
| 0Ah | Reserved | – | – | Reserved for unified memory extension standard. |
| 0Bh | fPermanentlyDisableFWUpdate | Read/Write once | 00h | Permanently disable firmware update: 00h: The UFS device firmware may be modified. 01h: The UFS device permanently disallows future firmware updates to the UFS device. |
| 0Ch | Reserved | – | – | Reserved for unified memory extension standard. |
| 0Dh | Reserved | – | – | Reserved for unified memory extension standard. |

All the flags reported in the table are device level flags. They are addressed setting INDEX = 00h and SELECTOR = 00h.

An attribute is a parameter that represents a specific range of numeric values that can be written or read. Attribute size can be from 1-bit to 32-bit. Attributes of the same type can be organized in arrays, each element of them identified by an index.

Table 25: Attributes

| IDN | Name | Type | Size (Byte) | Default Value | Description |
|-----|-------------------|-----------------|-------------|---------------|--|
| 00h | bBootLunEN | Read/Persistent | 1 | 00h | Boot LUN enable: 00h: Boot disabled 01h: Enabled boot from boot LU A 02h: Enabled boot from boot LU B All others: Reserved |
| 01h | Reserved | – | – | – | Reserved |
| 02h | bCurrentPowerMode | Read only | 1 | 11h | Current power mode: 00h: Idle mode 10h: Pre-active mode 11h: Active mode 20h: Pre-sleep mode 22h: UFS-sleep mode 30h: Pre-power down mode 33h: UFS-power down mode Others: Reserved |
| 03h | bActiveICCLevel | Read/Volatile | 1 | 00h | Active I_{CC} level: bActiveICCLevel defines the maximum current consumption allowed during active mode. 00h: Lowest active I_{CC} level 0Fh: Highest active I_{CC} level Others: Reserved |
| 04h | bOutOfOrderDataEn | Read/Write once | 1 | 00h | Out-of-order data transfer enable: 00h: Out-of-order data transfer is disabled 01h: Out-of-order data transfer is enabled Others: Reserved |



32GB, 64GB, 128GB, 256GB: Automotive UFS Memory UFS Flags, Attributes, and Commands

Table 25: Attributes (Continued)

| IDN | Name | Type | Size (Byte) | Default Value | Description |
|-----|------------------------|-----------------|-------------|---------------|---|
| 05h | bBackgroundOpStatus | Read only | 1 | 00h | Background operations status device health status for background operation: 00h: Not required 01h: Required, not critical 02h: Required, performance impact 03h: Critical Others: Reserved |
| 06h | bPurgeStatus | Read only | 1 | 00h | PURGE operation status: 00h: Idle (PURGE operation disabled) 01h: PURGE operation in progress 02h: PURGE operation stopped prematurely 03h: PURGE operation completed successfully 04h: PURGE operation failed due to logical unit queue not empty 05h: PURGE operation general failure Others: Reserved |
| 07h | bMaxDataInSize | Read/Persistent | 1 | 40h | Maximum data in size |
| 08h | bMaxDataOutSize | Read/Persistent | 1 | 40h | Maximum data out size |
| 09h | dDynCapNeeded | Read only | 4 | 00h | Dynamic capacity needed |
| 0Ah | bRefClkFreq | Read/Persistent | 1 | 01h | Reference clock frequency value: 00h: 19.2 MHz 01h: 26 MHz 02h: 38.4 MHz 03h: 52 MHz Others: Reserved |
| 0Bh | bConfigDescrLock | Read/Write once | 1 | 00h | Configuration descriptor lock: 00h: Configuration descriptor not locked 01h: Configuration descriptor locked Others: Reserved |
| 0Ch | bMaxNumOfRTT | Read/Persistent | 1 | 02h | Maximum current number of outstanding RTTs in device that is allowed. |
| 0Dh | wExceptionEventControl | Read/Volatile | 2 | 00h | Exception event control: Bit 0: DYNCAP_EVENT_EN Bit 1: SYSPOOL_EVENT_EN Bit 2: URGENT_BKOPS_EN Bit 3-15: Reserved |
| 0Eh | wExceptionEventStatus | Read only | 2 | 00h | Bit 0: DYNCAP_NEEDED Bit 1: SYSPOOL_EXHAUSTED Bit 2: URGENT_BKOPS Bit 3-15: Reserved |
| 0Fh | dSecondsPassed | Write only | 4 | 00h | Bits[31:0]: Seconds passed from TIME BASELINE |
| 10h | wContextConf | Read/Volatile | 2 | 00h | INDEX specifies the LU number. SELECTOR specifies the context ID within the LU. Valid values are 01h-Fh. |
| 11h | Obsolete | - | - | - | - |



32GB, 64GB, 128GB, 256GB: Automotive UFS Memory UFS Flags, Attributes, and Commands

Table 25: Attributes (Continued)

| IDN | Name | Type | Size (Byte) | Default Value | Description |
|-----|-----------------------------|-----------------|-------------|---------------|---|
| 12h | Reserved | — | — | — | Reserved for Unified Memory Extension standard. |
| 13h | Reserved | — | — | — | Reserved for Unified Memory Extension standard. |
| 14h | bDeviceFFUStatus | Read only | 1 | 00h | Device FFU status: 00h: No information 01h: Successful microcode update 02h: Microcode corruption error 03h: Internal error 04h: Microcode version mismatch 05h–FEh: Reserved FFh: General error |
| 15h | bPSAState | Read/Persistent | 1 | 00h | 00h: Off. PSA feature is off. 01h: Pre-soldering. PSA feature is on, device is in the pre-soldering state. 02h: Loading complete. PSA feature is on. The host will set to this value after the host finished writing data during pre-soldering state. 03h: Soldered. PSA feature is no longer available. Set by the device to indicate it is in post-soldering state. This attribute unchangeable after it is in soldered state. |
| 16h | dPSADataSize | Read/Persistent | 4 | 00h | The amount of data that the host plans to load to all logical units with bPSASensitive set to 1. |
| 18h | bDeviceCaseRough-Temperaure | Read only | 1 | 00h | Device's rough package case surface temperature. This value shall be valid when (TOO_HIGH_TEMPERATURE is supported and TOO_HIGH_TEMP_EN is enabled) or (TOO_LOW_TEMPERATURE is supported and TOO_LOW_TEMP_EN is enabled). 0: Unknown temperature 1~250: (this value - 80) degrees in Celsius (i.e., -79°C~170°C) Others: Reserved |
| 19h | bDeviceTooHighTemp-Boundar | Read only | 1 | BCh | High temperature boundary from which TOO_HIGH_TEMP in wExceptionEventStatus is turned on. 0: Unknown 100~250: (this value - 80) degrees in Celsius (i.e., 20°C~170°C) Others: Reserved |
| 1Ah | bDeviceTooLowTemp-Boundary | Read only | 1 | 2Bh | Low temperature boundary from which TOO_LOW_TEMP in wExceptionEventStatus is turned on. 0: Unknown 1~80: (this value - 80) degrees in Celsius (i.e., -79°C~0°C) Others: Reserved |



32GB, 64GB, 128GB, 256GB: Automotive UFS Memory UFS Flags, Attributes, and Commands

Table 25: Attributes (Continued)

| IDN | Name | Type | Size (Byte) | Default Value | Description |
|-----|----------------|-----------------|-------------|---------------|--|
| 1Bh | Reserved | – | – | – | – |
| ... | Reserved | – | – | – | – |
| 2Bh | Reserved | – | – | – | – |
| 2Ch | bRefreshStatus | Read only | 1 | 00h | <p>REFRESH operation status:</p> <ul style="list-style-type: none"> 00h: Idle (REFRESH operation disabled) 01h: REFRESH operation in progress 02h: REFRESH operation stopped prematurely 03h: REFRESH operation completed successfully 04h: REFRESH operation failed due to logical unit queue not empty 05h: REFRESH operation general failure Others: Reserved <p>When the bRefreshStatus is equal to the values 02h, 03h, 04h, or 05h, the bRefreshStatus is automatically cleared to 00h (idle) the first time that it is read.</p> |
| 2Dh | bRefreshFreq | Read/Persistent | 1 | 00h | <p>Refresh frequency:</p> <p>Host should make sure that dRefreshTotalCount will be incremented on this frequency.</p> <ul style="list-style-type: none"> 00h: Not defined 01h: 1 month 02h: 2 month ... FFh: 255 month. |
| 2Eh | bRefreshUnit | Read/Persistent | 1 | 00h | <p>REFRESH operation unit:</p> <p>This attribute may be set to adjust the minimum physical block numbers to be refreshed upon a single request (for example, fRefreshEnable set to 1)</p> <ul style="list-style-type: none"> 00h: Minimum refresh capability of device 01h: 100.000% (for example, entire device) Others: Reserved |



32GB, 64GB, 128GB, 256GB: Automotive UFS Memory UFS Flags, Attributes, and Commands

Table 25: Attributes (Continued)

| IDN | Name | Type | Size (Byte) | Default Value | Description |
|-----|----------------|-------------------------|-------------|---------------|---|
| 2Fh | bRefreshMethod | Read/REFRESH Persistent | 1 | 00h | <p>Refresh method: This parameter specifies the REFRESH operation method.</p> <p>00h : Not defined</p> <p>01h: Manual-force. The device is obliged to refresh the amount of physical blocks as requested by the host, regardless whether these blocks need refresh or not. The REFRESH command refreshes the amount of physical blocks given in bRefreshUnit. Refresh starts at the next physical block from where it stopped (or the first block if refresh was never triggered before).</p> <p>02h: Manual-selective. The REFRESH command refreshes the amount of physical blocks given in bRefreshUnit. Refresh starts at the next physical block from where it stopped (or the first block if refresh was never triggered before). The device only refreshes the blocks that it considers to be in need of refresh. Regardless of the actually refreshed blocks, dRefreshProgress is increased by bRefreshUnit once the REFRESH command is completed.</p> <p>Others: Reserved .</p> |

Notes: 1. dDynCapNeeded and wContextConf are arrays of attributes.
2. Default value means attribute's value after device manufacturing.

Table 26: SCSI Commands

| Command Name | Opcode | Command Name | Opcode |
|--------------------|--------|------------------------|--------|
| FORMAT UNIT | 04h | SECURITY PROTOCOL IN | A2h |
| INQUIRY | 12h | SECURITY PROTOCOL OUT | B5h |
| MODE SELECT (10) | 55h | SEND DIAGNOSTIC | 1Dh |
| MODE SENSE (10) | 5Ah | START STOP UNIT | 1Bh |
| PREFETCH (10) | 34h | SYNCHRONIZE CACHE (10) | 35h |
| PREFETCH (16) | 90h | SYNCHRONIZE CACHE (16) | 91h |
| READ (6) | 08h | TEST UNIT READY | 00h |
| READ (10) | 28h | UNMAP | 42h |
| READ (16) | 88h | VERIFY (10) | 2Fh |
| READ BUFFER | 3Ch | WRITE (6) | 0Ah |
| READ CAPACITY (10) | 25h | WRITE (10) | 2Ah |
| READ CAPACITY(16) | 9Eh | WRITE (16) | 8Ah |
| REPORT LUNS | A0h | WRITE BUFFER | 3Bh |
| REQUEST SENSE | 03h | – | – |



UFS Supported Pages

Micron devices support the following UFS mode pages. For detailed information, refer to the JEDEC UFS specification.

Table 27: UFS Supported Pages

| Page Name | Page Code | Subpage Code | Description |
|---------------------------|-----------|--------------|--|
| Control | 0Ah | 00h | Return control mode page |
| Read-write error recovery | 01h | 00h | Return read-write error recovery mode page |
| Caching | 08h | 00h | Return caching mode page |
| All pages | 3Fh | 00h | Return all mode pages (not including subpages) |
| All subpages | 3Fh | FFh | Return all mode pages and subpages |

Table 28: Control Mode Page

| Offset | Bit | Field | Default Value | Description |
|--------|-----|-------------|---------------|--|
| 00h | 5:0 | PAGE CODE | 0Ah | Indicates the format and parameters for particular mode page. |
| 00h | 6 | SPF | 0h | Indicates SUBPAGE format. |
| 00h | 7 | PS | 01h | Indicates the page parameters can be saved. |
| 01h | 7:0 | PAGE LENGTH | 0Ah | Indicates the size in bytes of the following mode page parameters. |
| 02h | 0 | RLEC | 0h | Report log exception condition. Setting this bit to 0 specifies that the device server shall not report log exception conditions. |
| 02h | 1 | GLTSD | 0h | Global logging target save disable (GLTSD): Setting this bit to 0 specifies that the logical unit implicitly saves, at vendor specific intervals, each log parameter in which the TSD bit is set to 0. |
| 02h | 2 | D_SENSE | 0h | A descriptor format sense data (D_SENSE) bit set to 0 specifies that the device server shall return fixed format sense data when returning sense data in the same I_T_L_Q nexus transaction as the status. |
| 02h | 3 | DPICZ | 0h | A disable protection information check if protect field is 0 (DPICZ) bit set to 0 indicates that checking of protection information bytes is enabled. |
| 02h | 4 | TMF_ONLY | 0h | The allow task management functions only (TMF_ONLY) bit set to 0 specifies that the device server shall process commands with the auto contingent allegiance (ACA) task attribute received on the faulted I_T nexus when an ACA condition has been established. |
| 02h | 7:5 | TST | 0h | Indicates task set type (TST). |
| 03h | 0 | Obsolete | 0h | Not available |
| 03h | 2:1 | QERR | 0h | The queue error management (QERR) field specifies how the device server shall handle other commands when one command is terminated with check condition status. If an ACA condition is established, the affected commands in the task set shall resume after the ACA condition is cleared. Otherwise, all commands other than the command that received the check condition status shall be processed as if no error occurred. |
| 03h | 3 | NUAR | 0h | No unit attention on release (NUAR) bit set to 0 specifies that the device server shall establish a unit attention condition. |

**Table 28: Control Mode Page (Continued)**

| Offset | Bit | Field | Default Value | Description |
|--------|------|------------------------------------|---------------|--|
| 03h | 7:4 | QUEUE ALGORITHM MODIFIER | 01h | A value of 1 in this field specifies that the device server may reorder the processing sequence of commands having the SIMPLE task attribute in any manner. |
| 04h | 2:0 | Obsolete | 0h | Not available |
| 04h | 3 | SWP | 0h | A software write protect (SWP) bit (user configurable) |
| 04h | 5:4 | UA_INTLCK_CTRL | 0h | The unit attention interlocks control (UA_INTLCK_CTRL) field set to 00b specifies that the logical unit shall clear any unit attention condition reported in the same I_T_L_Q nexus transaction as a check condition status and shall not establish a unit attention condition when a command is completed with busy, task set full, or reservation conflict status. |
| 04h | 6 | RAC | 0h | A report a check (RAC) bit set to 0 specifies that the device server may return busy status regardless of the length of time the reason for returning busy status may persist. |
| 04h | 7 | VS | 0h | Not available |
| 05h | 2:0 | AUTOLOAD MODE | 0h | This field specifies the action to be taken by a removable medium device server when a medium is inserted. Setting it to 0 means that medium shall be loaded for full access. |
| 05h | 3 | Reserved | – | – |
| 05h | 4 | RWWP | 0h | A reject write without protection (RWWP) bit set to 0 specifies that WRITE commands without protection information shall be processed. |
| 05h | 5 | ATMPE | 0h | An application tag mode page enabled (ATMPE) bit set to 0 specifies that the application tag mode page is disabled and the contents of logical block application tags are not defined by this standard. |
| 05h | 6 | TAS | 0h | A task aborted status (TAS) bit set to 0 specifies that aborted commands shall be terminated by the device server without any response to the application client. |
| 05h | 7 | ATO | 0h | An application tag owner (ATO) bit set to 0 specifies that the device server may modify the contents of the LOGICAL BLOCK APPLICATION TAG field and, depending on the protection type, may modify the contents of the LOGICAL BLOCK REFERENCE TAG field. |
| 06h | 15:0 | Obsolete | 0h | Not available |
| 08h | 15:0 | BUSY TIMEOUT PERIOD | 01h | Busy timeout period: 0001h = 100ms |
| 0Ah | 15:0 | EXTENDED SELF-TEST COMPLETION TIME | 0h | This field contains advisory data that is the time in seconds that the device server requires to complete an extended self-test when the device server is not interrupted by subsequent commands and no errors occur during processing of the self-test. |



Notes: 1. Some fields are user configurable.

Table 29: Read – Write Error Recovery Mode Page

| Offset | Bit | Field | Default Value | Description |
|--------|-----|----------------------|---------------|---|
| 00h | 5:0 | PAGE CODE | 01h | Indicates the format and parameters for particular mode page. |
| 00h | 6 | SPF | 0h | Indicates SUBPAGE format. |
| 00h | 7 | PS | 01h | Indicates the page parameters can be saved. |
| 01h | 7:0 | PAGE LENGTH | 0Ah | Indicates the size in bytes of the following mode page parameters. |
| 02h | 0 | DCR | 0h | A disable correction (DCR) bit set to 0 allows the use of additional information (for example, ECC bytes) for data error recovery. If the EER bit is set to 1, the DCR bit shall be set to 0. |
| 02h | 1 | DTE | 0h | A data terminate on error (DTE) bit set to 0 specifies that the device server shall not terminate the data-in or data-out buffer transfer of a command performing a READ or WRITE operation upon detection of a recovered error. |
| 02h | 2 | PER | 0h | A post error (PER) bit set to 0 specifies that if a recovered read error occurs during a command performing a READ or WRITE operation, then the device server shall perform error recovery procedures within the limits established by the error recovery parameters and only terminate the command with check condition status if the error becomes uncorrectable based on the established limits. If the DTE bit is set to 1, then the PER bit shall be set to 1. |
| 02h | 3 | EER | 0h | An enable early recovery (EER) bit set to 0 specifies that the device server shall use an error recovery procedure that minimizes the risk of error mis-detection or mis-correction. |
| 02h | 4 | RC | 0h | A read continuous (RC) bit set to 0 specifies that ERROR RECOVERY operations that cause delays during the data transfer are acceptable. Data shall not be fabricated. |
| 02h | 5 | TB | 0h | A transfer block (TB) bit set to 0 specifies that if an unrecovered read error occurs during a READ operation, then the device server shall not transfer any data for the logical block to the data-in buffer. |
| 02h | 6 | ARRE | 0h | An automatic read reassignment enabled (ARRE) bit set to 0 specifies that the device server shall not perform automatic reassignment of defective logical blocks during READ operations. |
| 02h | 7 | AWRE | 01h | An automatic write reassignment enabled (AWRE) bit set to 1 specifies that the device server shall enable automatic reassignment of defective logical blocks during WRITE operations. |
| 03h | 7:0 | READ RETRY COUNT | 01h | This field (user configurable) specifies the number of times that the device server shall attempt its recovery algorithm during READ operations. |
| 04h | 7:0 | Obsolete | 0h | Not available |
| 05h | 7:0 | Obsolete | 0h | Not available |
| 06h | 7:0 | Obsolete | 0h | Not available |
| 07h | 1:0 | Restricted for MMC-6 | 0h | Not available |
| 07h | 6:2 | Reserved | – | – |
| 07h | 7 | TPERE | 0h | Not available |

**Table 29: Read – Write Error Recovery Mode Page**

| Offset | Bit | Field | Default Value | Description |
|--------|------|---------------------|---------------|--|
| 08h | 7:0 | WRITE RETRY COUNT | 00h | This field (user configurable) specifies the number of times that the device server shall attempt its recovery algorithm during WRITE operations. |
| 09h | 7:0 | Reserved | – | – |
| 0Ah | 15:0 | RECOVERY TIME LIMIT | 4B0h | This field (user configurable) specifies in milliseconds the maximum time duration that the device server shall use for data error recovery procedures. When both a retry count and a recovery time limit are specified, the field that specifies the recovery action of least duration shall have priority. |

Table 30: Caching Mode Page

| Offset | Bit | Field | Default Value | Description |
|--------|-----|-------------|---------------|--|
| 00h | 5:0 | PAGE CODE | 08h | Indicates the format and parameters for particular mode page. |
| 00h | 6 | SPF | 0h | Indicates SUBPAGE format. |
| 00h | 7 | PS | 01h | Indicates the page parameters can be saved. |
| 01h | 7:0 | PAGE LENGTH | 12h | Indicates the size in bytes of the following mode page parameters. |
| 02h | 0 | RCD | 0h | A read cache disable (RCD) bit (user configurable) set to 0 specifies that the device server may return data requested by a READ command by accessing either the cache or medium. A RCD bit set to 1 specifies that the device server shall transfer all of the data requested by a READ command from the medium (for example, data shall not be transferred from the cache). |
| 02h | 1 | MF | 0h | A multiplication factor (MF) bit set to 0 specifies that the device server shall interpret the MINIMUM PREFETCH field and the MAXIMUM PREFETCH field in terms of the number of logical blocks for each of the respective types of prefetch. |
| 02h | 2 | WCE | 01h | A write back cache enable (WCE) bit (user configurable) set to 0 specifies that the device server shall complete a WRITE command with good status only after writing all of the data to the medium without error. A WCE bit set to 1 specifies that the device server may complete a WRITE command with good status after receiving the data without error and prior to having written the data to the medium. |
| 02h | 3 | SIZE | 0h | A size enable (SIZE) bit set to 0 specifies that the NUMBER OF CACHE SEGMENTS field is used to control caching segmentation. Simultaneous use of both the number of segments and the segment size is vendor specific. |
| 02h | 4 | DISC | 0h | A discontinuity (DISC) bit set to 0 specifies that prefetches be truncated or wrapped at time discontinuities. |
| 02h | 5 | CAP | 0h | A caching analysis permitted (CAP) bit set to 0 specifies that caching analysis is disabled (for example, to reduce overhead time or to prevent non-pertinent operations from impacting tuning values). |
| 02h | 6 | ABPF | 0h | An abort prefetch (ABPF) bit set to 0 when the DRA bit set to 0 specifies that the termination of any active prefetch is dependent upon caching mode page bytes 4 through 11 and is vendor specific. |

**Table 30: Caching Mode Page (Continued)**

| Offset | Bit | Field | Default Value | Description |
|--------|------|----------------------------------|---------------|---|
| 02h | 7 | IC | 0h | An initiator control (IC) enable bit set to 0 specifies that the device server uses its own adaptive caching algorithm. |
| 03h | 3:0 | WRITE RETENTION PRIORITY | 0h | This field set to 0h means that the device server should not distinguish between retaining the indicated data and data placed into the cache by other means (for example, prefetch). |
| 03h | 7:4 | DEMAND READ RETENTION PRIORITY | 0h | This field set to 0 means that the device server should not distinguish between retaining the indicated data and data placed into the cache by other means (for example, prefetch). |
| 04h | 15:0 | DISABLE PREFETCH TRANSFER LENGTH | 0h | This field specifies the selective disabling of anticipatory prefetch on long transfer lengths. If this field is set to 0, then all anticipatory prefetching is disabled for any request for data, including those with a transfer length of 0. |
| 06h | 15:0 | MINIMUM PREFETCH | 0h | This field specifies the number of logical blocks to prefetch regardless of the delays it might cause in processing subsequent commands. If MF bit is set to 0, this field contains the number of logical blocks. |
| 08h | 15:0 | MAXIMUM PREFETCH | 0h | This field specifies the number of logical blocks to prefetch if the prefetch does not delay processing of subsequent commands. If MF bit is set to 0, this field contains the number of logical blocks. |
| 0Ah | 15:0 | MAXIMUM PREFETCH CEILING | 0h | This field specifies an upper limit on the number of logical blocks computed as the maximum prefetch. If this number of logical blocks is greater than the value in the MAXIMUM PREFETCH field, then the number of logical blocks to prefetch shall be truncated to the value stored in this field. |
| 0Ch | 0 | NV_DIS | 0h | An NV_DIS bit set to 0 specifies that the device server may use a nonvolatile cache and indicates that a nonvolatile cache may be present and enabled. |
| 0Ch | 2:1 | Reserved | – | – |
| 0Ch | 4:3 | Vendor specific | 0h | Vendor specific |
| 0Ch | 5 | DRA | 0h | A disable read-ahead (DRA) bit set to 0 specifies that the device server may continue to read logical blocks into the prefetch buffer beyond the addressed logical block(s). |
| 0Ch | 6 | LBCSS | 0h | A logical block cache segment size (LBCSS) bit set to 0 specifies that the CACHE SEGMENT SIZE field units shall be interpreted as bytes. The LBCSS shall not impact the units of other fields. |
| 0Ch | 7 | FSW | 0h | A force sequential write (FSW) bit set to 0 specifies that the device server may reorder the sequence of writing logical blocks (for example, in order to achieve faster command completion). |
| 0Dh | 7:0 | NUMBER OF CACHE SEGMENTS | 0h | This field specifies the number of segments into which the device server shall divide the cache. |
| 0Eh | 15:0 | CACHE SEGMENT SIZE | 0h | This field specifies the segment size in bytes if the LBCSS bit is set to 0 or in logical blocks if the LBCSS bit is set to 1. This field is valid only when the SIZE bit is set to 1. |
| 10h | 7:0 | Reserved | – | – |
| 11h | 15:0 | Obsolete | 0h | Not available |



32GB, 64GB, 128GB, 256GB: Automotive UFS Memory UFS Supported Pages

Notes: 1. Some fields are user configurable.



UFS Vital Product Data Parameters

The vital product data (VPD) pages are returned by an INQUIRY command with the EVPD bit set to 1 and contain vendor specific product information about a logical unit and SCSI target device. A UFS device supports the following VPD pages.

Table 31: Supported VPD Pages

| Offset | Bit | Field | Default Value | Description |
|--------|------|----------------------------|---------------|--|
| 00h | 4:0 | PERIPHERAL DEVICE TYPE | 1Eh | This bit set to 1 means device server is a direct access block device. 1Eh: Well known logical unit |
| 00h | 7:5 | PERIPHERAL QUALIFIER | 0h | A peripheral device having the specified peripheral device type is connected to this logical unit. If the device server is unable to determine whether or not a peripheral device is connected, it also shall use this peripheral qualifier. This peripheral qualifier does not mean that the peripheral device connected to the logical unit is ready for access. |
| 01h | 7:0 | PAGE CODE | 0h | This field identifies the VPD page and contains the same value as in this field in the INQUIRY CDB. |
| 02h | 15:0 | PAGE LENGTH | 07h | This field indicates the length in bytes of the VPD parameters that follow this field. |
| 04h | 7:0 | Supported VPD Page List[0] | 0h | The supported VPD page list contains a list of all VPD page codes implemented by the logical unit in ascending order beginning with page code 00h: SUPPORTED_VPD_PAGE |
| 05h | 7:0 | Supported VPD Page List[1] | 80h | UNIT_SERIAL_NUM |
| 06h | 7:0 | Supported VPD Page List[2] | 83h | DEVICE_ID |
| 07h | 7:0 | Supported VPD Page List[3] | 87h | MODE_PAGE_POLICY |
| 08h | 7:0 | Supported VPD Page List[4] | B0h | BLOCK_LIMITS |
| 09h | 7:0 | Supported VPD Page List[5] | B1h | BLOCK_DEVICE_CHARACTERISTICS |
| 0Ah | 7:0 | Supported VPD Page List[6] | B2h | LOGICAL_BLOCK_PROVISIONING |

Table 32: Unit Serial Number VPD Page

| Offset | Bit | Field | Default Value | Description |
|--------|-----|------------------------|---------------|--|
| 00h | 4:0 | PERIPHERAL DEVICE TYPE | 1Eh | This bit set to 1 means device server is a direct access block device. 1Eh: Well known logical unit |
| 00h | 7:5 | PERIPHERAL QUALIFIER | 0h | A peripheral device having the specified peripheral device type is connected to this logical unit. If the device server is unable to determine whether or not a peripheral device is connected, it also shall use this peripheral qualifier. This peripheral qualifier does not mean that the peripheral device connected to the logical unit is ready for access. |

**Table 32: Unit Serial Number VPD Page (Continued)**

| Offset | Bit | Field | Default Value | Description |
|--------|------|-----------------------|---------------|---|
| 01h | 7:0 | PAGE CODE | 80h | This field identifies the VPD page and contains the same value as in this field in the INQUIRY CDB. |
| 02h | 15:0 | PAGE LENGTH | 4h | This field indicates the length in bytes of the VPD parameters that follow this field. |
| 04h | 7:0 | PRODUCT SERIAL NUMBER | – | This field contains right-aligned ASCII data that is vendor-assigned serial number. |

Table 33: Device Identification VPD Page

| Offset | Bit | Field | Default Value | Description |
|--------|------|--------------------------------------|---------------|--|
| 00h | 4:0 | PERIPHERAL DEVICE TYPE | 1Eh | This bit set to 1 means device server is a direct access block device. 1Eh: Well known logical unit |
| 00h | 7:5 | PERIPHERAL QUALIFIER | 0h | A peripheral device having the specified peripheral device type is connected to this logical unit. If the device server is unable to determine whether or not a peripheral device is connected, it also shall use this peripheral qualifier. This peripheral qualifier does not mean that the peripheral device connected to the logical unit is ready for access. |
| 01h | 7:0 | PAGE CODE | 83h | This field identifies the VPD page and contains the same value as in this field in the INQUIRY CDB. |
| 02h | 15:0 | PAGE LENGTH | Ch | This field indicates the length in bytes of the VPD parameters that follow this field. |
| 04h | 4:0 | CODE SET | 2h | This field contains a code set enumeration that indicates the format of the DESIGNATOR field. |
| 04h | 7:5 | PROTOCOL IDENTIFIER | 0h | This field may indicate the SCSI transport protocol to which the designation descriptor applies. |
| 05h | 3:0 | DESIGNATOR TYPE | 1h | This field indicates the format and assignment authority for the designator. |
| 05h | 5:4 | ASSOCIATION | 0h | This field indicates the entity with which the DESIGNATOR field is associated. If a logical unit returns a designation descriptor with this field set to 00b or 10b, it shall return the same descriptor when it is accessed through any other I_T nexus. |
| 05h | 6 | Reserved | – | – |
| 05h | 7 | PIV | 0h | A protocol identifier valid (PIV) bit set to 0 indicates the PROTOCOL IDENTIFIER field contents are reserved. |
| 06h | 7:0 | Reserved | – | – |
| 07h | 7:0 | DESIGNATOR LENGTH | 8h | This field indicates the length in bytes of the DESIGNATOR field. |
| 08h | 23:0 | IEEE COMPANY ID | – | – |
| 0Bh | 39:0 | VENDOR SPECIFIC EXTENSION IDENTIFIER | – | – |

**Table 34: Mode Page Policy VPD Page**

| Offset | Bit | Field | Default Value | Description |
|---------------------------------|------|------------------------|---|--|
| 00h | 4:0 | PERIPHERAL DEVICE TYPE | 1Eh | This bit set to 1 means device server is a direct access block device 1Eh: Well known logical unit |
| 00h | 7:5 | PERIPHERAL QUALIFIER | 0h | A peripheral device having the specified peripheral device type is connected to this logical unit. If the device server is unable to determine whether or not a peripheral device is connected, it also shall use this peripheral qualifier. This peripheral qualifier does not mean that the peripheral device connected to the logical unit is ready for access. |
| 01h | 7:0 | PAGE CODE | 87h | This field identifies the VPD page and contains the same value as in this field in the INQUIRY CDB. |
| 02h | 15:0 | PAGE LENGTH | 0Ch | This field indicates the length in bytes of the VPD parameters that follow this field. |
| Mode page policy descriptor [0] | | | Contains information describing the mode page policy for read-write error recovery mode page. | |
| 04h | 5:0 | Policy page code | 1h | |
| 04h | 7:6 | Reserved1 | 0h | |
| 05h | 7:0 | Policy subpage code | 0h | |
| 06h | 1:0 | ModePagePolicy | 0h | |
| 06h | 6:2 | Reserved 2 | 0h | |
| 06h | 7 | MLUS | 1h | |
| 07h | 7:0 | Reserved 3 | 0h | |
| Mode page policy descriptor [1] | | | Contains information describing the mode page policy for caching mode page. | |
| 08h | 5:0 | Policy page code | 8h | |
| 08h | 7:6 | Reserved1 | 0h | |
| 09h | 7:0 | Policy subpage code | 0h | |
| 0Ah | 1:0 | Mode page policy | 0h | |
| 0Ah | 6:2 | Reserved 2 | 0h | |
| 0Ah | 7 | MLUS | 01h | |
| 0Bh | 7:0 | Reserved 3 | 0h | |
| Mode page policy descriptor [2] | | | Contains information describing the mode page policy for control mode page. | |
| 0Ch | 5:0 | Policy page code | Ah | |
| 0Ch | 7:6 | Reserved 1 | 0h | |
| 0Dh | 7:0 | Policy subpage code | 0h | |
| 0Eh | 1:0 | ModePagePolicy | 0h | |
| 0Eh | 6:2 | Reserved 2 | 0h | |
| 0Eh | 7 | MLUS | 0h | |
| 0Fh | 7:0 | Reserved 3 | 0h | |

**Table 35: Block Limits VPD Page**

| Offset | Bit | Field | Default Value | Description |
|--------|------|---|---------------|---|
| 00h | 4:0 | PERIPHERAL DEVICE TYPE | 1Eh | This bit set to 1 means device server is a direct access block device. 1Eh: Well known logical unit |
| 00h | 7:5 | PERIPHERAL QUALIFIER | 0h | A peripheral device having the specified peripheral device type is connected to this logical unit. If the device server is unable to determine whether or not a peripheral device is connected, it also shall use this peripheral qualifier. This peripheral qualifier does not mean that the peripheral device connected to the logical unit is ready for access. |
| 01h | 7:0 | PAGE CODE | B0h | This field identifies the VPD page and contains the same value as in this field in the INQUIRY CDB. |
| 02h | 15:0 | PAGE LENGTH | 3Ch | This field indicates the length in bytes of the VPD parameters that follow this field. |
| 04h | 7:0 | Reserved | – | – |
| 05h | 7:0 | MAXIMUM COMPARE AND WRITE LENGTH | 0h | This field is set to 0, if the device server does not support this command. |
| 06h | 15:0 | OPTIMAL TRANSFER LENGTH GRANULARITY | 20h | This field indicates the optimal transfer length granularity in blocks for a single ORWRITE command, PREFETCH command, READ command, VERIFY command, WRITE command, WRITE AND VERIFY command, XDREAD command, XDWRITE command, XDWRITEREAD command, or XPWRITE command. |
| 08h | 31:0 | MAXIMUM TRANSFER LENGTH | 0h | This field indicates the maximum transfer length in blocks that the device server accepts for a single ORWRITE command, READ command, VERIFY command, WRITE command, WRITE AND VERIFY command, XDWRITEREAD command, or XPWRITE command. |
| 0Ch | 31:0 | OPTIMAL TRANSFER LENGTH | 20h | This field indicates the optimal transfer length in blocks for a single ORWRITE command, PREFETCH command, READ command, VERIFY command, WRITE command, WRITE AND VERIFY command, XDREAD command, XDWRITE command, XDWRITEREAD command, or XPWRITE command. |
| 10h | 31:0 | MAXIMUM PREFETCH XDREAD XDWRITE TRANSFER LENGTH | 100h | This field indicates: a) the maximum transfer length in blocks that the device server accepts for a single PREFETCH command b) if the XOR control mode page is implemented, then the maximum value supported by the MAXIMUM XOR WRITE SIZE field in the XOR control mode page. c) if the XOR control mode page is not implemented, then the maximum transfer length in blocks that the device server accepts for a single XDWRITE command or XDREAD command. The device server should set this field to less than or equal to the MAXIMUM TRANSFER LENGTH field. |

**Table 35: Block Limits VPD Page (Continued)**

| Offset | Bit | Field | Default Value | Description |
|--------|------|--------------------------------------|---------------|---|
| 14h | 31:0 | MAXIMUM UNMAP LBA COUNT | FFFFFFFh | <p>This field indicates the maximum number of LBAs that may be unmapped by an UNMAP command.</p> <p>If the number of LBAs that may be unmapped by an UNMAP command is constrained only by the amount of data that may be contained in the UNMAP parameter list, then the device server shall set this field to FFFF_FFFFh.</p> <p>If the device server implements the UNMAP command, then the value in this field shall be greater than or equal to 1.</p> |
| 18h | 31:0 | MAXIMUM UNMAP BLOCK DESCRIPTOR COUNT | 10h | <p>This field indicates the maximum number of unmap block descriptors that shall be contained in the parameter data transferred to the device server for an UNMAP command.</p> <p>If there is no limit on the number of unmap block descriptors contained in the parameter data, then the device server shall set this field to FFFF_FFFFh.</p> <p>If the device server implements the UNMAP command, then the value in this field shall be greater than or equal to 1.</p> |
| 1Ch | 31:0 | OPTIMAL UNMAP GRANULARITY | 1h | <p>This field indicates the optimal granularity in logical blocks for unmap requests. An unmap request with a number of logical blocks that is not a multiple of this value may result in UNMAP operations on fewer LBAs than requested.</p> <p>If this field is set to 0000_0000h, then the optimal unmap granularity is not specified.</p> |
| 20h | 30:0 | UNMAP GRANULARITY ALIGNMENT | 0h | <p>This field indicates the LBA of the first logical block to which the OPTIMAL UNMAP GRANULARITY field applies.</p> <p>The unmap granularity alignment is used to calculate an optimal unmap request starting LBA as follows:</p> $\text{Optimal unmap request starting LBA} = (n \times \text{OPTIMAL UNMAP GRANULARITY}) + \text{UNMAP GRANULARITY ALIGNMENT}$ <p>Where n is 0 or any positive integer value.</p> |
| 20h | 31 | UGAVALID | 0h | An unmap granularity alignment valid (UGAVALID) bit set to 0 indicates that the UNMAP GRANULARITY ALIGNMENT field is not valid. |

Table 36: Block Device Characteristics

| Offset | Bit | Field | Default Value | Description |
|--------|------|------------------------|---------------|--|
| 00h | 4:0 | PERIPHERAL DEVICE TYPE | 1Eh | This bit set to 1 means device server is a direct access block device. 1Eh: Well known logical unit |
| 00h | 7:5 | PERIPHERAL QUALIFIER | 000h | A peripheral device having the specified peripheral device type is connected to this logical unit. If the device server is unable to determine whether or not a peripheral device is connected, it also shall use this peripheral qualifier. This peripheral qualifier does not mean that the peripheral device connected to the logical unit is ready for access. |
| 01h | 7:0 | PAGE CODE | B1h | This field identifies the VPD page and contains the same value as in the PAGE CODE field in the INQUIRY CDB. |
| 02h | 15:0 | PAGE LENGTH | 3Ch | This field indicates the length in bytes of the VPD parameters that follow this field. |

**Table 36: Block Device Characteristics (Continued)**

| Offset | Bit | Field | Default Value | Description |
|--------|------|----------------------|---------------|---|
| 04h | 15:0 | MEDIUM ROTATION RATE | 0001h | 0001h means device is a non-rotating medium (for example, solid state). |
| 06h | 7:0 | Reserved | — | — |
| 07h | 3:0 | NOMINAL FORM FACTOR | 05h | This field indicates the nominal form factor of the device containing the logical unit. |
| 07h | 7:4 | Reserved | — | — |

Table 37: Logical Block Provisioning

| Offset | Bit | Field | Default Value | Description |
|--------|------|------------------------|---------------|--|
| 00h | 4:0 | PERIPHERAL DEVICE TYPE | 1Eh | This bit set to 1 means device server is a direct access block device. 1Eh: Well known logical unit |
| 00h | 7:5 | PERIPHERAL QUALIFIER | 000h | A peripheral device having the specified peripheral device type is connected to this logical unit. If the device server is unable to determine whether or not a peripheral device is connected, it also shall use this peripheral qualifier. This peripheral qualifier does not mean that the peripheral device connected to the logical unit is ready for access. |
| 01h | 7:0 | PAGE CODE | B2h | This fields identifies the VPD page and contains the same value as in the PAGE CODE field in the INQUIRY CDB. |
| 02h | 15:0 | PAGE LENGTH | 04h | This field indicates the length in bytes of the VPD parameters that follow this field. |
| 04h | 7:0 | THRESHOLD EXPONENT | 16h | This field indicates the threshold set size in LBAs as a power of 2. |
| 05h | 0 | DP | 00h | A descriptor present (DP) bit set to 0 indicates that a PROVISIONING GROUP DESCRIPTOR is not present. |
| 05h | 1 | ANC_SUP | 00h | This bit set to 0 indicates that the device server does not support anchored LBAs. |
| 05h | 5:2 | Reserved | — | — |
| 05h | 6 | TBPWS | 00h | This bit set to 0 indicates that the device server does not support the use of the WRITE SAME (16) command to unmap LBAs. |
| 05h | 7 | TPU | 01h | This bit set to 1 indicates that the device server supports the UNMAP command. |
| 06h | 7:0 | Reserved | — | — |
| 07h | 7:0 | Reserved | — | — |

When the EVPD bit is set to 0 and page code = 0, the standard INQUIRY DATA is responded to INQUIRY command. The standard INQUIRY DATA format is shown in the table below:

Table 38: Standard Inquiry Data

| Offset | Bit | Field | Default Value | Description |
|--------|-----|------------------------|---------------|---|
| 00h | 4:0 | PERIPHERAL DEVICE TYPE | 1Eh | This bit set to 1 means device server is a direct access block device. 1Eh: Well known logical unit |



32GB, 64GB, 128GB, 256GB: Automotive UFS Memory UFS Vital Product Data Parameters

Table 38: Standard Inquiry Data (Continued)

| Offset | Bit | Field | Default Value | Description |
|--------|------|------------------------|---------------|--|
| 00h | 7:5 | PERIPHERAL QUALIFIER | 0h | A peripheral device having the specified peripheral device type is connected to this logical unit. If the device server is unable to determine whether or not a peripheral device is connected, it also shall use this peripheral qualifier. This peripheral qualifier does not mean that the peripheral device connected to the logical unit is ready for access. |
| 01h | 6:0 | Reserved | — | — |
| 01h | 7 | RMB | 0h | A removable medium (RMB) bit set to 0 indicates that the medium is not removable. |
| 02h | 7:0 | VERSION | 6h | This field indicates the implemented version of this standard. This field set to 06h means the conformance to SPC. |
| 03h | 3:0 | RESPONSE DATA FORMAT | 2h | This field value of two indicates that the data shall be in the format defined in SPC. |
| 03h | 7:4 | NA1 | 0h | Not available in UFS standard |
| 04h | 7:0 | ADDITIONAL LENGTH | 1Fh | This field indicates the length in bytes of the remaining standard INQUIRY data. |
| 05h | 7:0 | NA2 | 0h | Not available in UFS standard |
| 06h | 7:0 | NA3 | 0h | Not available in UFS standard |
| 07h | 0 | NA4 | 0h | Not available in UFS standard |
| 07h | 1 | CMDQUE | 1h | This bit is set to 1 indicating that the logical unit supports the command management model (SAM). |
| 07h | 7:2 | NA5 | 0h | Not available in UFS standard |
| 08h | 15:0 | VENDOR IDENTIFICATION | — | This field contains left-aligned ASCII data identifying the vendor of the product. |
| 10h | 15:0 | PRODUCT IDENTIFICATION | — | This field contains left-aligned ASCII data defined by the vendor. |
| 20h | 15:0 | PRODUCT REVISION LEVEL | — | This field contains left-aligned ASCII data defined by the vendor. |



Electrical Specifications

According to JEDEC UFS v2.1 specification, power-up timing starts when the supply voltage crosses 300mV and ends when it reaches the minimum operating value. Micron device only supports V_{CC} and V_{CCQ2} . V_{CCQ} is not used.

Table 39: Power Supply Parameters

| Parameter | Symbol | Min | Max | Unit |
|---------------------------------|------------|-----|------|------|
| V_{CC} operating range | V_{CC} | 2.7 | 3.6 | V |
| V_{CCQ} operating range | V_{CCQ} | – | – | – |
| V_{CCQ2} operating range | V_{CCQ2} | 1.7 | 1.95 | V |
| Supply power-up timing for 3.3V | t_{PRUH} | – | 35 | ms |
| Supply power-up timing for 1.8V | t_{PRUL} | – | 25 | ms |
| Supply power-up timing for 1.2V | t_{PRUV} | – | – | – |

Table 40: Reference Clock Parameters¹

| Parameter | Symbol | Min | Max | Units |
|------------------------------|----------------------|--------------------------|------|------------|
| Frequency | f_{ref} | 19.2 26 38.4 52 | | MHz |
| Frequency error | f_{ERROR} | –150 | +150 | ppm |
| Clock rise time ¹ | t_{IRISE} | – | 2 | ns |
| Clock fall time | t_{IFALL} | – | 2 | ns |
| Duty cycle | t_{DC} | 45 | 55 | % |
| Phase noise | N | – | –66 | dBc |
| Noise floor density | N _{density} | – | –140 | dBc/Hz |
| Input impedance | RL_{RX} | 100 | – | k Ω |
| | CL_{RX} | – | 5 | pF |

Notes: 1. V_{IL} parameter is 0.2V on RST_n and REF_CLK signals.



Revision History

Rev. E – 04/2022

- Fixed typo

Rev. D – 03/2022

- Added Functional Safety information

Rev. C – 01/2021

- Updated Legal Status to Production
- Added Note to Device Descriptor Table
- Updated RPMB Unit Descriptor Table
- Added Note to Active Current Consumption and Low Power-Mode Tables

Rev. B – 11/2020

- Updated Ordering Information table (removed ES from MPNs)
- Updated Device Descriptor table in UFS Descriptors section
- Updated RPMB Unit Descriptor table in UFS Descriptors section
- Updated Product Name String Descriptor table in UFS Descriptors section
- Updated Mode Page Policy VPD Page table in UFS Vital Product Data Parameters section
- Updated Block Limits VPD Page table in UFS Vital Product Data Parameters section

Rev. A – 05/2020

- Initial release