

CHIPLINK P-Channel Enhancement Mode Power MOSFET

Description

The LX2301S combines advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltage as low as 1.8V. This device is suitable for use as a load switch or other general applications.

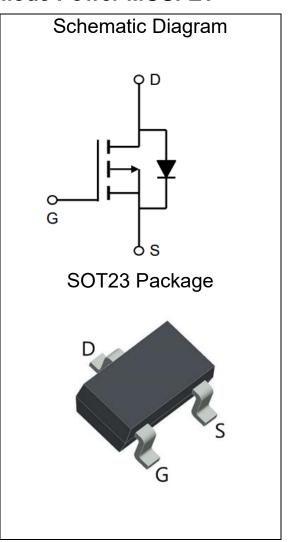
Features

- V_{DS} = -20V, I_{D} = -1.5A $R_{DS(ON)}$ <160mΩ@VDS=-4.5V $R_{DS(ON)}$ <230mΩ@VDS=-2.5V
- Low gate charge
- High power and current handing capability
- Termination is Lead-free and RoHS Compliant



Applications

- PWM applications
- Load switch
- Power Management



Maximum Ratings(T_A=25 °C unless otherwise noted)

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V _{DS}	-20	V
Gate-Source Voltage	V _{GS}	±10	V
Continuous Drain Current	I _D	-1.5	Α
Pulsed Drain Current ^B	I _{DM}	-6	Α
Maximum Power Dissipation ^A	P _D	0.7	W
Junction and Storage Temperature Range	T _J , T _{STG}	-55 To 150	$^{\circ}$ C

Thermal Characteristic

Thermal Resistance, Junction to Ambient	R _{QJA}	178	°C/W
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Electrical Characteristics (T_A =25 $^{\circ}$ Cunless otherwise specified)

Parameter	Symbol	Test conditions	MIN	TYP	MAX	UNIT
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250uA	-20			V
Gate-Threshold Voltage	$V_{th(GS)}$	V_{DS} = V_{GS} , I_{D} =-250 uA	-0.4	-0.7	-1	V
Gate-body Leakage	IGSS	$V_{DS}=0V$, $V_{GS}=\pm10V$			±100	nA
Zero Gate Voltage Drain Current	IDSS	V _{DS} =-20V, V _{GS} =0V			-1	uA
Drain-Source On-Resistance	Dag (au)	V_{GS} =-4.5V, I_{D} =-1.5A		130	160	mΩ
Dialii-Source Ori-Nesistance	R _{DS(ON)}	V_{GS} =-2.5V, I_{D} =-1A		180	230	mΩ
Forward Transconductance	g FS	V_{DS} =-5 V , I_{D} =-1.5 A		4		S
Dynamic Characteristics	Dynamic Characteristics					
Input Capacitance	C _{iss}	101/1/		252		
Output Capacitance	Coss	$V_{DS} = -10V$, $V_{GS} = 0V$, $F = 1MHz$		48		pF
Reverse Transfer Capacitance	C _{rss}	1 - 11VII 12		27		
Switching Capacitance						
Turn-on Delay Time	t _{d(on)}			3		nS
Turn-on Rise Time	t _r	V_{DD} = -10V, R_L =5 Ω		4		nS
Turn-off Delay Time	t _{d(off)}	$V_{GS} = -4.5V$, $R_{GEN}=3\Omega$		18		nS
Turn-off Fall Time	t _f			3.8		nS
Total Gate Charge	Qg	V _{DS} = -10V, I _D =-1.5A.		2.9		nC
Gate-Source Charge	Q_{gs}	V _{GS} =-4.5V		0.45		nC
Gate-Drain Charge	Q_{gd}			0.75		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V _{SD}	V _{GS} =0V, I _D =-1.5A			-1.2	V
Diode Forward Current	ls				-1.5	Α

Notes:

- A. The Power dissipation P_D is based on $T_{J(MAX)}$ =150 $^{\circ}$ C, using≤10s junction-to ambient thermal resistance.
- B. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$ =150 $^{\circ}$ C.Ratings are based on low frequency and duty cycles to keep initial T_J =25 $^{\circ}$ C.
- C. The Static characteristics in Figures are obtained using \leq 300 μ s pulses, duty cycle 2% max.



Typical Electrical and Thermal Characteristics

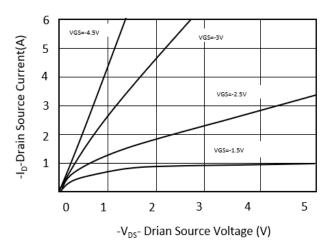


Figure 1: On-region Characteristics

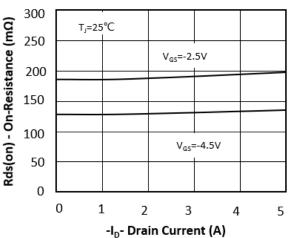


Figure 3: Drain-Source On-Resistance

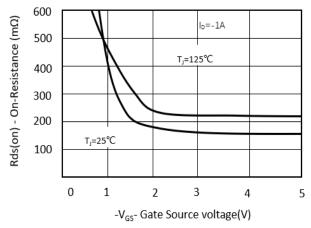


Figure 5: On-Resistance vs. Gate-Source Voltage

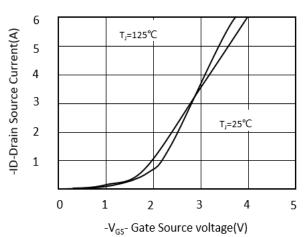


Figure 2: Transfer Characteristics

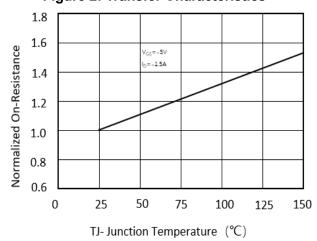


Figure 4: On-Resistance vs. Junction Temperature

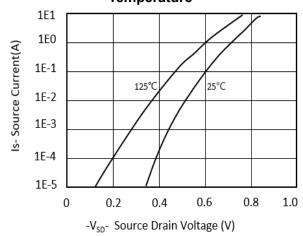


Figure 6: Body-Diode Characteristics



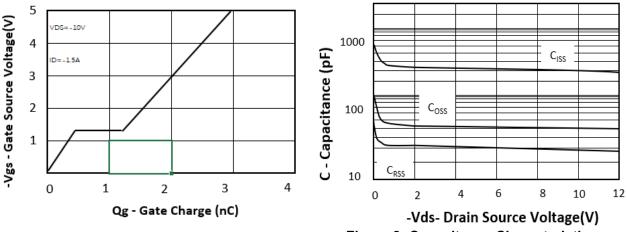


Figure 7: Gate-Charge Characteristics

Figure 8: Capacitance Characteristics

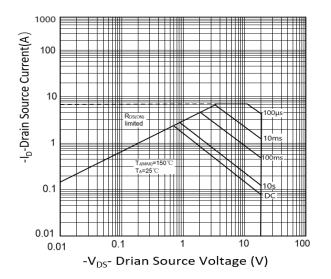


Figure 9: Safe Operation Area

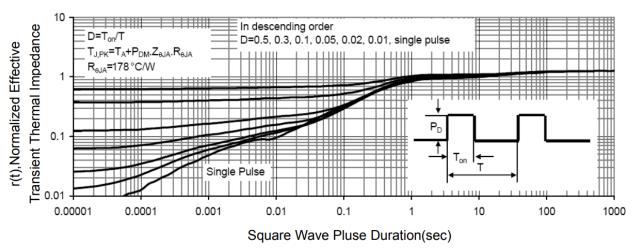
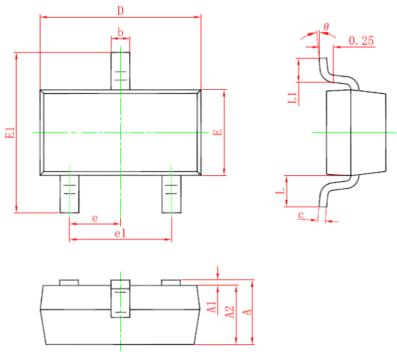


Figure 10: Normalized Maximum transient Thermal Impedance



SOT-23 Package Information



C) male of	Dimensions In Millimeters		Dimensions In Inches		
Symbol	Min.	Max.	Min.	Max.	
Α	0.900	1.150	0.035	0.045	
A1	0.000	0.100	0.000	0.004	
A2	0.900	1.050	0.035	0.041	
b	0.300	0.500	0.012	0.020	
С	0.080	0.150	0.003	0.006	
D	2.800	3.000	0.110	0.118	
E	1.200	1.400	0.047	0.055	
E1	2.250	2.550	0.089	0.100	
е	0.950 TYP.		0.037 TYP.		
e1	1.800	2.000	0.071	0.079	
L	0.550 REF.		0.022 REF.		
L1	0.300	0.500	0.012	0.020	
θ	0°	8°	0°	8°	

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