

CHIPLINK P-Channel Enhancement Mode Power MOSFET

Description

The LX2305S combines advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltage as low as 1.8V. This device is suitable for use as a load switch or other general applications.

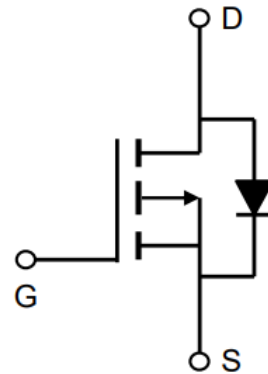
Features

- $V_{DS} = -20V$, $I_D = -5A$
 $R_{DS(ON)typ.} = 32m\Omega @ V_{GS} = -4.5V$
 $R_{DS(ON)typ.} = 41m\Omega @ V_{GS} = -2.5V$
- Low gate charge
- High power and current handling capability
- Termination is Lead-free and RoHS Compliant

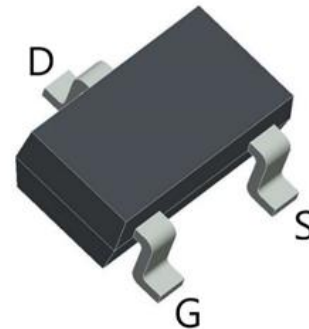


Applications

- PWM applications
- Load switch
- Power Management



Schematic Diagram



SOT23 Package

Maximum Ratings($T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	± 12	V
Continuous Drain Current	I_D	-5	A
Pulsed Drain Current ^B	I_{DM}	-17	A
Maximum Power Dissipation ^A	P_D	1.0	W
Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction to Ambient	R_{QJA}	114	$^\circ C/W$
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Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Test conditions	MIN	TYP	MAX	UNIT
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250uA	-20			V
Gate-Threshold Voltage	V _{th(GS)}	V _{DS} = V _{GS} , I _D =-250 uA	-0.4	-0.7	-1.0	V
Gate-body Leakage	IGSS	V _{DS} =0V, V _{GS} =±12V			±100	nA
Zero Gate Voltage Drain Current	IDSS	V _{DS} =-20V, V _{GS} =0V			-1	uA
Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =-4.5V, I _D =-4.0A		32	42	mΩ
		V _{GS} =-2.5V, I _D =-3.0A		41	50	mΩ
		V _{GS} =-1.8V, I _D =-1.0A		60	110	mΩ
Forward Transconductance	g _{FS}	V _{DS} =-5V, I _D =-2A		4		s
Dynamic Characteristics						
Input Capacitance	C _{iss}	V _{DS} = -10V, V _{GS} =0V, F=1MHz		830		pF
Output Capacitance	C _{oss}			132		
Reverse Transfer Capacitance	C _{rss}			85		
Switching Capacitance						
Turn-on Delay Time	t _{d(on)}	V _{DD} = -10V, R _L =5Ω V _{GS} = -4.5V, R _{GEN} =3Ω		10		nS
Turn-on Rise Time	t _r			32		nS
Turn-off Delay Time	t _{d(off)}			50		nS
Turn-off Fall Time	t _f			51		nS
Total Gate Charge	Q _g	V _{DS} = -10V, I _D =-2A, V _{GS} =-4.5V		8.8		nC
Gate-Source Charge	Q _{gs}			1.4		nC
Gate-Drain Charge	Q _{gd}			1.9		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V _{SD}	V _{GS} =0V, I _D =-4.2A			-1.2	V
Diode Forward Current	I _s				-5	A

Notes:

- The Power dissipation P_D is based on $T_{J(MAX)}=150^{\circ}\text{C}$, using $\leq 10s$ junction-to ambient thermal resistance.
- Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=150^{\circ}\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J=25^{\circ}\text{C}$.
- The Static characteristics in Figures are obtained using $<300\mu s$ pulses, duty cycle 2% max.

Typical Electrical and Thermal Characteristics

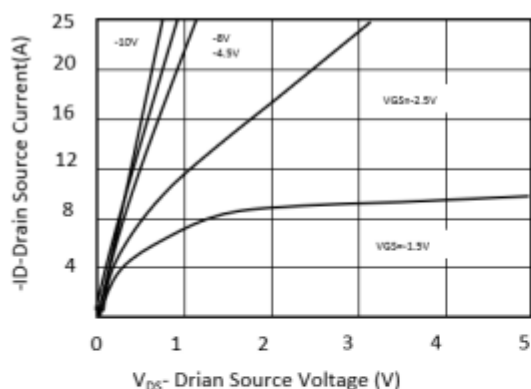


Figure 1: Output Characteristics

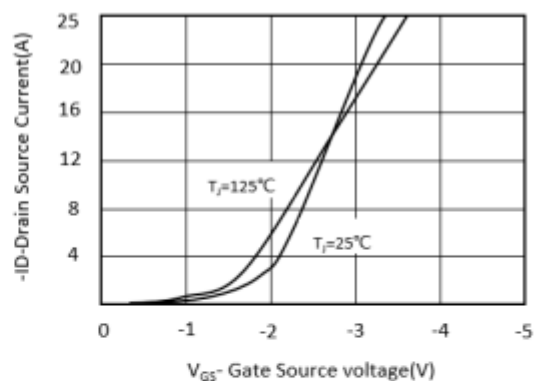


Figure 2: Transfer Characteristics

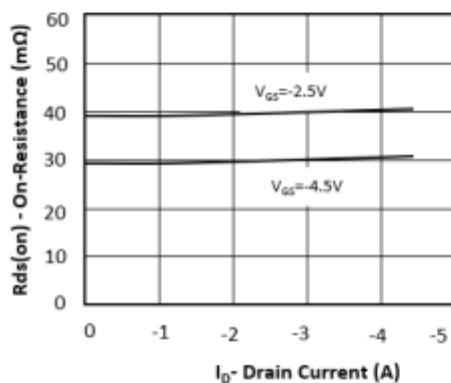


Figure 3: On-Resistance Vs. Drain Current

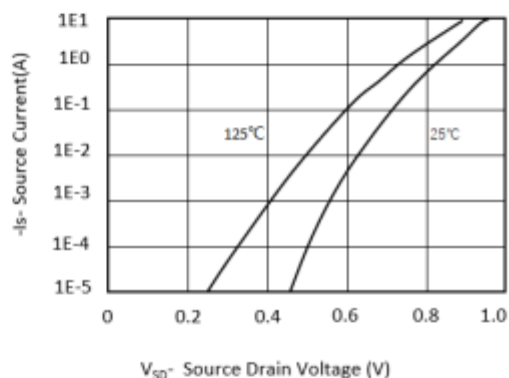


Figure 4: Body Diode Characteristics

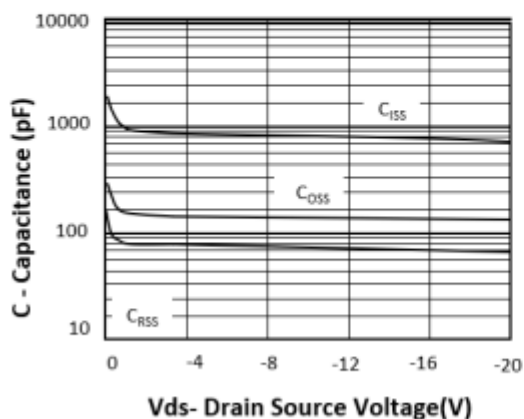


Figure 5: Capacitance Characteristics

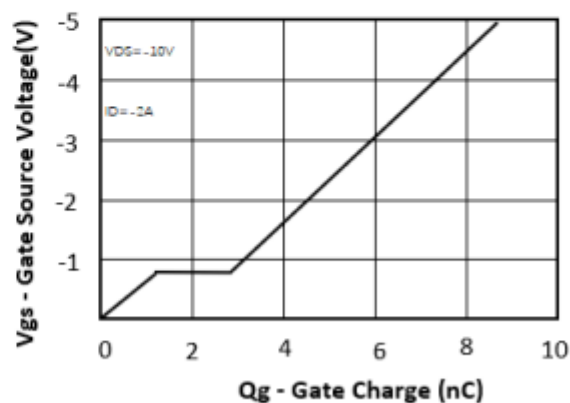


Figure 6: Gate Charge Characteristics

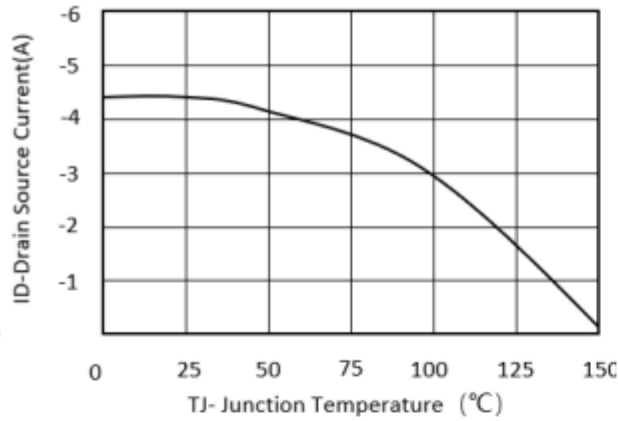


Figure 7: Drain Current Vs Junction Temperature

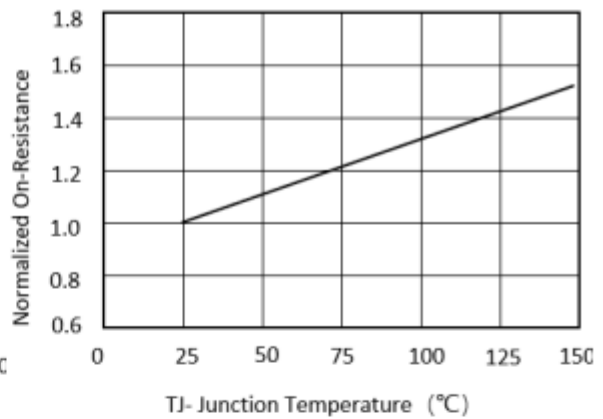


Figure 8: Normalized On-resistance Vs. Junction Temperature

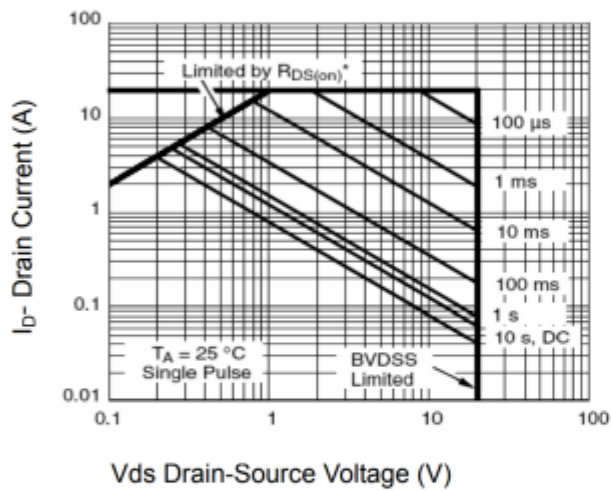


Figure 9: Safe Operation Area

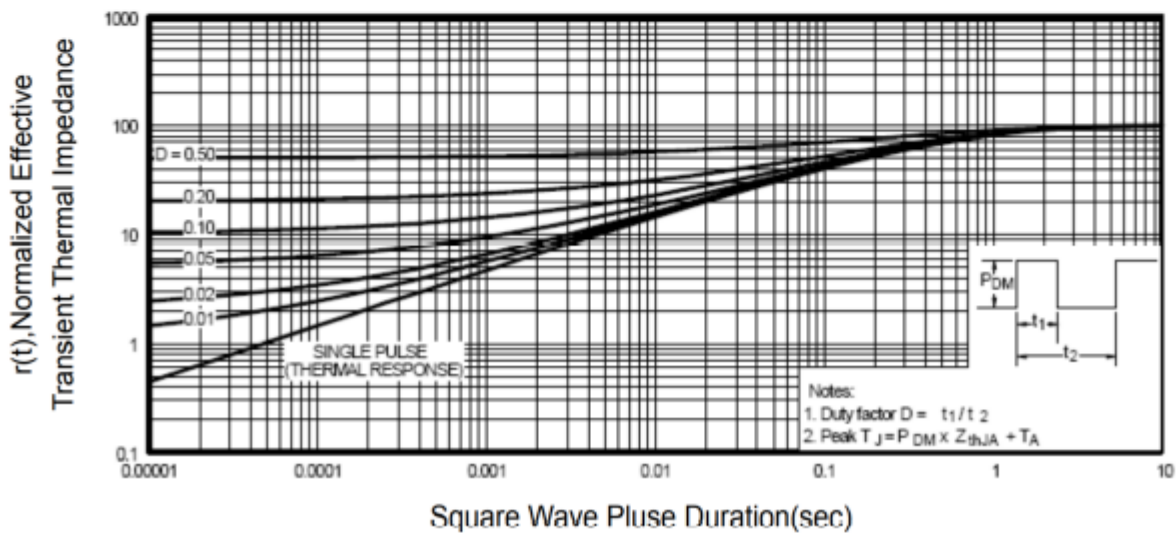
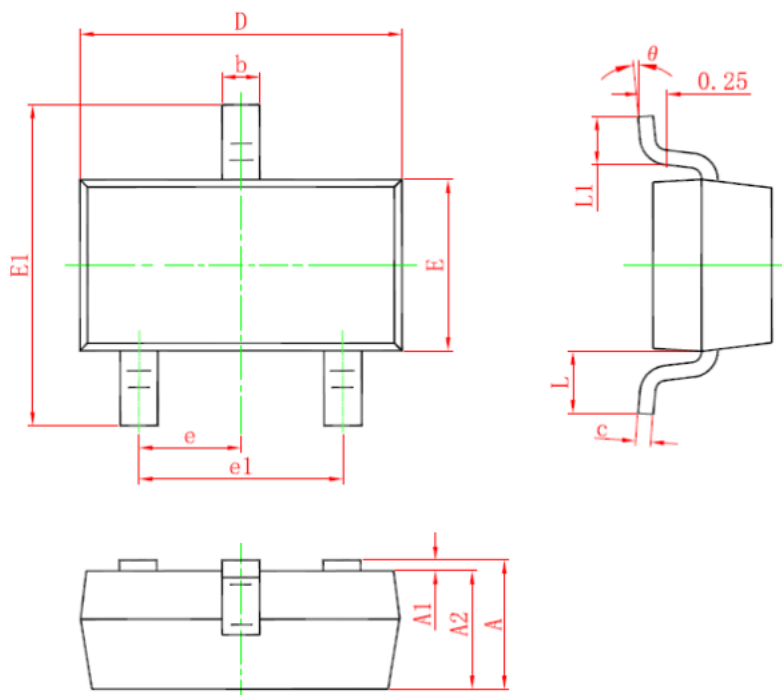


Figure 10: Normalized Maximum Transient Thermal Impedance

SOT-23 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP.		0.037 TYP.	
e1	1.800	2.000	0.071	0.079
L	0.550 REF.		0.022 REF.	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

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