8-bit Serial-in, Serial or Parallel-out Shift Register with Output Latches; 3-state

Features:

- Input levels:CMOS level
- 8-bit serial input
- 8-bit serial or parallel output
- Storage register with 3-state outputs
- Shift register with direct clear
- Specified from -40℃ to +85℃
- Packaging information: DIP-16、SOP-16、TSSOP-16、QSOP-16 and QFN-16


DIP-16


SOP-16


QSOP-16


TSSOP-16


QFN-16 3*3

Ordering Information

DEVICE	Package Type	MARKING	Packing	Packing Qty
74HC595DN	DIP-16	74HC595D	TUBE	1000pcs/box
74HC595DM/TR	SOP-16	74HC595D	REEL	2500pcs/reel
74HC595DMT/TR	TSSOP-16	HC595D	REEL	2500pcs/reel
74HC595DMS/TR	QSOP-16	HC595D	REEL	2500pcs/reel
74HC595DLQ/TR	QFN-16 3*3	HC595D	REEL	5000pcs/reel

General Description

The 74HC595D is an 8-bit serial-in/serial or parallel-out shift register with a storage register and 3-state outputs. Both the shift and storage register have separate clocks. The device features a serial input(DS) and a serial output (Q7S) to enable cascading and an asynchronous reset $\overline{MR}$ input. A LOW on $\overline{MR}$ will reset the shift register. Data is shifted on the LOW-to-HIGH transitions of the SHCP input. The data in the shift register is transferred to the storage register on a LOW-to-HIGH transition of the STCP input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register. Data in the storage register appears at the output whenever the output enable input ($\overline{OE}$) is LOW.A HIGH on $\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the registers. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

Block Diagram

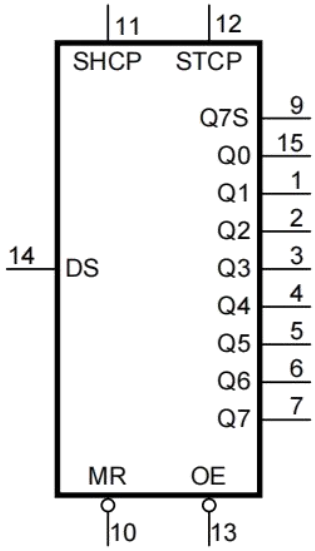


Figure 1. Logic symbol

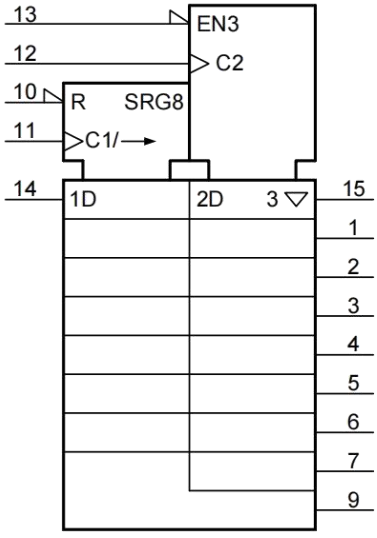


Figure 2. IEC logic symbol

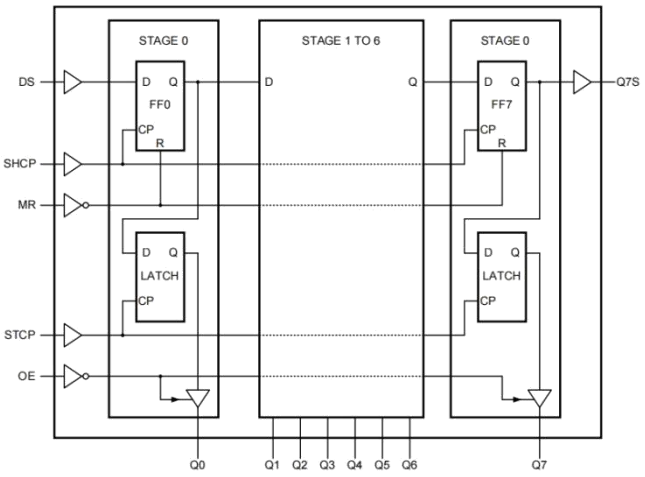


Figure 3. Logic diagram

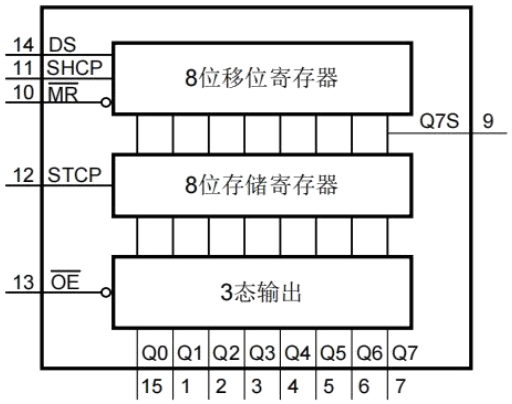


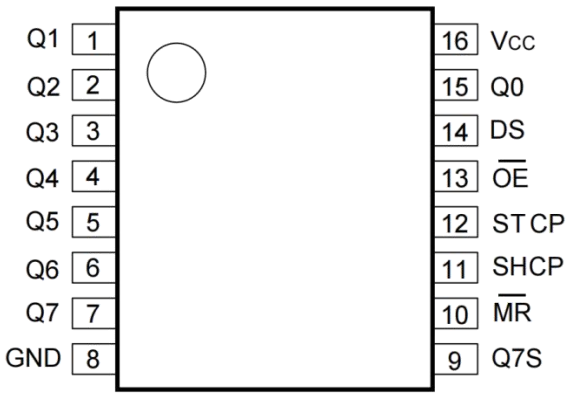
Figure 4. Functional diagram

Function Table

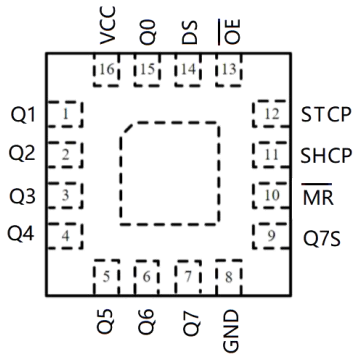
Control				Input	Output		Function
SHCP	STCP	$\overline{OE}$	$\overline{MR}$	DS	Q7S	Qn	
X	X	L	L	X	L	NC	a LOW-level on $\overline{MR}$ only affects the shift registers
X	↑	L	L	X	L	L	empty shift register loaded into storage register
X	X	H	L	X	L	Z	shift register clear; parallel outputs in high - impedance OFF-state
↑	X	L	H	H	Q6S	NC	logic HIGH-level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q6S) appears on the serial output(Q7S)
X	↑	L	H	X	NC	QnS	contents of shift register stages (internal QnS) are transferred to the storage register and parallel output stages
↑	↑	L	H	X	Q6S	QnS	contents of shift register shifted through; previous contents of the shift register is transferred to the storage register and the parallel output stages

Note: H=HIGH voltage level; L=LOW voltage level; Z=high-impedance OFF-state;
↑=LOW-to-HIGH transition; X=don't care; NC=no change.

Pin Configuration



SOP-16/DIP-16/TSSOP-16/QSOP-16



QFN-16 3*3

Pin Description

Pin No.	Pin Name	Description
1	Q1	parallel data output
2	Q2	parallel data output
3	Q3	parallel data output
4	Q4	parallel data output
5	Q5	parallel data output
6	Q6	parallel data output
7	Q7	parallel data output
8	GND	ground (0V)
9	Q7S	serial data output
10	$\overline{MR}$	master reset (active LOW)
11	SHCP	shift register clock input
12	STCP	storage register clock input
13	$\overline{OE}$	output enable input (active LOW)
14	DS	serial data input
15	Q0	parallel data output
16	V_{CC}	supply voltage

Electrical Parameter

Absolute Maximum Ratings

(Voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V_{CC}	-		-0.5	+7.0	V
input clamping current	I_{IK}	V_I < -0.5V or V_I > V_{CC}+0.5V		-	±20	mA
output clamping current	I_{OK}	V_O < -0.5V or V_O > V_{CC}+0.5V		-	±20	mA
output current	I_O	V_O= -0.5V to (V_{CC}+0.5V)	pin Q7S	-	±25	mA
			pins Qn	-	±35	mA
supply current	I_{CC}	-		-	70	mA
ground current	I_{GND}	-		-70	-	mA
storage temperature	T_{stg}	-		-65	+150	℃
total power dissipation	P_{tot}	-		-	500	mW
soldering temperature	T_L	10s		260		℃

Note:Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured.

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{CC}	-	2.0	5.0	6.0	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
ambient temperature	T_{amb}	-	-40	-	+85	℃

Electrical Characteristics

DC Characteristics 1

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	1.2	-	V
		V_{CC}=4.5V		3.15	2.4	-	V
		V_{CC}=6.0V		4.2	3.2	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	0.8	0.5	V
		V_{CC}=4.5V		-	1.35	1.0	V
		V_{CC}=6.0V		-	1.8	1.5	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	all outputs; I_O=-20uA; V_{CC}=2.0V	1.9	2.0	-	V
			all outputs; I_O=-20uA; V_{CC}=4.5V	4.4	4.5	-	V
			all outputs; I_O=-20uA; V_{CC}=6.0V	5.9	6.0	-	V
			Q7S output; I_O=-4.0mA; V_{CC}=4.5V	3.84	4.32	-	V
			Q7S output; I_O=-5.2mA; V_{CC}=6.0V	5.34	5.81	-	V
			Qn bus driver outputs; I_O=-6.0mA; V_{CC}=4.5V	3.84	4.32	-	V
			Qn bus driver outputs; I_O=-7.8mA; V_{CC}=6.0V	5.34	5.81	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	all outputs; I_O=20uA; V_{CC}=2.0V	-	0	0.1	V
			all outputs; I_O=20uA; V_{CC}=4.5V	-	0	0.1	V
			all outputs; I_O=20uA; V_{CC}=6.0V	-	0	0.1	V
			Q7S output; I_O=4.0mA; V_{CC}=4.5V	-	0.15	0.33	V
			Q7S output; I_O=5.2mA; V_{CC}=6.0V	-	0.16	0.33	V
			Qn bus driver outputs; I_O=6.0mA; V_{CC}=4.5V	-	0.15	0.33	V
			Qn bus driver outputs; I_O=7.8mA; V_{CC}=6.0V	-	0.16	0.33	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
OFF-state output current	I_{OZ}	V_I=V_{IH} or V_{IL}; V_{CC}=6.0V; V_O=V_{CC} or GND		-	-	±5.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	80	uA
input capacitance	C_I	-		-	3.5	-	pF

DC Characteristics 2

(T_{amb}=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.0	V
		V_{CC}=6.0V		-	-	1.5	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	all outputs; I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V
			all outputs; I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			all outputs; I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
			Q7S output; I_O=-4.0mA; V_{CC}=4.5V	3.7	-	-	V
			Q7S output; I_O=-5.2mA; V_{CC}=6.0V	5.2	-	-	V
			Qn bus driver outputs; I_O=-6.0mA; V_{CC}=4.5V	3.7	-	-	V
			Qn bus driver outputs; IO=-7.8mA; VCC=6.0V	5.2	-	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	all outputs; I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
			all outputs; I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			all outputs; I_O=20uA; V_{CC}=6.0V	-	-	0.1	V
			Q7S output; I_O=4.0mA; V_{CC}=4.5V	-	-	0.4	V
			Q7S output; I_O=5.2mA; V_{CC}=6.0V	-	-	0.4	V
			Qn bus driver outputs; I_O=6.0mA; V_{CC}=4.5V	-	-	0.4	V
			Qn bus driver outputs; I_O=7.8mA; V_{CC}=6.0V	-	-	0.4	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
OFF-state output current	I_{OZ}	V_I=V_{IH} or V_{IL}; V_{CC}=6.0V; V_O=V_{CC} or GND		-	-	±10	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	160	uA

AC Characteristics 1

(T_{amb}=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.[1]	Max.	Unit
propagation delay	t_{PLH}, t_{PHL}	SHCP to Q7S; see Figure 6	V_{CC}=2.0V	-	75	160	ns
			V_{CC}=4.5V	-	19	32	ns
			V_{CC}=6.0V	-	15	27	ns
		STCP to Qn; see Figure 7	V_{CC}=2.0V	-	85	175	ns
			V_{CC}=4.5V	-	20	35	ns
			V_{CC}=6.0V	-	16	30	ns
HIGH to LOW propagation delay	t_{PHL}	$\overline{MR}$ to Q7S; see Figure 9	V_{CC}=2.0V	-	47	175	ns
			V_{CC}=4.5V	-	17	35	ns
			V_{CC}=6.0V	-	14	30	ns
$\overline{OE}$ to Qn enable time	t_{PZH}, t_{PZL}	see Figure 10	V_{CC}=2.0V	-	47	150	ns
			V_{CC}=4.5V	-	17	30	ns
			V_{CC}=6.0V	-	14	26	ns
$\overline{OE}$ to Qn disable time	t_{PLZ}, t_{PHZ}	see Figure 10	V_{CC}=2.0V	-	41	150	ns
			V_{CC}=4.5V	-	15	30	ns
			V_{CC}=6.0V	-	12	27	ns
pulse width	t_W	SHCP HIGH or LOW; see Figure 6	V_{CC}=2.0V	75	17	-	ns
			V_{CC}=4.5V	15	6	-	ns
			V_{CC}=6.0V	13	5	-	ns
		STCP HIGH or LOW; see Figure 7	V_{CC}=2.0V	75	11	-	ns
			V_{CC}=4.5V	15	4	-	ns
			V_{CC}=6.0V	13	3	-	ns
		$\overline{MR}$ LOW; see Figure 9	V_{CC}=2.0V	75	17	-	ns
			V_{CC}=4.5V	15	6	-	ns
			V_{CC}=6.0V	13	5	-	ns
set-up time	t_{su}	DS to SHCP; see Figure 8	V_{CC}=2.0V	50	11	-	ns
			V_{CC}=4.5V	10	4	-	ns
			V_{CC}=6.0V	9	3	-	ns
		SHCP to STCP; see Figure 7	V_{CC}=2.0V	75	22	-	ns
			V_{CC}=4.5V	15	8	-	ns
			V_{CC}=6.0V	13	7	-	ns
DS to SHCP hold time	t_h	see Figure 8	V_{CC}=2.0V	3	-6	-	ns
			V_{CC}=4.5V	3	-2	-	ns
			V_{CC}=6.0V	3	-2	-	ns
$\overline{MR}$ to SHCP recovery time	t_{rec}	see Figure 9	V_{CC}=2.0V	50	-19	-	ns
			V_{CC}=4.5V	10	-7	-	ns
			V_{CC}=6.0V	9	-6	-	ns
maximum frequency	f_{max}	SHCP or STCP; see Figure 6 and Figure 7	V_{CC}=2.0V	9	-	-	MHz
			V_{CC}=4.5V	30	-	-	MHz
			V_{CC}=6.0V	35	-	-	MHz

Note:

[1] Typical values are measured at nominal supply voltage.

AC Characteristics 2

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
propagation delay	t_{PLH}, t_{PHL}	SHCP to Q7S; see Figure 6	V_{CC}=2.0V	-	-	200	ns
			V_{CC}=4.5V	-	-	40	ns
			V_{CC}=6.0V	-	-	34	ns
		STCP to Qn; see Figure 7	V_{CC}=2.0V	-	-	220	ns
			V_{CC}=4.5V	-	-	44	ns
			V_{CC}=6.0V	-	-	37	ns
HIGH to LOW propagation delay	t_{PHL}	$\overline{MR}$ to Q7S; see Figure 9	V_{CC}=2.0V	-	-	220	ns
			V_{CC}=4.5V	-	-	44	ns
			V_{CC}=6.0V	-	-	37	ns
$\overline{OE}$ to Qn enable time	t_{PZH}, t_{PZL}	see Figure 10	V_{CC}=2.0V	-	-	190	ns
			V_{CC}=4.5V	-	-	38	ns
			V_{CC}=6.0V	-	-	33	ns
$\overline{OE}$ to Qn disable time	t_{PLZ}, t_{PHZ}	see Figure 10	V_{CC}=2.0V	-	-	190	ns
			V_{CC}=4.5V	-	-	38	ns
			V_{CC}=6.0V	-	-	33	ns
pulse width	t_W	SHCP HIGH or LOW; see Figure 6	V_{CC}=2.0V	95	-	-	ns
			V_{CC}=4.5V	19	-	-	ns
			V_{CC}=6.0V	16	-	-	ns
		STCP HIGH or LOW;	V_{CC}=2.0V	95	-	-	ns
			V_{CC}=4.5V	19	-	-	ns
		see Figure 7	V_{CC}=6.0V	16	-	-	ns
		$\overline{MR}$ LOW; see Figure 9	V_{CC}=2.0V	95	-	-	ns
			V_{CC}=4.5V	19	-	-	ns
			V_{CC}=6.0V	16	-	-	ns
set-up time	t_{su}	DS to SHCP; see Figure 8	V_{CC}=2.0V	65	-	-	ns
			V_{CC}=4.5V	13	-	-	ns
			V_{CC}=6.0V	11	-	-	ns
		SHCP to STCP; see Figure 7	V_{CC}=2.0V	95	-	-	ns
			V_{CC}=4.5V	19	-	-	ns
			V_{CC}=6.0V	16	-	-	ns
DS to SHCP hold time	t_h	see Figure 8	V_{CC}=2.0V	3	-	-	ns
			V_{CC}=4.5V	3	-	-	ns
			V_{CC}=6.0V	3	-	-	ns
$\overline{MR}$ to SHCP recovery time	t_{rec}	see Figure 9	V_{CC}=2.0V	65	-	-	ns
			V_{CC}=4.5V	13	-	-	ns
			V_{CC}=6.0V	11	-	-	ns
maximum frequency	f_{max}	SHCP or STCP; see Figure 6 and Figure 7	V_{CC}=2.0V	4.8	-	-	MHz
			V_{CC}=4.5V	24	-	-	MHz
			V_{CC}=6.0V	28	-	-	MHz

AC Characteristics 3

(T_{amb}=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
propagation delay	t_{PLH}, t_{PHL}	SHCP to Q7S; see Figure 6	V_{CC}=2.0V	-	-	240	ns
			V_{CC}=4.5V	-	-	48	ns
			V_{CC}=6.0V	-	-	41	ns
		STCP to Qn; see Figure 7	V_{CC}=2.0V	-	-	265	ns
			V_{CC}=4.5V	-	-	53	ns
			V_{CC}=6.0V	-	-	45	ns
HIGH to LOW propagation delay	t_{PHL}	$\overline{MR}$to Q7S; see Figure 9	V_{CC}=2.0V	-	-	265	ns
			V_{CC}=4.5V	-	-	53	ns
			V_{CC}=6.0V	-	-	45	ns
$\overline{OE}$ to Qn enable time	t_{PZH}, t_{PZL}	see Figure 10	V_{CC}=2.0V	-	-	225	ns
			V_{CC}=4.5V	-	-	45	ns
			V_{CC}=6.0V	-	-	38	ns
$\overline{OE}$ to Qn disable time	t_{PLZ}, t_{PHZ}	see Figure 10	V_{CC}=2.0V	-	-	225	ns
			V_{CC}=4.5V	-	-	45	ns
			V_{CC}=6.0V	-	-	38	ns
pulse width	t_W	SHCP HIGH or LOW;see Figure 6	V_{CC}=2.0V	110	-	-	ns
			V_{CC}=4.5V	22	-	-	ns
			V_{CC}=6.0V	19	-	-	ns
		STCP HIGH or LOW;see Figure 7	V_{CC}=2.0V	110	-	-	ns
			V_{CC}=4.5V	22	-	-	ns
			V_{CC}=6.0V	19	-	-	ns
		$\overline{MR}$ LOW; see Figure 9	V_{CC}=2.0V	110	-	-	ns
			V_{CC}=4.5V	22	-	-	ns
			V_{CC}=6.0V	19	-	-	ns
set-up time	t_{su}	DS to SHCP; see Figure 8	V_{CC}=2.0V	75	-	-	ns
			V_{CC}=4.5V	15	-	-	ns
			V_{CC}=6.0V	13	-	-	ns
		SHCP to STCP; see Figure 7	V_{CC}=2.0V	110	-	-	ns
			V_{CC}=4.5V	22	-	-	ns
			V_{CC}=6.0V	19	-	-	ns
DS to SHCP hold time	t_h	see Figure 8	V_{CC}=2.0V	3	-	-	ns
			V_{CC}=4.5V	3	-	-	ns
			V_{CC}=6.0V	3	-	-	ns
$\overline{MR}$ to SHCP recovery time	t_{rec}	see Figure 9	V_{CC}=2.0V	75	-	-	ns
			V_{CC}=4.5V	15	-	-	ns
			V_{CC}=6.0V	13	-	-	ns
maximum frequency	f_{max}	SHCP or STCP; see Figure 6 and Figure 7	V_{CC}=2.0V	4	-	-	MHz
			V_{CC}=4.5V	20	-	-	MHz
			V_{CC}=6.0V	24	-	-	MHz

Testing Circuit

AC Testing Circuit

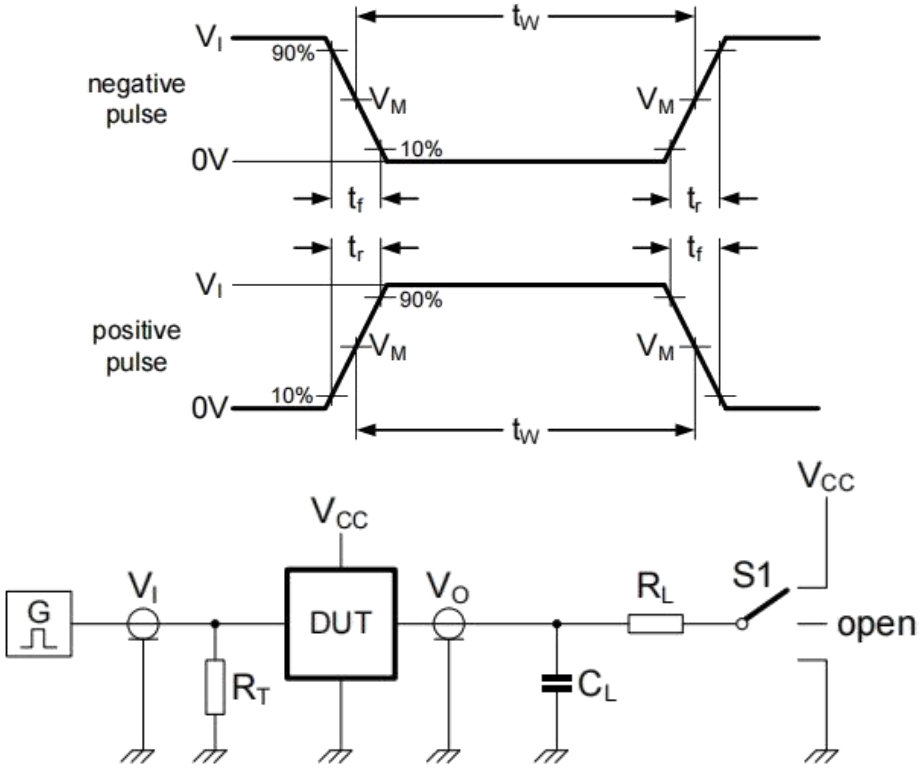


Figure 5. Test circuit for measuring switching times

Definitions for test circuit: R_L=Load resistance.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator.

S_1=Test selection switch.

AC Testing Waveforms

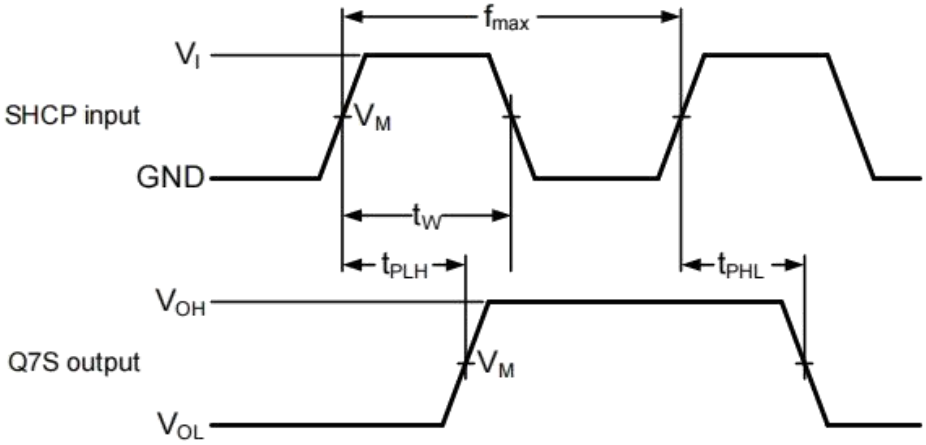


Figure 6. Shift clock pulse, maximum frequency and input to output propagation delays

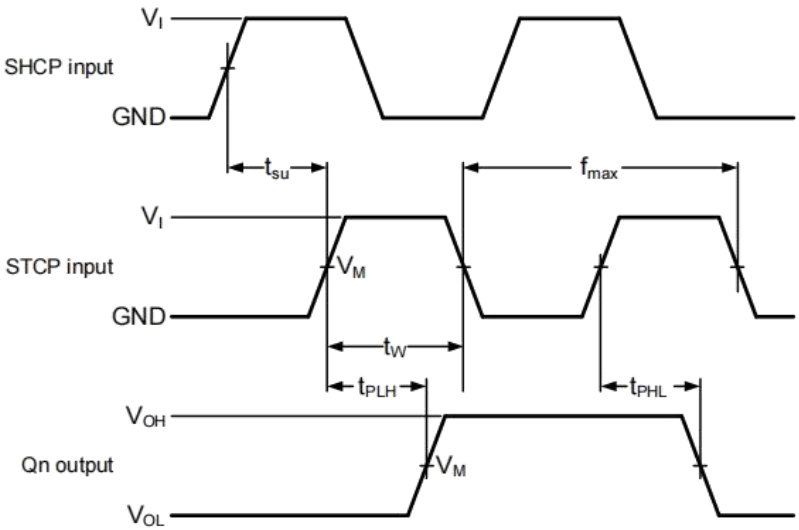


Figure 7. Storage clock to output propagation delays

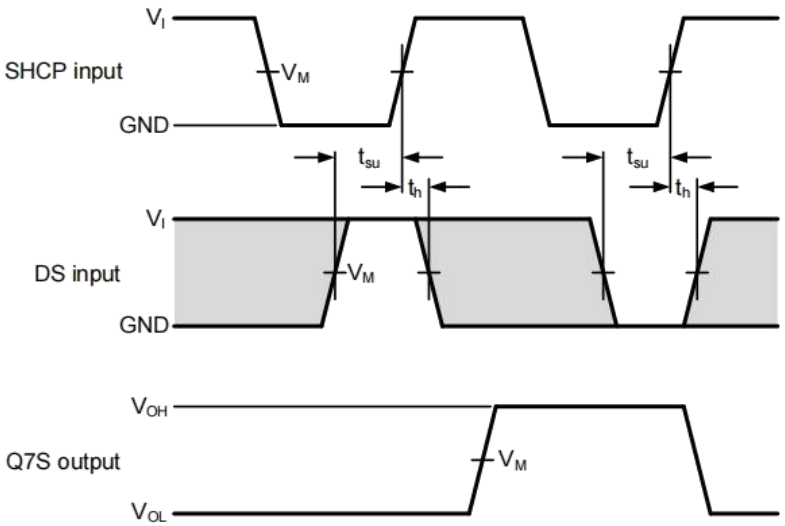


Figure 8. Data set-up and hold times

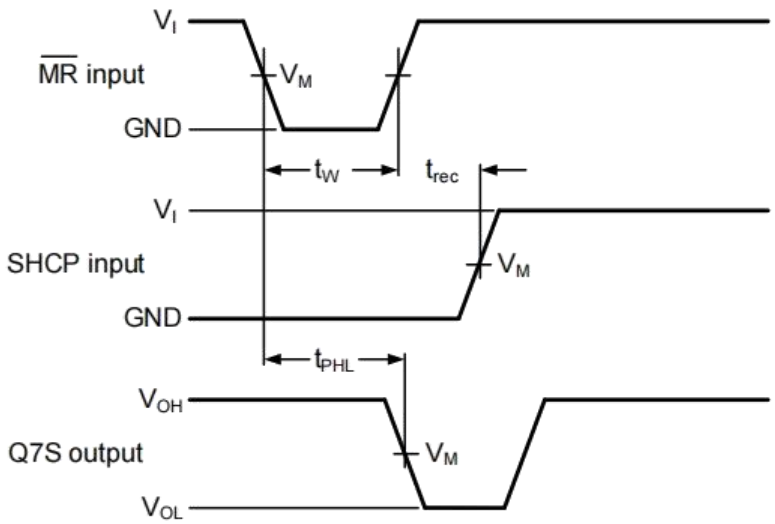


Figure 9. Master reset to output propagation delays

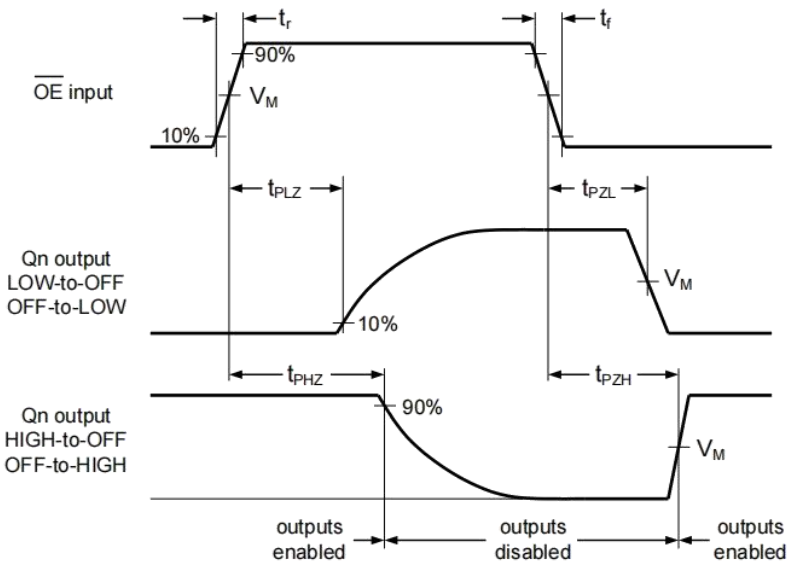


Figure 10. Enable and disable times

Measurement Points

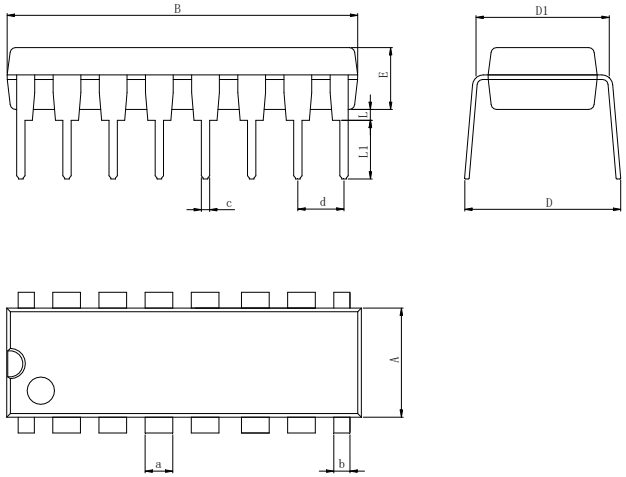
Type	Input	Output
	V_M	V_M
74HC595D	0.5×V_{CC}	0.5×V_{CC}

Test Data

Type	Input		Load		S1 position		
	V_I	t_r , t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC595D	V_{CC}	6ns	50pF	1kΩ	open	GND	V_{CC}

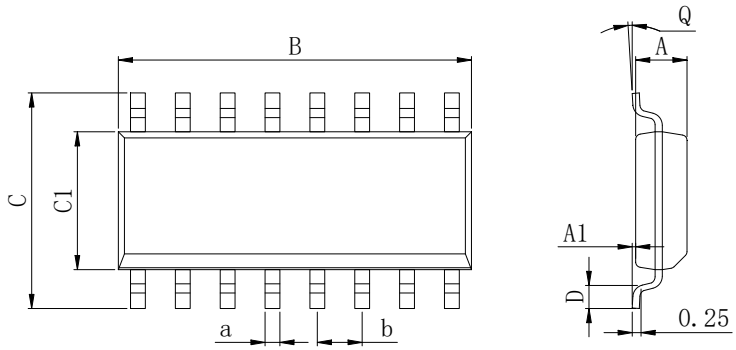
Physical Dimensions

DIP-16



Dimensions In Millimeters(DIP-16)											
Symbol:	A	B	D	D1	E	L	L1	a	b	c	d
Min:	6.10	18.94	8.10	7.42	3.10	0.50	3.00	1.50	0.85	0.40	2.54 BSC
Max:	6.68	19.56	10.9	7.82	3.55	0.70	3.60	1.55	0.90	0.50	

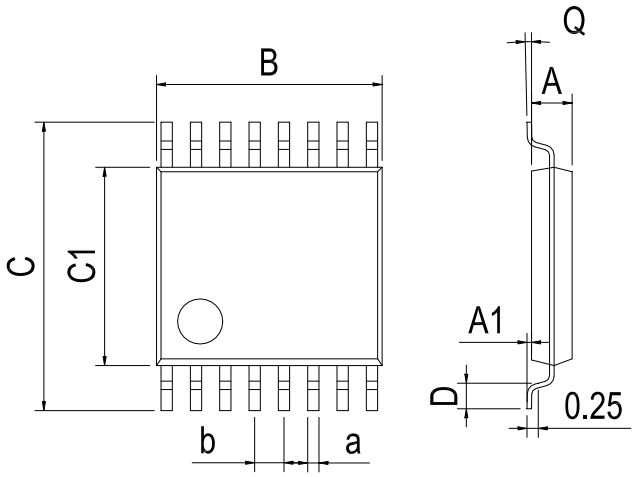
SOP-16



Dimensions In Millimeters(SOP-16)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	9.80	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	10.0	6.20	4.00	0.80	8°	0.45	

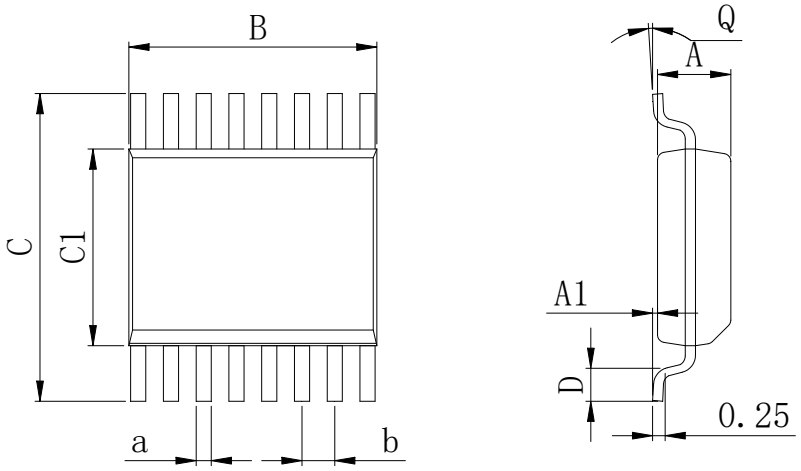
Physical Dimensions

TSSOP-16



Dimensions In Millimeters(TSSOP-16)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.85	0.05	4.90	6.20	4.30	0.40	0°	0.20	0.65 BSC
Max:	0.95	0.20	5.10	6.60	4.50	0.80	8°	0.25	

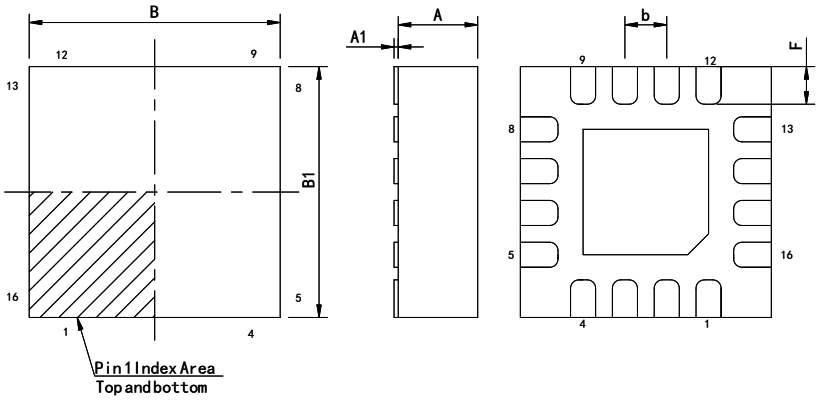
QSOP-16



Dimensions In Millimeters(QSOP-16)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	4.80	5.80	3.80	0.40	0°	0.20	0.635 BSC
Max:	1.55	0.20	5.10	6.20	4.00	0.80	8°	0.25	

Physical Dimensions

QFN-16 3*3



Dimensions In Millimeters(QFN-16 3*3)								
Symbol:	A	A1	B	B1	E	F	a	b
Min:	0.85	0	2.90	2.90	0.15	0.25	0.18	0.50TYP
Max:	0.95	0.05	3.10	3.10	0.25	0.45	0.30	

Revision History

REVISION NUMBER	DATE	REVISION	PAGE
V1.0	2016-11	New	1-18
V1.1	2024-11	Document Reformatting	1-18

IMPORTANT STATEMENT:

Huaguan Semiconductor reserves the right to change its products and services without notice. Before ordering, the customer shall obtain the latest relevant information and verify whether the information is up to date and complete. Huaguan Semiconductor does not assume any responsibility or obligation for the altered documents.

Customers are responsible for complying with safety standards and taking safety measures when using Huaguan Semiconductor products for system design and machine manufacturing. You will bear all the following responsibilities: Select the appropriate Huaguan Semiconductor products for your application; Design, validate and test your application; Ensure that your application meets the appropriate standards and any other safety,security or other requirements. To avoid the occurrence of potential risks that may lead to personal injury or property loss.

Huaguan Semiconductor products have not been approved for applications in life support, military, aerospace and other fields, and Huaguan Semiconductor will not bear the consequences caused by the application of products in these fields. All problems, responsibilities and losses arising from the user's use beyond the applicable area of the product shall be borne by the user and have nothing to do with Huaguan Semiconductor, and the user shall not claim any compensation liability against Huaguan Semiconductor by the terms of this Agreement.

The technical and reliability data (including data sheets), design resources (including reference designs), application or other design suggestions, network tools, safety information and other resources provided for the performance of semiconductor products produced by Huaguan Semiconductor are not guaranteed to be free from defects and no warranty, express or implied, is made. The use of testing and other quality control technologies is limited to the quality assurance scope of Huaguan Semiconductor. Not all parameters of each device need to be tested.

The documentation of Huaguan Semiconductor authorizes you to use these resources only for developing the application of the product described in this document. You have no right to use any other Huaguan Semiconductor intellectual property rights or any third party intellectual property rights. It is strictly forbidden to make other copies or displays of these resources. You should fully compensate Huaguan Semiconductor and its agents for any claims, damages, costs, losses and debts caused by the use of these resources. Huaguan Semiconductor accepts no liability for any loss or damage caused by infringement.