

LSI1012DW1T1G

N-Channel Enhancement Mode MOSFET

1. FEATURES

- We declare that the material of product compliance with RoHS requirements and Halogen Free.
- Surface-mounted package.
- Extremely low threshold voltage
- Advanced trench cell design
- Gate to Source ESD protected:
HBM>2KV

2. APPLICATION

- Portable appliances

3. DEVICE MARKING AND ORDERING INFORMATION

Device	Marking	Shipping
LSI1012DW1T1G	9D	3000/Tape&Reel

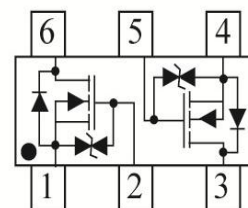
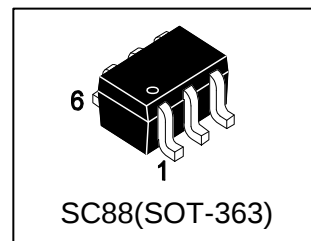
4. MAXIMUM RATINGS(Ta = 25°C)

Parameter	Symbol	Limits	Unit
Drain-Source Voltage	VDSS	20	V
Gate-Source Voltage	VGSS	±10	V
Drain Current (TA = 25 °C, VGS = 10 V)	ID	0.9	A
Pulsed Drain Current (TA = 25 °C, VGS = 10 V)	IDM	3.6	A
Storage Temperature	Tstg	-55~+150	°C
Junction Temperature	TJ	150	°C

5. THERMAL CHARACTERISTICS

Parameter	Symbol	Limits	Unit
Total Device Dissipation(Note 1)	PD	245	mW
Junction-to-Ambient(Note 1)	RθJA	511	°C/W

1. 30.0mm×25.0mm×1.6mm(FR4), Copper foil thickness 35μm;

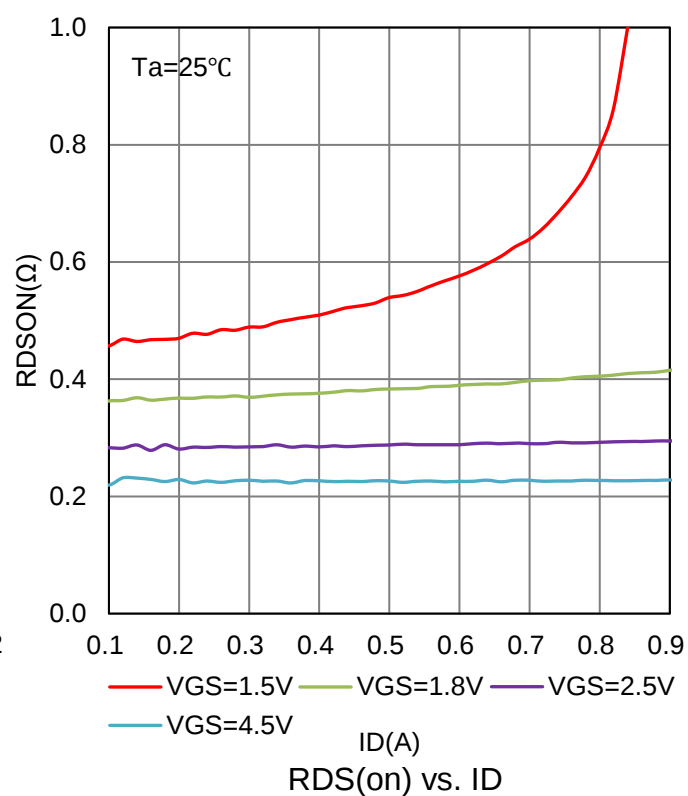
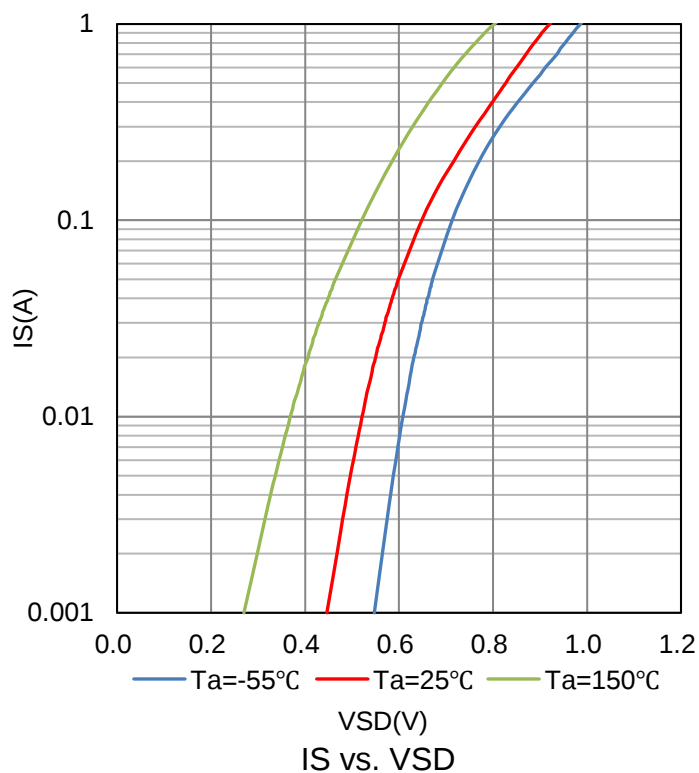
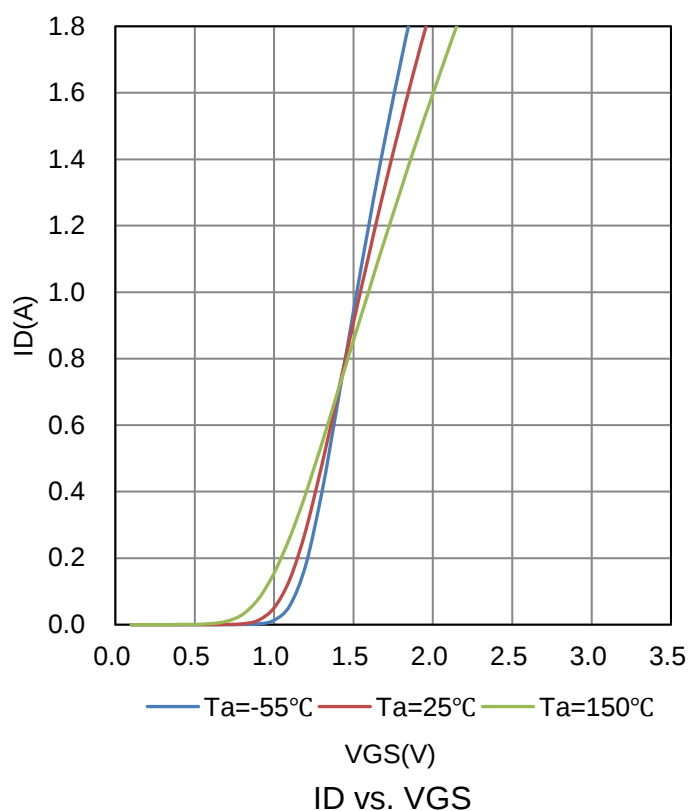
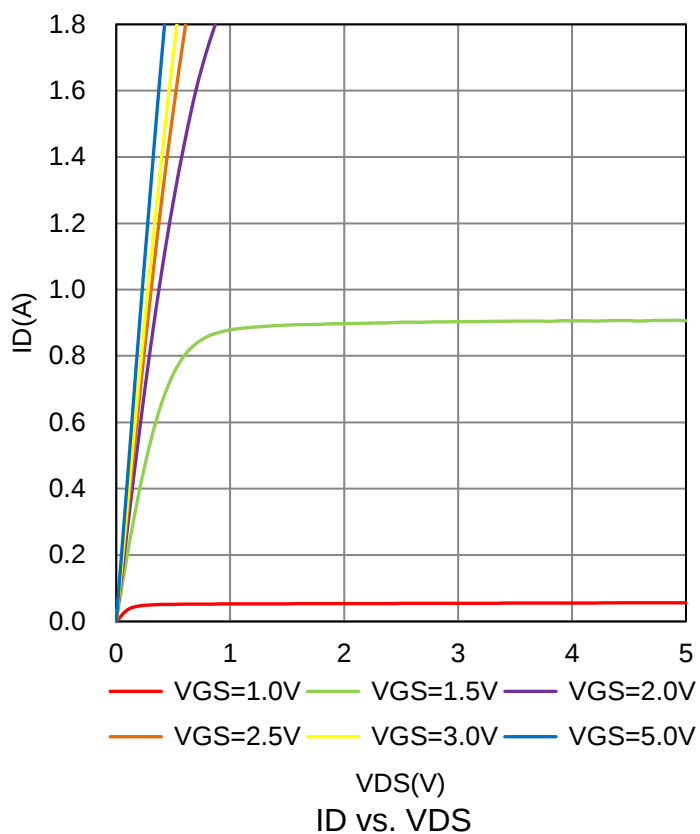


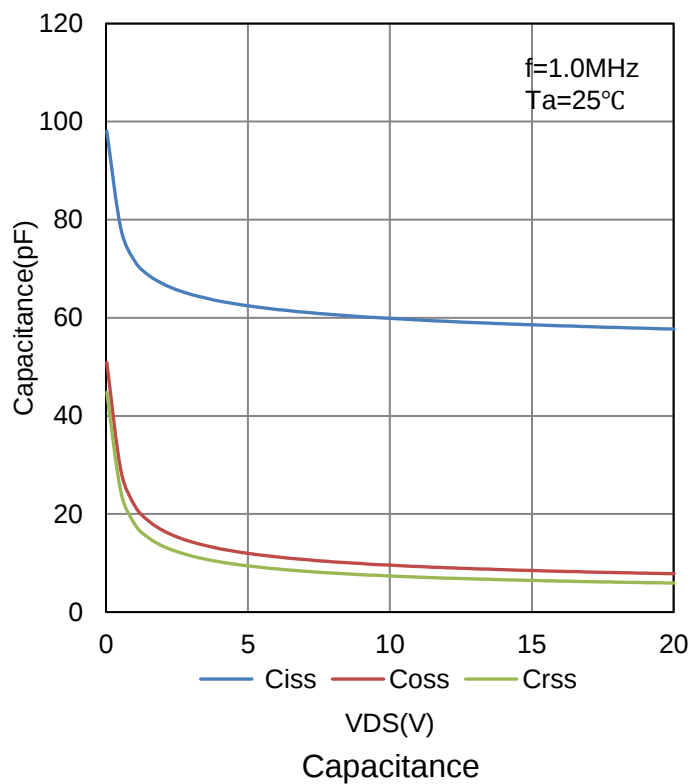
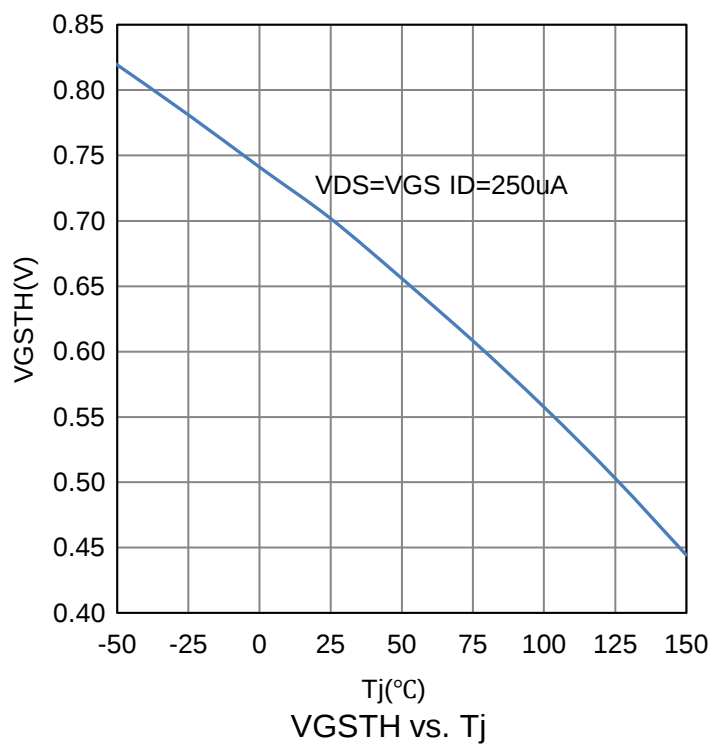
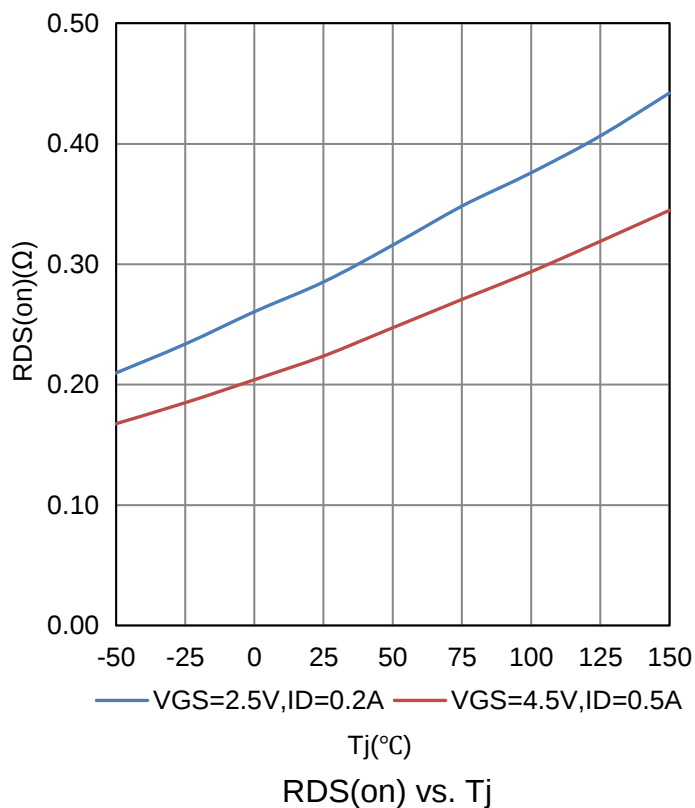
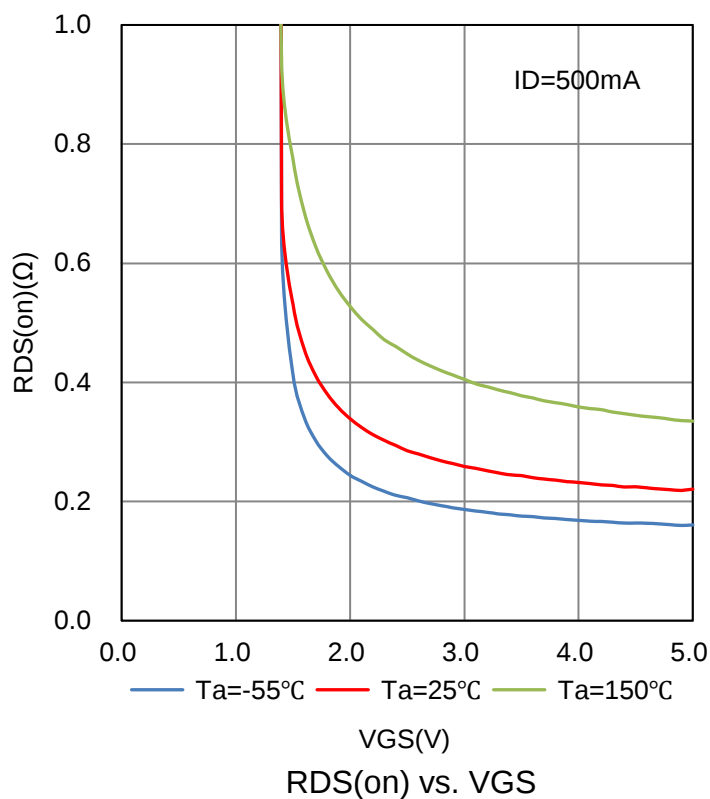
6. ELECTRICAL CHARACTERISTICS (Ta= 25°C)

Characteristic		Symbol	Min.	Typ.	Max.	Unit
Static Characteristics						
Drain-Source Breakdown Voltage (VGS = 0 V, IDS = 250 μA)		BVDSS	20	-	-	V
Gate Threshold Voltage (VDS = VGS , IDS = 250 μA)		VGS(th)	0.3	0.65	1	V
Drain Leakage Current (VDS = 16 V, VGS = 0V) (VDS = 16 V, VGS = 0V, TJ = 85 °C)		IDSS	- -	- -	1 30	μA
Gate Leakage Current (VGS = ±8 V, VDS = 0 V)		IGSS	-	-	±10	μA
On-State Resistance (VGS = 4.5 V, IDS = 0.5 A) (VGS = 2.5 V, IDS = 0.2 A) (VGS = 1.8 V, IDS = 0.1 A)		RDS(ON)	- - -	0.25 0.35 0.4	0.4 0.65 0.8	Ω
Diode Characteristics						
Diode Forward Voltage (ISD = 0.5 A, VGS = 0 V)		VSD	-	0.7	1.3	V
Dynamic						
Input Capacitance	(VGS = 0 V, VDS = 10 V,f=1MHz)	Ciss	-	60.7	-	pF
Output Capacitance		Coss	-	9.8	-	
Reverse Transfer Capacitance		Crss	-	7.6	-	
Turn-On Delay Time	(VDS = 10 V, VGEN= 4.5 V,RG = 10 Ω, RL = 50 Ω,ID = 0.2 A)	td(on)	-	6.8	-	nS
Rise Time		tr	-	5	-	
Turn-Off Delay Time		td(off)	-	48	-	
Fall Time		tf	-	17	-	
Total Gate Charge	(VGS = 4.5 V, VDS = 10 V,IDS = 0.5 A)	Qg	-	0.88	-	nC
Gate-Source Charge		Qgs	-	0.13	-	
Gate-Drain Charge		Qgd	-	0.25	-	
Gate Resistance (VDS=0V,VGS=0V,f=1MHz)		Rg	-	52	-	Ω

2. Pulse width $\leq$ 300 μ s, duty cycle $\leq$ 2%

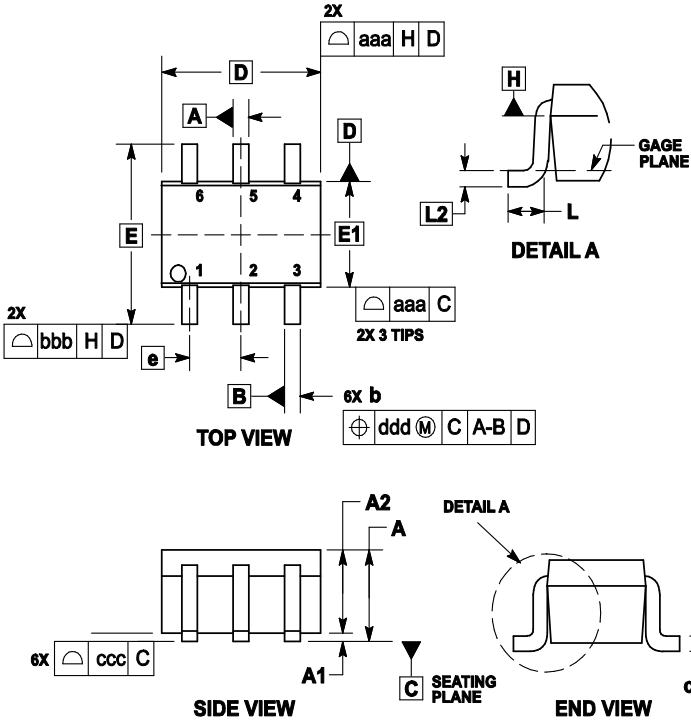
7.ELECTRICAL CHARACTERISTICS CURVES



7.ELECTRICAL CHARACTERISTICS CURVES(Con.)


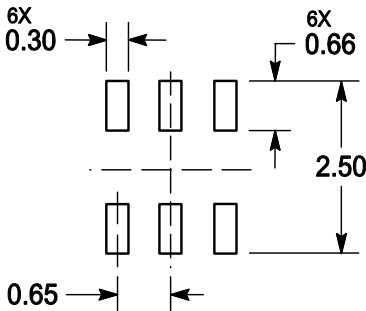
8.OUTLINE AND DIMENSIONS

- Notes:
- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 - 2. CONTROLLING DIMENSION: MILLIMETERS.
 - 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
 - 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.



DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	0.043
A1	0.00	---	0.10	0	---	0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.01
C	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.07	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018
L2	0.15 BSC			0.006 BSC		
aaa	0.15			0.01		
bbb	0.30			0.01		
ccc	0.10			0.00		
ddd	0.10			0.00		

9.SOLDERING FOOTPRINT



DISCLAIMER

- Curve guarantee in the specification. The curve of test items with electric parameter is used as quality guarantee. The curve of test items without electric parameter is used as reference only.
- Before you use our Products for new Project, you are requested to carefully read this document and fully understand its contents. LRC shall not be in any way responsible or liable for failure, malfunction or accident arising from the use of any LRC's Products against warning, caution or note contained in this document.
- All information contained in this document is current as of the issuing date and subject to change without any prior notice. Before purchasing or using LRC's Products, please confirm the latest information with a LRC sales representative.