

## General description

The MX5052SL high-side OR-ing works with an internal MOSFET and acts as an ideal diode rectifier when connected in series with the power supply. This OR-ing circuit enables MOSFETs to replace diode rectifiers in power distribution networks, reducing power loss and voltage drop.

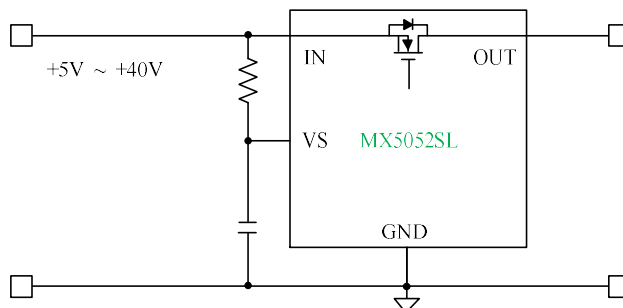
The MX5052SL controller provides charge pump gate drive for an internal N-channel MOSFET and fast response comparator to turn off the FET when current flows in reverse. The MX5052SL can be connected to power supplies from 1V to 40V (a separate VS supply is needed when IN is 1V to 4V) and can withstand transient voltages up to 60V.

## Features

- ◆ Wide operating input voltage range  $V_{IN}$ : 5V to 40V
- ◆ 60V transient voltage
- ◆ Charge pump gate driver for internal N-channel MOSFET
- ◆ 50ns fast response to current reversal
- ◆ 2A peak gate off current internal
- ◆ Ultra-small  $V_{DS}$  turn-off voltage reduces turn-off time
- ◆ 8-Pin SOP8L

## Applications

## Typical application



Active OR-ing of redundant (N+1) power supplies

## General information

### Ordering information

Part Number	Description
MX5052SL	SOP8L
MPQ	3000pcs

### Package dissipation rating

Package	R $\theta$ JA (°C/W)
SOP8L	108.1

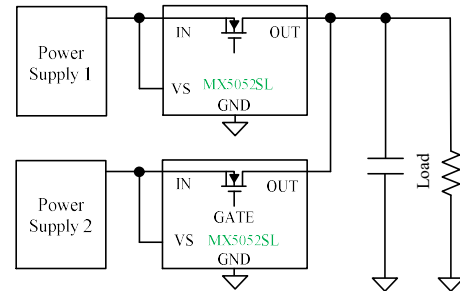
### Absolute maximum ratings

Parameter	Value
IN, OUT Pins to GND	-0.3 to 50V
VS Pin to Ground	-0.3 to 50V
Internal MOSFET VDS	$\geq 60V$
Junction temperature	150°C
Storage temperature, Tstg	-50 to 150°C
Leading temperature (soldering, 10secs)	260°C
ESD Susceptibility HBM	$\pm 2000V$

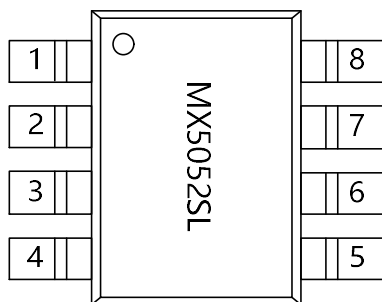
Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

### Recommended operating condition

Symbol	Range
IN, OUT Pins ( $V_S \geq 4.5V$ for $IN < 4V$ )	1-40V
VS Pin	5-40V
Operating temperature	-40~125°C



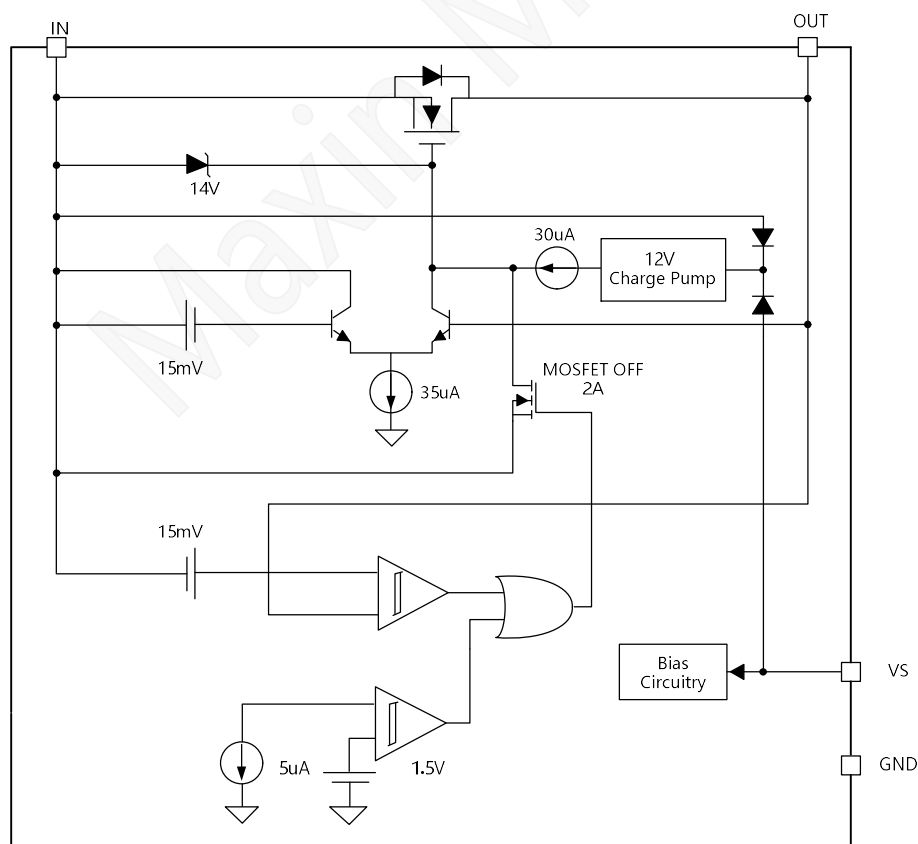
## Terminal assignments



Pin information

PIN NO.	PIN name	Description
1	VS	The main supply pin for all internal biasing and an auxiliary supply for the internal gate drive charge pump. Typically connected to either $V_{OUT}$ or $V_{IN}$ ; a separate supply can also be used.
2	GND	Ground return for the controller
3、4	IN	Voltage sense connection to the external MOSFET source pin.
5~8	OUT	Voltage sense connection to the external MOSFET drain pin.

## Block diagram



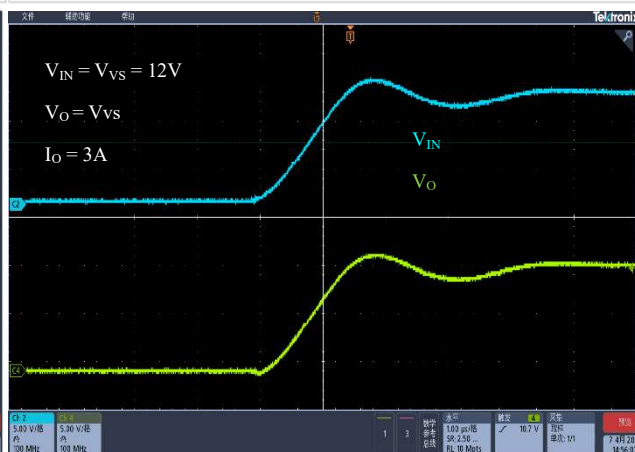
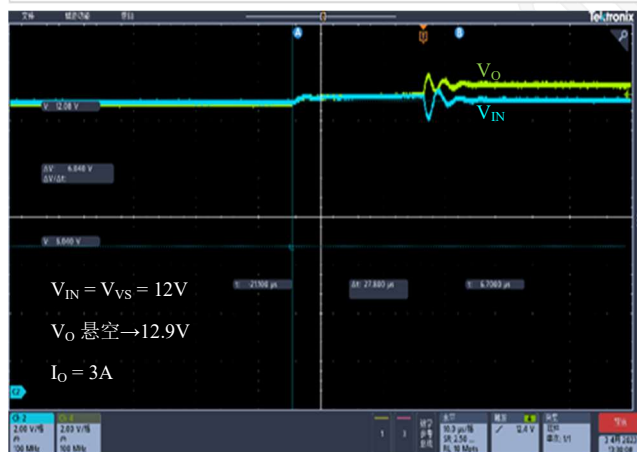
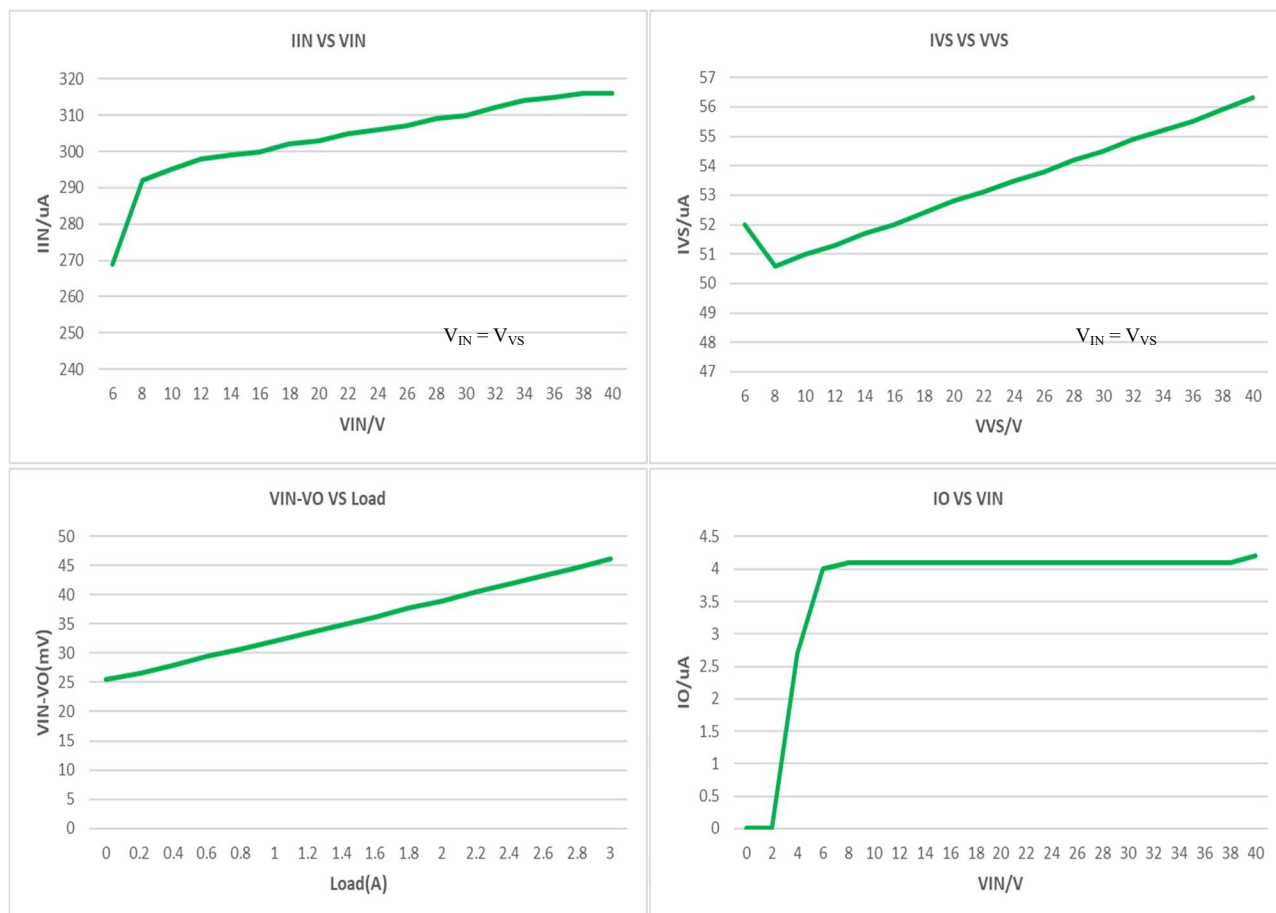
## Electrical characteristics

(  $V_{IN}=12V$ ,  $V_{VS}=V_{IN}$ ,  $T_A=25^{\circ}C$ , unless otherwise noted )

Symbol	Parameter	Test condition	Min	Typ.	Max	Unit
VS PIN						
V <sub>VS</sub>	Operating Supply Voltage Range		5		40	V
I <sub>VS</sub>	Operating Supply Current	V <sub>VS</sub> = 5V, V <sub>IN</sub> = V <sub>VS</sub>		50	70	uA
		V <sub>VS</sub> = 12V, V <sub>IN</sub> = 5V		52	70	
		V <sub>VS</sub> = 40V, V <sub>IN</sub> = 5V		56	100	
IN PIN						
V <sub>IN</sub>	Operating Input Voltage Range		5		40	V
I <sub>IN</sub>	IN Pin current	V <sub>IN</sub> = 5V, V <sub>VS</sub> = V <sub>IN</sub>	150	240	300	uA
		V <sub>IN</sub> = 12V to 40V, V <sub>VS</sub> = V <sub>IN</sub>	200	300	400	
OUT PIN						
V <sub>OUT</sub>	Operating Output Voltage Range		5		40	V
I <sub>OUT</sub>	OUT Pin Current	V <sub>IN</sub> = 5V to 40V, V <sub>VS</sub> = V <sub>IN</sub>		4.1		uA
INTERNAL REGULATOR						
I <sub>GATE(OFF)</sub>	Internal Sink Current	V <sub>GATE</sub> = V <sub>IN</sub> + 3V, V <sub>OUT</sub> > V <sub>IN</sub> + 100mV, t ≤ 10ms		2		A
V <sub>SD(REV)</sub>	Reverse V <sub>SD</sub> Threshold V <sub>IN</sub> < V <sub>OUT</sub>	V <sub>IN</sub> - V <sub>OUT</sub>	-35	-15	-5	mV
V <sub>SD(REG)</sub>	Regulated Forward V <sub>SD</sub> Threshold V <sub>IN</sub> > V <sub>OUT</sub>	V <sub>IN</sub> = 5V, V <sub>VS</sub> = V <sub>IN</sub> , V <sub>IN</sub> - V <sub>OUT</sub>	1	30	40	mV
		V <sub>IN</sub> = 12V, V <sub>VS</sub> = V <sub>IN</sub> , V <sub>IN</sub> - V <sub>OUT</sub>	5	60	80	
INTERNAL MOSFET						
V <sub>DS</sub>	Drain to source voltage	I <sub>DS</sub> = 250uA	60			V
R <sub>ON</sub>	On resistance	I <sub>D</sub> = 1A		8	12	mΩ

## Characteristic plots

( $V_{IN} = V_{VS} = V_{OUT}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted)



## Operation description

### IN and OUT Pins

When power is initially applied, the load current will flow from source to drain through the body diode of the MOSFET. Once the voltage across the body diode exceeds  $V_{SD(REG)}$  then the MX5052SL begins charging the internal MOSFET gate through a 30  $\mu A$  (typical) charge pump current source. In forward operation, the gate of the internal MOSFET is charged. The MX5052SL is designed to regulate the internal MOSFET gate-to-source voltage. If the MOSFET current decreases to the point that the voltage across the MOSFET falls below the  $V_{SD(REG)}$  voltage regulation point of 30mV (typical), the internal MOSFET gate voltage will be decreased until the voltage across the MOSFET is regulated at 30mV. If the source-to-drain voltage is greater than the  $V_{SD(REG)}$  voltage, the gate-to-source voltage will increase and eventually reach the 12V gate to IN pin Zener clamp level.

If the MOSFET current reverses, possibly due to failure of the input supply, such that the voltage across the MX5052SL IN and OUT pins is more negative than the  $V_{SD(REV)}$  voltage of -28mV (typical), the MX5052SL will quickly discharge the internal MOSFET gate through a strong gate to IN pin discharge transistor. If the input supply fails abruptly, as would occur if the supply was shorted directly to ground, a reverse current will temporarily flow through the MOSFET until the gate can be fully discharged. This reverse current is sourced from the load capacitance and from the parallel connected supplies. The MX5052SL responds to a voltage reversal condition typically within 50ns. The actual time required to turn off the MOSFET will depend on the charge held by the gate capacitance of the MOSFET being used. For MX5052SL, the gate capacitance of the internal MOSFET is 4.6nF and the typical turn off time is 25ns. This fast turnoff time minimizes voltage disturbances at the output, as well as the current transients from the redundant supplies.

### VS Pin

The VS pin of MX5052SL is the main supply pin for all internal biasing and an auxiliary supply for the internal gate drive charge pump.

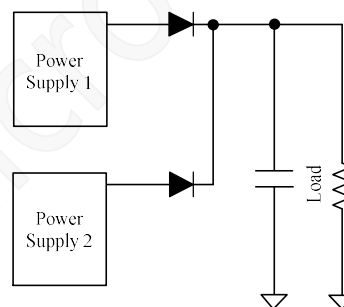
For typical MX5052SL applications, the VS pin can be connected directly to the OUT pin. The capacitor value should be the lowest value that produces acceptable filtering of the

voltage noise.

## Application and Implementation

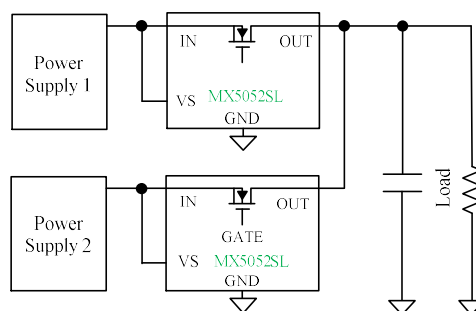
### Application Information

Systems that require high availability often use multiple, parallel-connected redundant power supplies to improve reliability. Schottky OR-ing diodes are typically used to connect these redundant power supplies to a common point at the load. The disadvantage of using OR-ing diodes is the forward voltage drop, which reduces the available voltage and the associated power losses as load currents increase. Using an N-channel MOSFET to replace the OR-ing diode requires a small increase in the level of complexity, but reduces, or eliminates, the need for diode heat sinks or large thermal copper area in circuit board layouts for high power applications.



OR-ing with Diodes

The MX5052SL is a positive voltage (that is, high-side) OR-ing controller that will drive an external N-channel MOSFET to replace an OR-ing diode. The voltage across the MOSFET source and drain pins is monitored by the MX5052SL at the IN and OUT pins, while the internal MOSFET gate drives the MOSFET to control its operation based on the monitored source-drain voltage. The resulting behavior is that of an ideal rectifier with source and drain pins of the MOSFET acting as the anode and cathode pins of a diode respectively.



OR-ing with internal MOSFETs

### Short Circuit Failure of an Input Supply

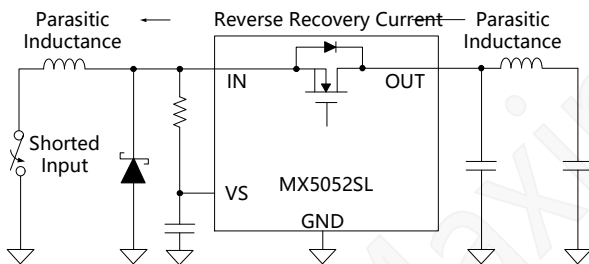
An abrupt  $0\Omega$  short circuit across the input supply will cause the highest possible reverse current to flow while the internal MX5052SL control circuitry discharges the gate of the MOSFET. During this time, the reverse current is limited only by the  $R_{DS(ON)}$  of the MOSFET, along with parasitic wiring resistances and inductances. Worst case instantaneous reverse current would be limited to:

$$I_{D(REV)} = (V_{OUT} - V_{IN}) / R_{DS(ON)} \quad (1)$$

The internal Reverse Comparator will react, and will start the process of discharging the internal MOSFET gate, when the reverse current reaches:

$$I_{D(REV)} = V_{SD(REV)} / R_{DS(ON)} \quad (2)$$

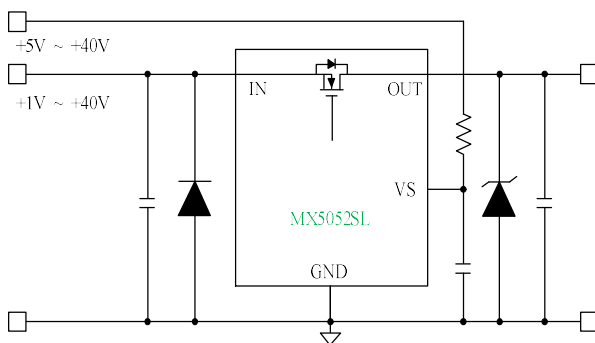
When the MOSFET is finally switched off, the energy stored in the parasitic wiring inductances will be transferred to the rest of the circuit. As a result, the MX5052SL IN pin will see a negative voltage spike while the OUT pin will see a positive voltage spike. The IN pin can be protected by diode clamping the pin to GND in the negative direction. The OUT pin can be protected with a TVS protection diode, a local bypass capacitor, or both.



Reverse Recovery Current Generates Spikes at  $V_{IN}$  and  $V_{OUT}$

### A Separate VS Supply for Low $V_{IN}$ Operation

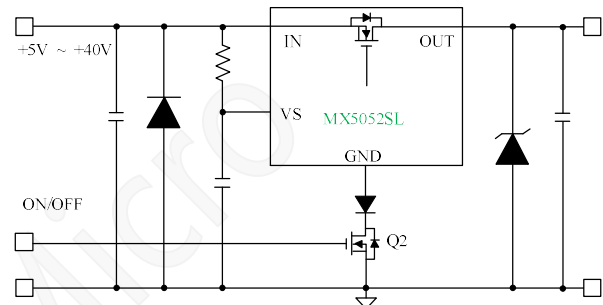
In some applications, it is desired to operate MX5052SL from low supply voltage. The MX5052SL can operate with a 1V rail voltage, provides its VS pin is biased from 5V to 40V. The detail of such application is depicted in the following figure.



### Reverse Input Voltage Protection with IQ Reduction

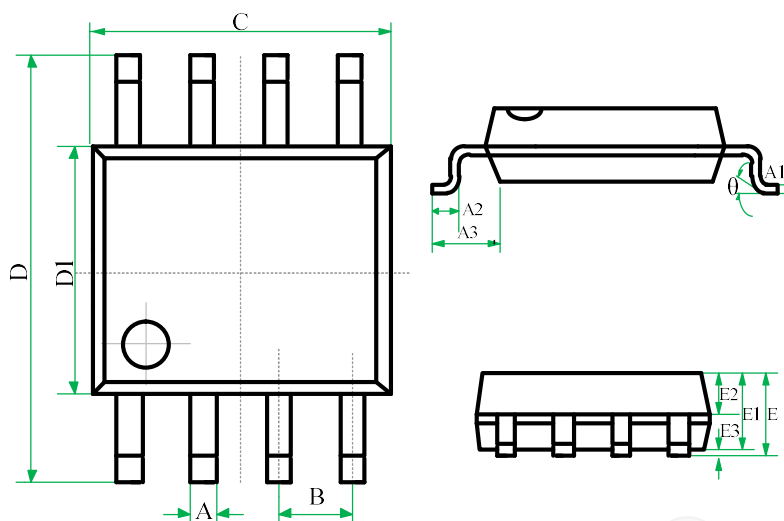
If VS is powered while IN is floating or grounded, then about 0.5mA will leak from the VS pin into the IC and about 3mA will leak from the OUT pin into the IC. From this leakage, about 0.05mA will flow out of the IN pin and the rest will flow to ground. This does not affect long term reliability of the IC but may influence circuit design.

In battery powered applications, whenever MX5052SL functionality is not needed, the supply to the MX5052SL can be disconnected by turning off Q2, as shown in the following figure. This disconnects to the ground path of the MX5052SL and eliminates the current leakage from the battery.



Reverse input voltage protection with IQ reduction schematic

## Package information



SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.39	-	0.48	0.0154	-	0.0189
A1	0.21	-	0.28	0.008	-	0.011
A2	0.50	-	0.80	0.020	-	0.031
A3	1.05BSC			0.041BSC		
B	1.27BSC			0.050BSC		
C	4.70	4.90	5.10	0.185	0.193	0.201
D	5.80	6.00	6.20	0.228	0.236	0.244
D1	3.70	3.90	4.10	0.146	0.154	0.161
E	-	-	1.75	-	-	0.069
E1	1.30	1.40	1.50	0.051	0.055	0.059
E2	0.60	0.65	0.70	0.024	0.026	0.028
E3	0.10	-	0.225	0.004	-	0.009
θ	0	-	8°	0	-	8°

SOP8 for MX5052SL

## Restrictions on Product Use

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Version update record:

V11 The original version

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