2A, 3MHz High Efficiency Step-Down Converter in DFN2x2-8L Package

DESCRIPTION

The ETA3410 is a high-efficiency, DC-to-DC step-down switching regulator, capable of delivering up to 2A of output current. The devices operate from an input voltage range of 2.6V to 5.5V and provide output voltages from 0.6V to VIN, making the ETA3410 ideal for low voltage power conversions. Running at a fixed frequency of 3MHz allows the use of small inductance value and low DCR inductors, thereby achieving higher efficiencies. Other external components, such as ceramic input and output caps, can also be small due to higher switching frequency, while maintaining exceptional low noise output voltages. Built-in EMI reduction circuitry makes this converter ideal power supply for RF applications. Internal soft-start control circuitry reduces inrush current. Short-circuit and thermal-overload protection improves design reliability.

ETA3410 is housed in a tiny DFN2x2-8L package

FEATURES

- Up to 96% Efficiency
- Up to 2A Max Output Current
- 3MHz Frequency
- Internal Compensation
- Clock Dithering
- Tiny DFN2x2-8L Package

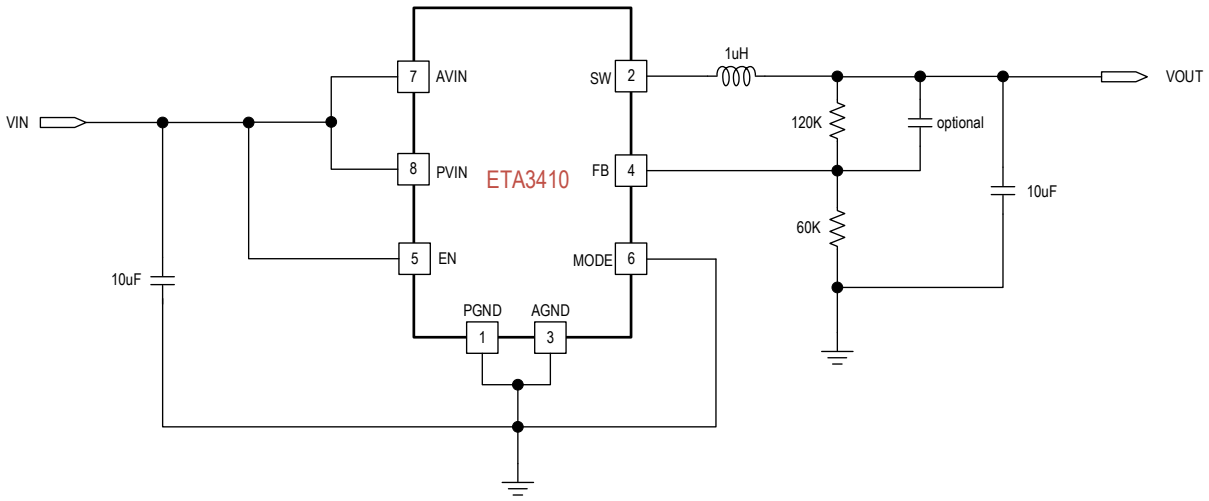
APPLICATIONS

- USB ports/Hubs
- Hot Swaps
- Cellphones
- Tablet PC
- Set Top Boxes

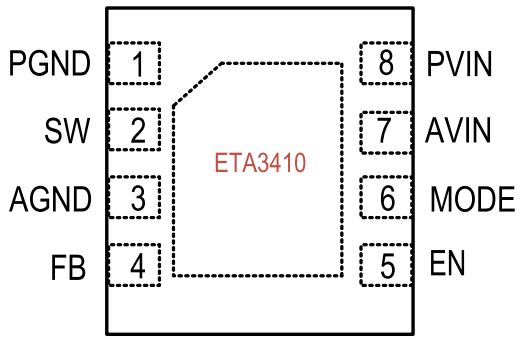
ORDERING INFORMATION

PART	PACKAGE PIN	TOP MARK
ETA3410D2I	DFN2x2-8	CEYW Date Code Product Number

TYPICAL APPLICATION



PIN CONFIGURATION



DFN2 x 2 - 8

ABSOLUTE MAXIMUM RATINGS

(Note: Exceeding these limits may damage the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.)

PVIN, AVIN,SW,FB,EN,MODE Voltage.....-0.3V to 6V
SW to ground current.....Internally limited
Maximum Power Dissipation.....1300mW
Operating Temperature Range .....–40°C to 85°C
Storage Temperature Range .....–55°C to 150°C

Thermal Resistance	θ_{JC}	θ_{JA}
DFN2X2-8	20	75 °C/W

Lead Temperature (Soldering 10sec) .....260°C
ESD HBM (Human Body Mode) 2KV
ESD MM (Machine Mode) 200V

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.6V, unless otherwise specified. Typical values are at TA = 25°C.)

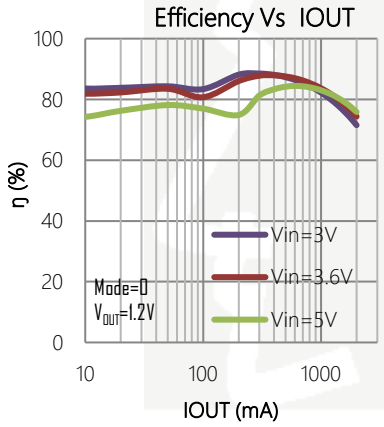
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range		2.6		5.5	V
Input UVLO	Rising, Hysteresis=200mV		2.1		V
Input Supply Current	V_{FB} =0.65V,MODE=GND		30		μA
Input Shutdown Current			0.1	1	μA
FB Feedback Voltage	V_{IN} =2.5 to 5.5V	0.588	0.6	0.612	V
FB Input Current			0.01		μA
Output Voltage Range		0.6		V_{IN}	V
Load Regulation			0.15		%/A
Line Regulation	V_{IN} =2.7 to 5.5V		0.04		%/V
Switching Frequency		2.4	3	3.6	MHz
NMOS Switch On Resistance	I_{SW} =200mA		100	150	mΩ
PMOS Switch On Resistance	I_{SW} =200mA		80	120	mΩ
PMOS Switch Current Limit		2.5	3		A
SW Leakage Current	V_{OUT}=5.5V,V_{SW}=0 or 5.5V,EN= GND			10	μA
EN, MODE Input Current	EN=MODE=GND			1	μA
EN,MODE Input Low Voltage				0.4	V
EN,MODE Input High Voltage (Rising)		1.05			V
EN,MODE Input High Voltage (Falling)		0.95			V
Thermal Shutdown	Rising, Hysteresis =15°C		160		°C

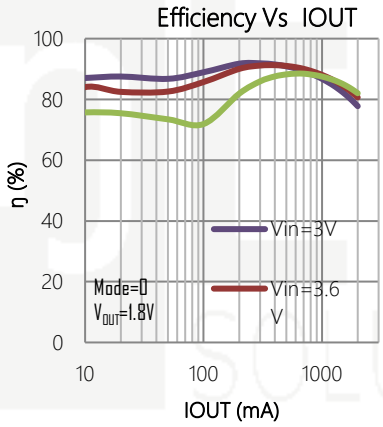
PIN DESCRIPTION

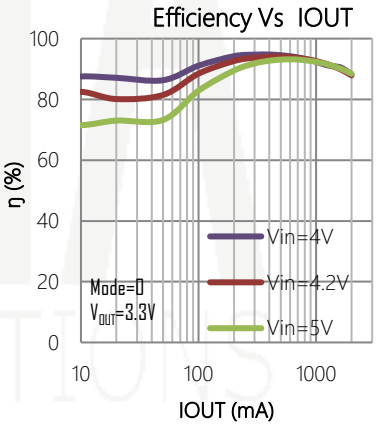
PIN #	NAME	DESCRIPTION
1	PGND	Power Ground. Bypass with a 10μF ceramic capacitor to PVIN
2	SW	Inductor Connection. Connect an inductor Between SW and the regulator output.
3	AGND	Analog Ground, Connect to PGND
4	FB	Feedback Input. Connect an external resistor divider from the output to FB and GND to set the output to a voltage between 0.6V and VIN
5	EN	Enable pin for the IC. Drive this pin to high to enable the part, low to disable.
6	MODE	When forced high, the device operates in fixed frequency PWM mode. When forced low, it enables the Power Save Mode with automatic transition from PFM mode to fixed frequency PWM mode. This pin must be terminated.
7	AVIN	Analog Power. Short externally to PVIN
8	PVIN	Supply Voltage. Bypass with a 10μF ceramic capacitor to PGND

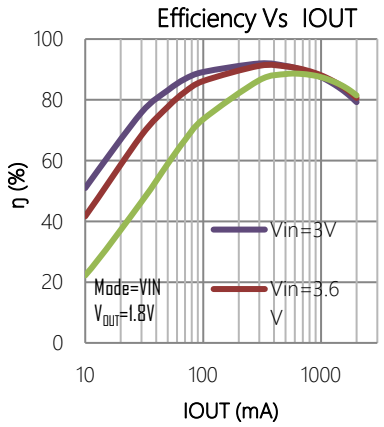
TYPICAL CHARACTERISTICS

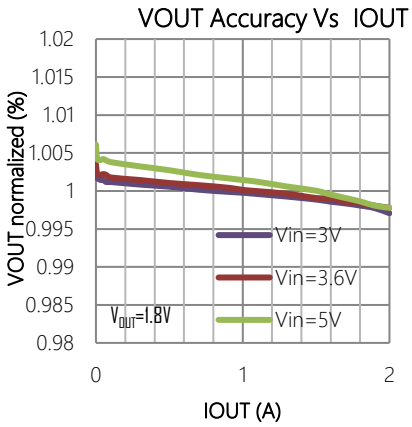
(Typical values are at TA = 25°C unless otherwise specified.)

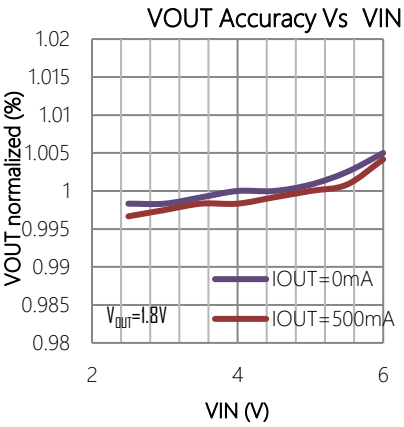








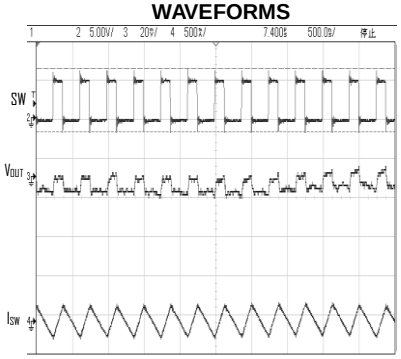




TYPICAL CHARACTERISTICS

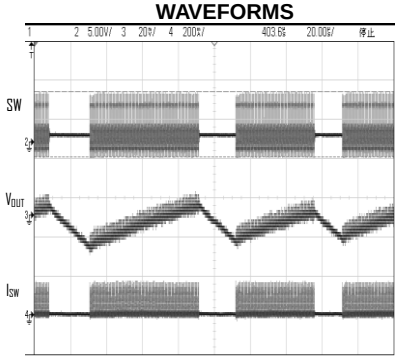
(Typical values are at TA = 25°C unless otherwise specified.)

SWITCHING WAVEFORMS



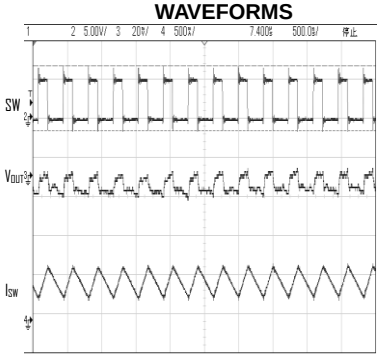
500nS/Div

SWITCHING WAVEFORMS



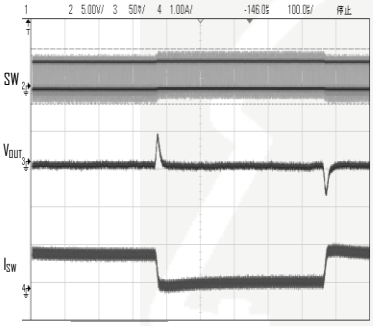
500nS/Div

SWITCHING WAVEFORMS



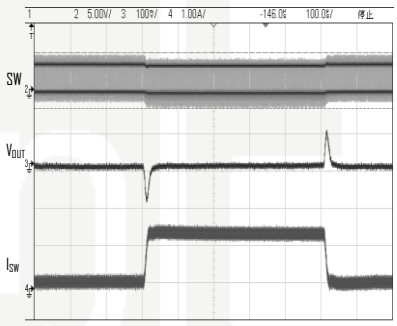
500nS/Div

Load Transient VOUT=1.2V 0.2A to 1.0A



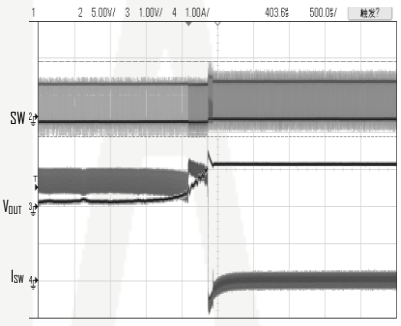
100μS/Div

Load Transient VOUT=1.8V 0.2A to 1.5A



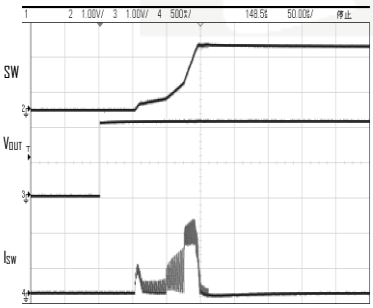
100μS/Div

Short-Circuit Recovery



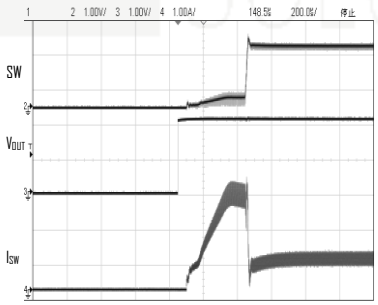
500μS/Div

Start-Up Waveform No Load



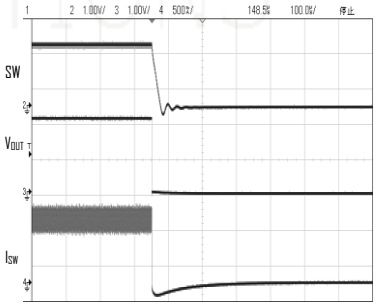
50μS/Div

Start-Up Waveform IOUT=1A



200μS/Div

Shutdown Waveform IOUT=1A



100μS/Div

FUNCTION DESCRIPTION

The ETA3410 high efficiency switching regulator is a small, simple, DC-to-DC step-down converter capable of delivering up to 2A of output current. The device operates in pulse-width modulation (PWM) at 3MHz from a 2.6V to 5.5V input voltage and provides an output voltage from 0.6V to VIN, making the ETA3410 ideal for on-board post-regulation applications. An internal synchronous rectifier improves efficiency and eliminates the typical Schottky free-wheeling diode. Using the on resistance of the internal high-side MOSFET to sense switching currents eliminates current-sense resistors, further improving efficiency and cost.

Loop Operation

ETA3410 uses a PWM current-mode control scheme. An open-loop comparator compares the integrated voltage-feedback signal against the sum of the amplified current-sense signal and the slope compensation ramp. At each rising edge of the internal clock, the internal high-side MOSFET turns on until the PWM comparator terminates the on cycle. During this on-time, current ramps up through the inductor, sourcing current to the output and storing energy in the inductor. The current mode feedback system regulates the peak inductor current as a function of the output voltage error signal. During the off cycle, the internal high-side P-channel MOSFET turns off, and the internal low-side N-channel MOSFET turns on. The inductor releases the stored energy as its current ramps down while still providing current to the output.

Current Sense

An internal current-sense amplifier senses the current through the high-side MOSFET during on time and produces a proportional current signal, which is used to sum with the slope compensation signal. The summed signal then is compared with the error amplifier output by the PWM comparator to terminate the on cycle.

Current Limit

There is a cycle-by-cycle current limit on the high-side MOSFET. When the current flowing out of SW exceeds this limit, the high-side MOSFET turns off and the synchronous rectifier turns on. ETA3410 utilizes a frequency fold-back mode to prevent overheating during short-circuit output conditions. The device enters frequency fold-back mode when the FB voltage drops below 200mV, limiting the current to I_{PEAK} and reducing power dissipation. Normal operation resumes upon removal of the short-circuit condition.

Soft-start

ETA3410 has a internal soft-start circuitry to reduce supply inrush current during startup conditions. When the device exits under-voltage lockout (UVLO), shutdown mode, or restarts following a thermal-overload event, the I soft-start circuitry slowly ramps up current available at SW.

UVLO and Thermal Shutdown

If PVIN/AVIN drops below 1.9V, the UVLO circuit inhibits switching. Once PVIN/AVIN rises above 2.1V, the UVLO clears, and the soft-start sequence activates. Thermal-overload protection limits total power dissipation in the device. When the junction temperature exceeds TJ= +160°C, a thermal sensor forces the device into shutdown, allowing the die to cool. The thermal sensor turns the device on again after the junction temperature cools by 15°C, resulting in a pulsed output during continuous overload conditions. Following a thermal-shutdown condition, the soft-start sequence begins.

Design Procedure

Setting Output Voltages

Output voltages are set by external resistors. The FB threshold is 0.6V.

$R_{TOP} = R_{BOTTOM} \times [(V_{OUT} / 0.6) - 1]$

Inductor Selection

The peak-to-peak ripple is limited to 30% of the maximum output current. This places the peak current far enough from the minimum overcurrent trip level to ensure reliable operation while providing enough current ripples for the current mode converter to operate stably. In this case, for 2A maximum output current, the maximum inductor ripple current is 667 mA. The inductor size is estimated as following equation:

$L_{IDEAL}=(V_{IN(MAX)}-V_{OUT})/I_{RIPPLE}*D_{MIN}*(1/F_{OSC})$

Therefore, for V_{OUT}=1.8V,

The inductor values is calculated to be L = 0.60μH.

Chose 1μH

For V_{OUT} =1.2V,

The inductor values is calculated to be L = 0.469μH.

Chose 0.47μH

The resulting ripple is

$I_{RIPPLE} =(V_{IN(MAX)}-V_{OUT})/L_{ACTUAL}*D_{MIN}*(1/F_{OSC})$

When,

V_{OUT}=1.8V, I_{RIPPLE} = 403mA

V_{OUT}=1.2V, I_{RIPPLE} = 665mA

Output Capacitor Selection

For most applications a nominal 10μF or 22μF capacitor is suitable. The ETA3410 internal compensation is designed for a fixed corner frequency that is equal to

$FC=\frac{1}{2*\pi\sqrt{COUT*L}}$ = 50Khz

For example, for V_{OUT}=1.8V, L=1μH, C_{OUT}=10μF, for V_{OUT} =1.2V, L=0.47μH, C_{OUT}=22μF

The output capacitor keeps output ripple small and ensures control-loop stability. The output capacitor must also have low impedance at the switching frequency. Ceramic, polymer, and tantalum capacitors are suitable, with ceramic exhibiting the lowest ESR and high-frequency impedance. Output ripple with a ceramic output capacitor is approximately as follows:

$V_{RIPPLE} = IL_{(PEAK)}[1 / (2\pi \times f_{OSC} \times C_{OUT})]$

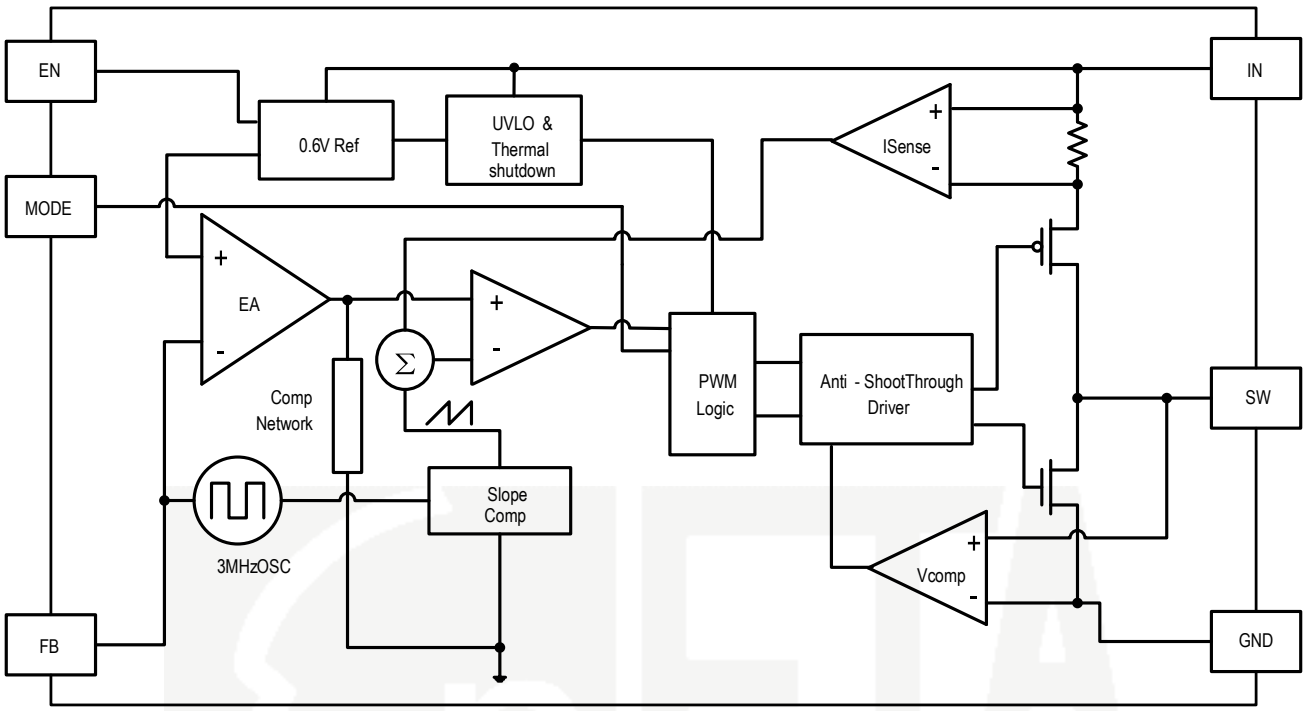
If the capacitor has significant ESR, the output ripple component due to capacitor ESR is as follows:

$V_{RIPPLE(ESR)} = IL_{(PEAK)} \times ESR$

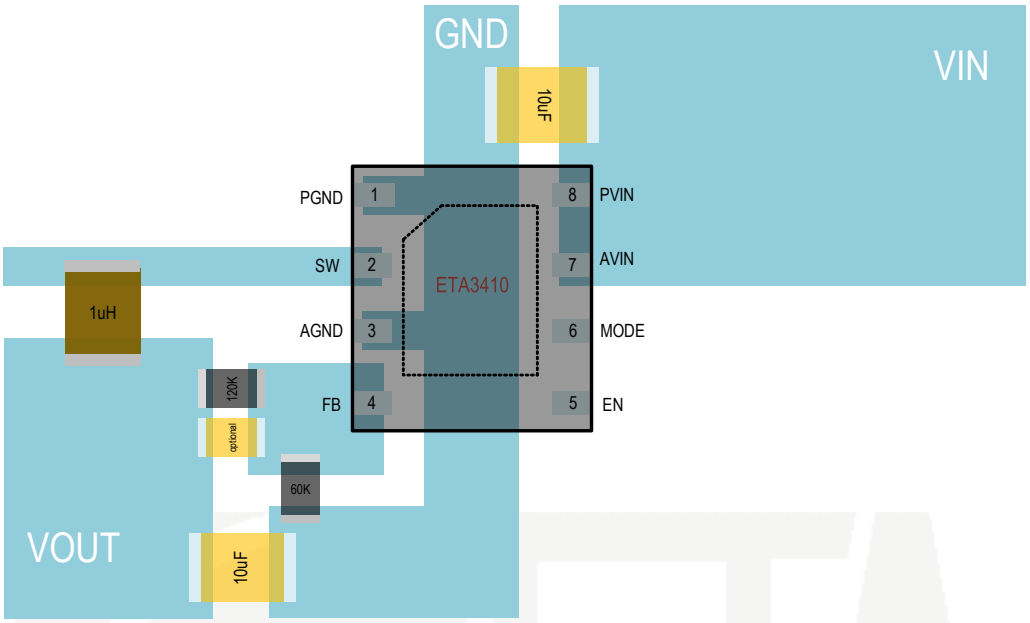
Input Capacitor Selection

The input capacitor in a DC-to-DC converter reduces current peaks drawn from the battery or other input power source and reduces switching noise in the controller. The impedance of the input capacitor at the switching frequency should be less than that of the input source so high-frequency switching currents do not pass through the input source. The output capacitor keeps output ripple small and ensures control-loop stability.

BLOCK DIAGRAM

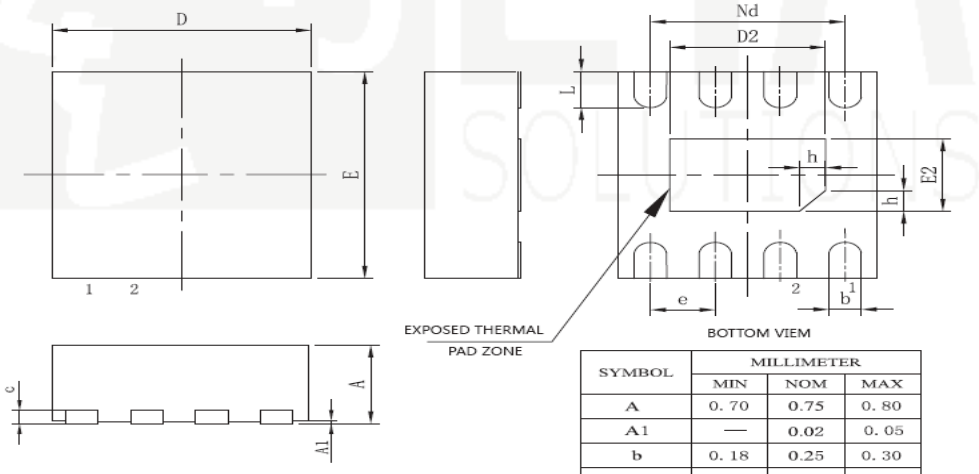


PCB LAYOUT



PACKAGE OUTLINE

DFN2X2-8L PACKAGE OUTLINE AND DIMENSIONS



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0. 70	0.75	0. 80
A1	—	0.02	0. 05
b	0. 18	0.25	0. 30
c	0. 18	0.20	0. 25
D	1. 90	2. 00	2. 10
D2	1. 10	1. 20	1. 30
e	0. 50BSC		
Nd	1. 50BSC		
E	1. 90	2. 00	2. 10
E2	0. 60	0. 70	0. 80
L	0. 30	0.35	0. 40
h	0. 15	0. 20	0. 25
载体尺寸（mil）	63X39		