Features

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

Product Summary

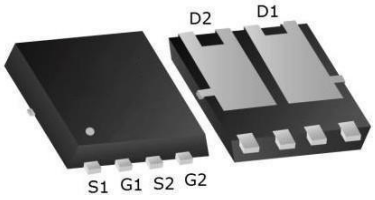
Green

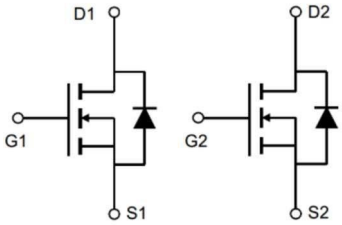
BVDSS	RDSON	ID
60V	16mΩ	20A

Applications

- DC-DC Converters
- Power management functions
- Synchronous-rectification applications

PDFN3333-8L Pin Configuration





Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_C=25℃	Continuous Drain Current, V_{GS} @ 10V[1,6]	20	A
I_D@T_C=100℃	Continuous Drain Current, V_{GS} @ 10V[1,6]	14	A
I_{DM}	Pulsed Drain Current[2]	100	A
EAS	Single Pulse Avalanche Energy[3]	33.8	mJ
I_{AS}	Avalanche Current	11	A
P_D@T_C=25℃	Total Power Dissipation[4]	30	W
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient [1]	---	---	℃/W
$R_{\theta JC}$	Thermal Resistance Junction-Case[1]	---	4.1	℃/W

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250uA	60	---	---	V
△BV_{DSS}/△T_J	BV_{DSS} Temperature Coefficient	Reference to 25℃ , I_D=1mA	---	---	---	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V , I_D=4.9A	---	16	21	mΩ
		V_{GS}=4.5V , I_D=3.4A	---	19	26	
		V_{GS}=2.5V , I_D=2A	---	---	---	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =-250uA	-0.4	---	-1.0	V
△$V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	3.95	---	mV/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=60V , V_{GS}=0V , T_J=25℃	---	---	1	uA
		V_{DS}=60V , V_{GS}=0V , T_J=55℃	---	---	5	
I_{GSS}	Gate-Source Leakage Current	V_{GS}= ±20V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=30V , I_D=10A	---	---	---	S
Q_g	Total Gate Charge	V_{DS}=30V , V_{GS}=10V , I_D=20A	---	12.1	---	nC
Q_{gs}	Gate-Source Charge		---	1.3	---	
Q_{gd}	Gate-Drain Charge		---	2.6	---	
$T_{d(on)}$	Turn-On Delay Time	V_{DD}=30V , V_{GS}=10V , R_G=6Ω , I_D=20A	---	3.3	---	ns
T_r	Rise Time		---	4	---	
$T_{d(off)}$	Turn-Off Delay Time		---	14	---	
T_f	Fall Time		---	5.5	---	
C_{iss}	Input Capacitance	V_{DS}=25V , V_{GS}=0V , f=1MHz	---	500	---	pF
C_{oss}	Output Capacitance		---	204	---	
C_{rss}	Reverse Transfer Capacitance		---	6.8	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current[1,4]	V_G=V_D=0V , Force Current	---	---	20	A
I_{SM}	Pulsed Source Current[2,4]		---	---	100	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V , I_S=1A , T_J=25℃	---	---	1.2	V
t_{rr}	Reverse Recovery Time	IF=15A , di/dt=100A/μs , T_J=25℃	---	20	---	nS
Q_{rr}	Reverse Recovery Charge		---	8.1	---	nC

Note :

1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.

2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3.The EAS data shows Max. rating . The test condition is TJ = 25℃,VDD=30V,VGS=10V,L=0.5mH,IAS=11A.

4.The power dissipation is limited by 150℃ junction temperature

5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

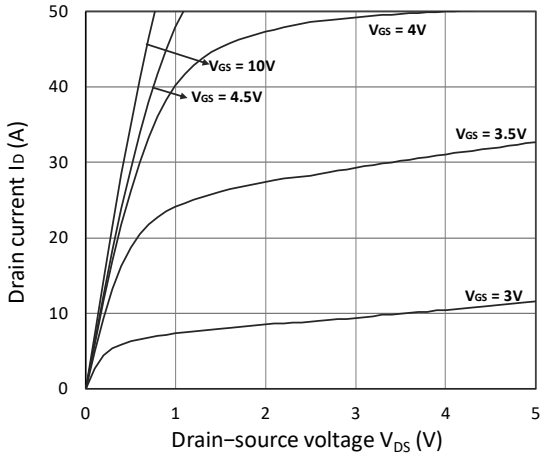


Figure 1. Output Characteristics

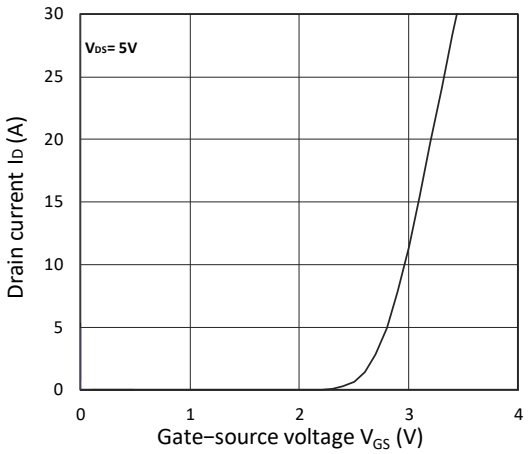


Figure 2. Transfer Characteristics

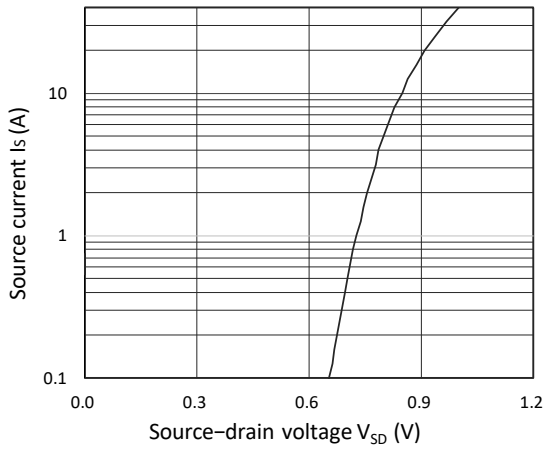


Figure 3. Forward Characteristics of Reverse

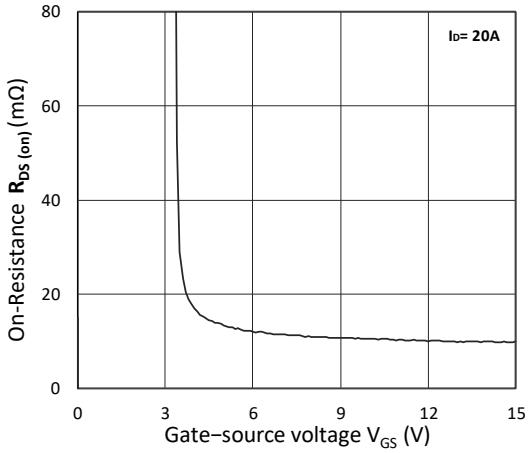


Figure 4. $R_{DS(ON)}$ vs. V_{GS}

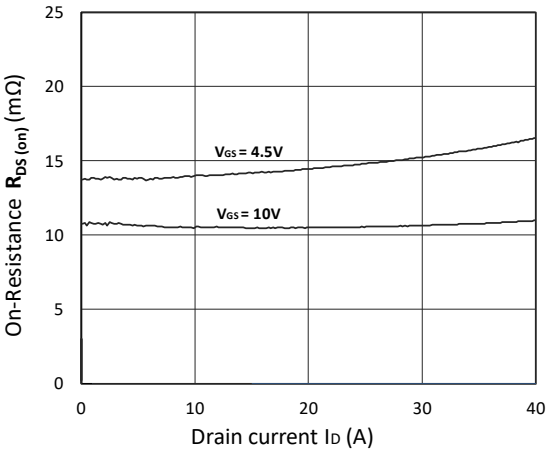


Figure 5. $R_{DS(ON)}$ vs. I_D

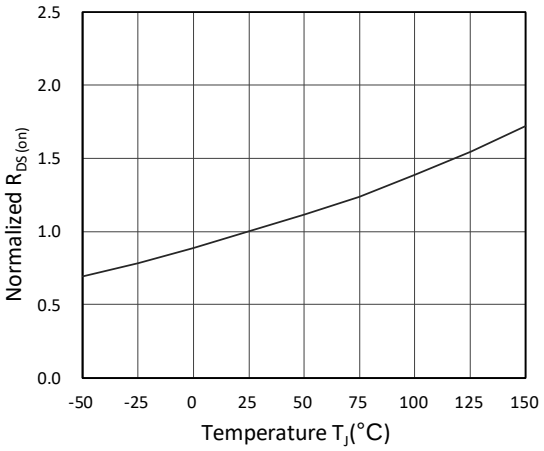


Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

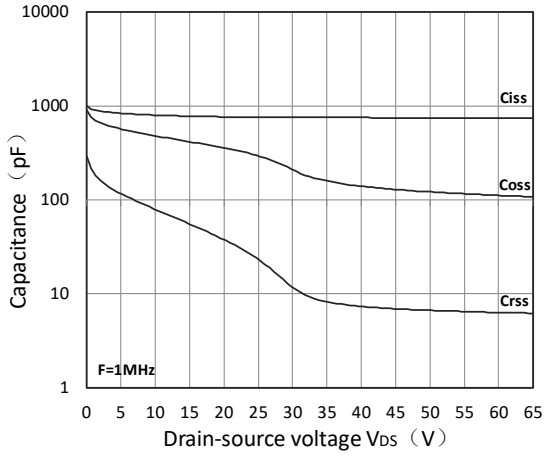


Figure 7. Capacitance Characteristics

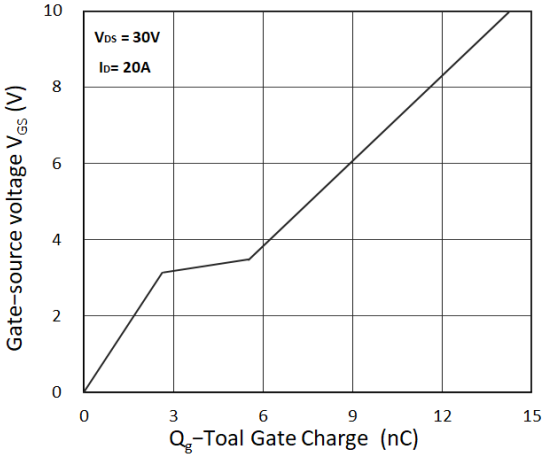


Figure 8. Gate Charge Characteristics

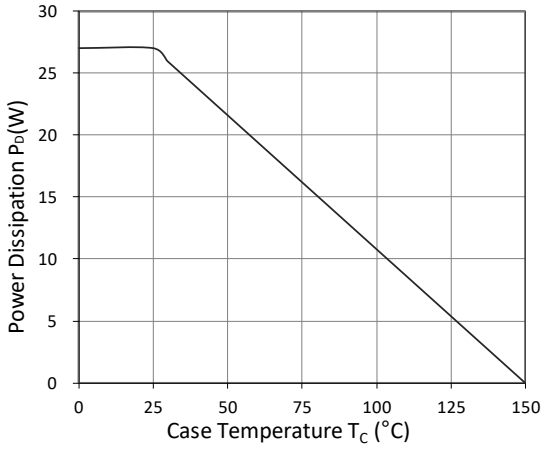


Figure 9. Power Dissipation

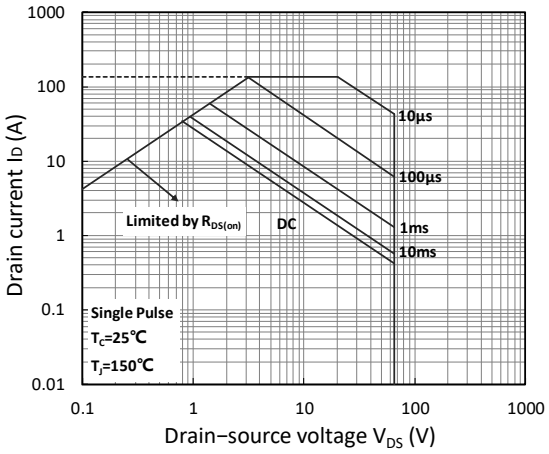


Figure10. Safe Operating Area

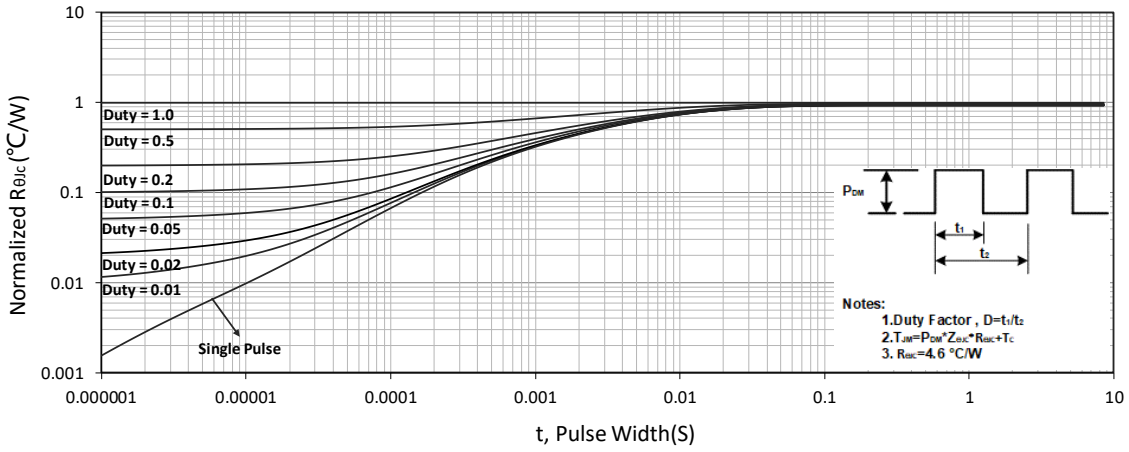
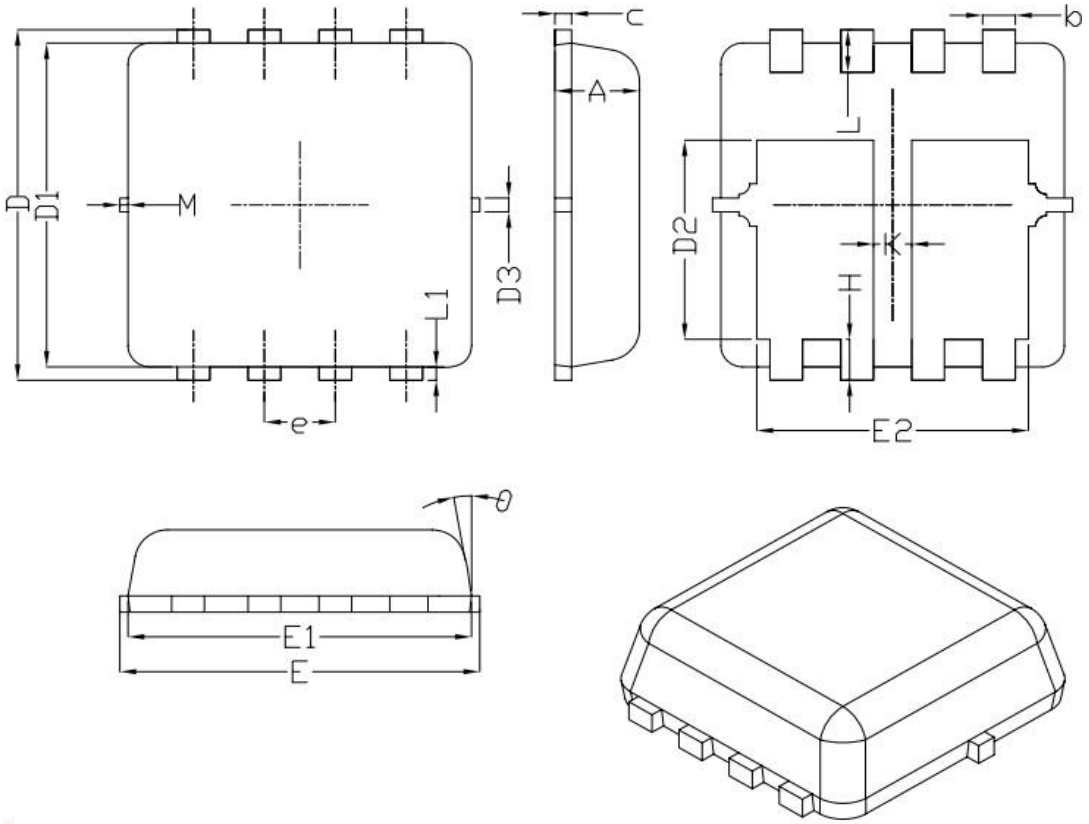


Figure 11. Normalized Maximum Transient Thermal Impedance

Dual PDFN3333-8L Package Outline Data



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.78	1.88	1.98
D3	--	0.13	--
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65 BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	--	0.13	--
K	0.30	--	--
θ	--	10°	12°
M	*	*	0.15
* Not Specified			

Notes:
1. Refer to JEDEC MO-240 variation CA.
2. Dimensions "D1" and "E1" do NOT include mold flash protrusions or gate burrs.
3. Dimensions "D1" and "E1" include interterminal flash or protrusion.