PL2303GL
8-Pin USB to UART Bridge Controller IC

USB Interface

- Fully Compliant with USB 2.0 specification (Full-Speed Mode).
- USB-IF certified (USB logo compliant) with TID 40001839.
- UHCI/OHCI (USB 1.1), EHCI (USB 2.0), xHCI (USB 3.1) Host Controller Compatible.
- Provides royalty-free USB to Virtual Com Port (VCP) drivers for Windows, Mac, Linux, and Android.
- Highly integrated USB 1.1 FS Transceiver. Integrated termination resistors and pull-up resistor to reduce PCB external components.
- Supports OTPROM (One-Time Programmable ROM) for USB device descriptors. OTPROM can be programmed directly through USB port.
- Each IC has unique ID (for Serial Number).
- Supports bus-power, self-power and high-power USB device configuration.
- Supports Windows USB Selective Suspend.
- Supports 3.3V VBUS voltage operation.

UART Interface

- Full-duplex transmitter/receiver (TXD/RXD):
  - Flexible baud rate support from 1bps to 115200bps
  - 5, 6, 7 or 8 data bits
  - Odd, Even, Mark, Space, None parity mode
  - One, one and a half, or two stop bits
  - Software Flow Control (XON/XOFF)
- 1024-byte bi-directional data FIFO buffers (768-byte receive/256-byte transmit) for faster data throughput.

Miscellaneous

- Integrated precise self-generated clock generator. No external crystal required.
- Integrated Power-on-Reset (POR) circuit.
- Integrated 5V to 3.3V LDO that can support 80mA for external components.
- Low operating power and USB suspend current.
- Wide I/O voltage range (1.8V/2.5V/3.3V/5V).
- -40ºC to 85ºC Operating Temperature.
- Small footprint 8-pin SOP packages.
- Pin-compatible with PL2303SA chip (SOP8).

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Website：http://www.prolific.com.tw/

REVISION HISTORY

Revision	Description	Date
1.0.2	➢ To remove and add the supported OS of SDK -removed OS: Win 2000, Vista, XP, Server 2003, 2008 ➢ To add 12.1 Chip Marking information	2020/9/7
1.0.1	➢ Added “supply the additional 80mA for external components” into the sections of 8.2 LDO Regulator and 10.1 USB Bus Powered Design.	2020/5/29
1.0.0	➢ Formal release	2020/3/13

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1. Product Applications

- Single-chip upgrade solution for Legacy RS232 devices to USB interface
- MCU-based devices to USB host interface
- Healthcare/Medical USB Interface Data Transfer Cable
- Cellular/PDA USB Interface Data Transfer Cable
- GPS/Navigation USB Interface
- Industrial / Instrumentation / Automation Control USB Interface
- USB Wireless / Zigbee USB Interface

2. Royalty-Free Driver Support

- Windows 10, 8, 7 (Microsoft Certified WHQL Drivers)
  - Windows Update Driver installation available in Windows 7 and above (32/64-bit)
- Windows Server 2008 R2, 2012, 2016, 2019
- Windows Embedded Industry, Point-of-Service (WEPOS), POSReady
- Windows Embedded Compact, Windows Embedded CE, Windows CE
- Mac OS X
- Linux OS
- Android 3.2 and above

3. Ordering Information

Chip Product Name	Package Type	Ordering Part Number	MPQ
PL2303GL	8-pin SOP (Lead Free)	PL2303G4PEG7P1	100pcs / tube
		PL2303G4PEG8P1	2500pcs / reel

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4. Block Diagram

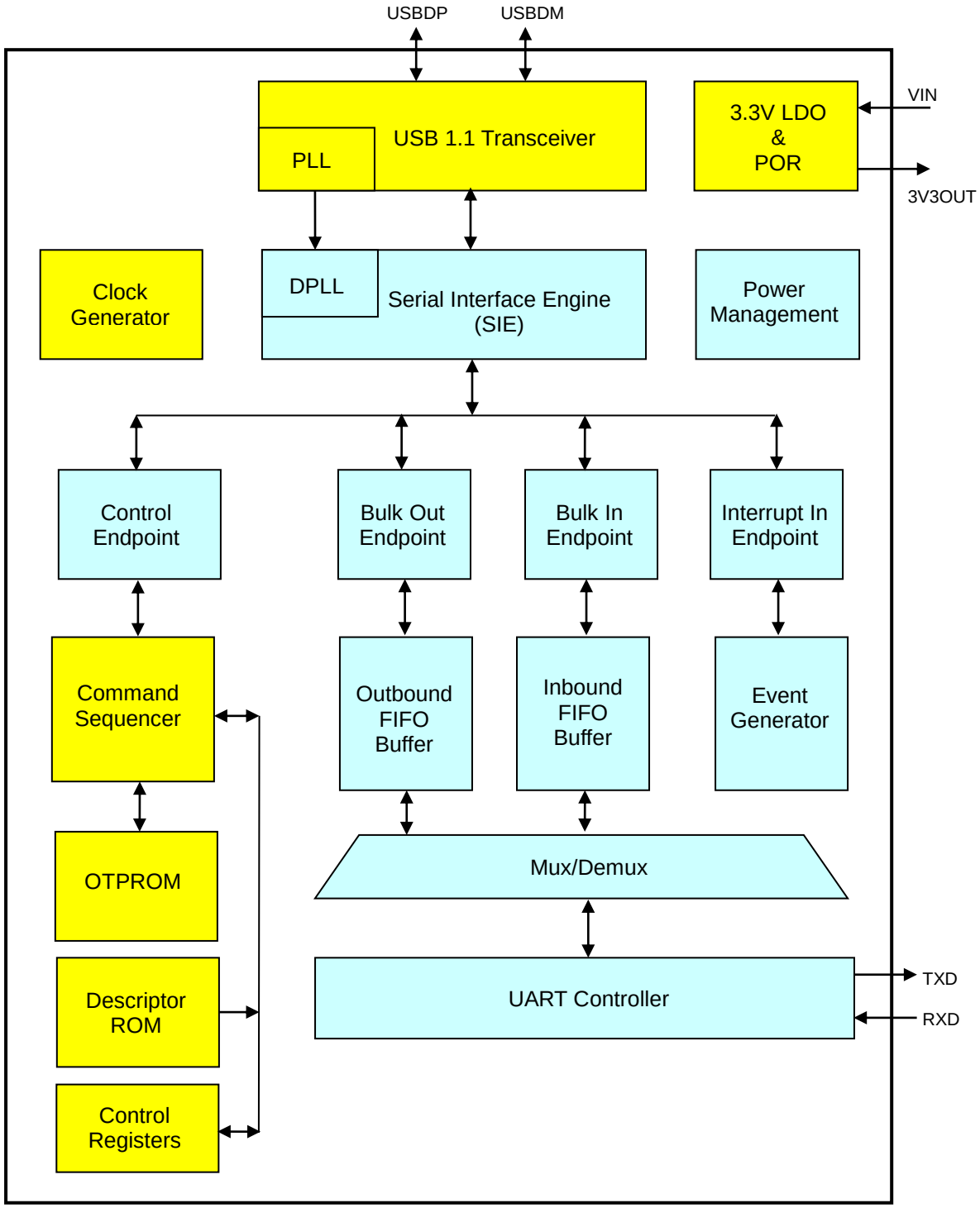

Figure 4-1 PL2303GL Block Diagram

5. USB Logo Certification

The PL2303GL IC has been certified by the USB-IF organization with TID 40001839 to be fully compliant with the USB 2.0 specification.

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6. Overview

The new PL2303GL chip is one of the latest G-Series IC product added to the popular PL2303 USB to Serial (UART) Bridge Controller family, replacing the PL2303SA SOP8 small footprint chip. It provides an advanced full-featured single-chip bridge solution for connecting a full-duplex UART asynchronous serial interface device (TX-RX only) to any Universal Serial Bus (USB) capable host. The PL2303GL provides highly compatible USB drivers to simulate the traditional COM port (via virtual COM Port) on most operating systems allowing existing serial UART applications based on legacy COM port to easily migrate.

The new PL2303GL (SOP8) is pin-to-pin compatible with the previous PL2303SA chip. It also integrates an internal precise clock generator (no external crystal required), USB 1.1 transceiver, Serial Interface Engine (SIE), LDO voltage regulator, power-on- reset (POR), FIFO data buffers, and OTPROM.

The PL2303GL added several new features and enhancements:

- Integrated termination resistors and pull-up resistor to reduce PCB external components.
- New USB drivers for different OS platforms with faster performance and advanced features.
- Precise baud rate generator (up to 115200bps).
- OTPROM can be programmed directly through USB (no high voltage generator required).
- Larger TX/RX FIFO data buffers (1024-byte).
- Supports 3.3V VBUS voltage operation.
- Each IC has unique ID (for Serial Number)..

The PL2303GL is designed to support a wide-range of serial application domain including mobile, embedded, industrial, consumer, healthcare, navigation, and wearable solutions in mind. It provides a small footprint that could easily fit in to any connectors and handheld devices. With very small power consumption in either operating or suspend mode, the PL2303GL is perfect for bus powered operation with plenty of power left for the attached devices. Flexible signal level requirement on the RS232-like serial port side also allows the PL2303GL to connect directly to any 5V~1.8V range devices.

The PL2303GL is available in SOP8 small footprint Pb-free (RoHS compliant) green compound package.

6.1 PL2303 G-Series USB to Serial Family Product Table

Prolific's new PL2303 G-series USB to Serial family product line offers a variety of new advanced features for USB serial interface product design. The PL2303 G-series are redesigned to provide accurate and flexible baud rate support as well as plenty of I/O functions that can be easily configured in OTPROM memory.

PL2303G-Series USB to Serial (UART) Family Product Line					
Product	**PL2303GC**	**PL2303GS**	**PL2303GE**	**PL2303GT**	**PL2303GL**
Description	USB to Full UART (Integrated Clock)	USB to Full UART (Integrated Clock)	USB to Full UART (High ESD Protection)	USB to RS232 (Internal RS232 Transceiver)	**USB to Basic UART (Low-Pin Count)**
Packages	SSOP28 QFN24	SSOP16 QFN16	SSOP28	SSOP28	**SOP8**
UART Interface	RS232 RS422/RS485	RS232 RS422/RS485	RS232 RS422/RS485	RS232 Only	**RS232 (TX-RX Only)**
Max. Data Rates	12Mbps	12Mbps	12Mbps	1Mbps	**115200bps**
Dedicated GPIO Pins	6	0	6	4	**0**
Shared GPIO (with UART pins)	9	9	9	0	**0**
Clocking	Internal[1]	Internal	Internal[1]	Internal	**Internal**
OTPROM[2]	USB Data + Configurable GPIO Function	USB Data + Configurable GPIO Function	USB Data + Configurable GPIO Function	USB Data + Configurable GPIO Function	**USB Data**
External EEPROM Option	YES[3]	YES[3]	YES[3]	YES[3]	**NO**
Android OS Support	YES	YES	YES	YES	**YES**
Configurable Data Buffer[4]	768-byte (RX) 256-byte (TX)	768-byte (RX) 256-byte (TX)	768-byte (RX) 256-byte (TX)	768-byte (RX) 256-byte (TX)	**768-byte (RX) 256-byte (TX)**
Battery Charger Detection Option	YES	YES	YES	No	**No**
I/O Voltage Range	I/O levels from 1.8V to 5V	I/O levels from 1.8V to 5V	I/O levels from 1.8V to 5V	3.3V	**I/O levels from 1.8V to 5V**
Pin Compatible	PL2303HXD (SSOP28 only)	New design	PL2303EA	PL2303RA	**PL2303SA (SOP8 only)**

[1] – Also supports external crystal clock source to bypass internal clock.

[2] – OTPROM allows setting the USB data descriptors. Also allows setting of multi-function GPIO options.

[3] – External EEPROM (when enabled in OTPROM) will override OTPROM settings.

[4] – TX/RX data buffers are configurable in OTPROM (PL2303GC, PL2303GS, and PL2303GE); or by driver customization.

7. Pin Diagram and Description

7.1 SOP8 Pin Diagram

Figure 7-1 PL2303GL Pin Diagram (SOP8)

7.2 Pin Out Description

Table 7-1: USB Data Interface Pins

Pin Name	SOP8 Pin No.	Type	Description
DP	5	I/O	USB Port Data Plus (D+) Signal
DM	6	I/O	USB Port Data Minus (D-) Signal

Table 7-2: UART (Serial Port) Interface Pins

Pin Name	SOP8 Pin No.	Type	Description
TXD	2	Output	Serial Port: Transmitted Data Output
RXD	4	Input	Serial Port: Received Data Input (5V tolerant)

Table 7-3: Power and Ground Pins

Pin Name	SOP8 Pin No.	Type	Description
VDD_IO	3	Power	+1.8V to +5V I/O signal power input pin. VDD_IO supply voltage should not be larger than VIN voltage.
VO_33	8	Power	+3.3V output power from integrated LDO regulator. For self-powered design, supply +3.3V to this pin for disabling the LDO.
GND	1	Power	Ground
VIN	7	Power	USB port VBUS input power supply. For self-powered design, supply +3.3V to this pin.

8. Functional Description

This section details the functional block diagram description of the PL2303GL.

8.1 USB 1.1 FS Transceiver

The USB Transceiver provides the USB full-speed electrical signal requirements and USB physical interface (DP/DM). This block also includes one precise internal oscillator for PLL. The PLL provides the clock to other logic functions. This block also includes the internal USB series termination resistors on the USB data lines and pull-up resistor for the DP signal.

8.2 LDO Regulator

This block is the 5V to 3.3V LDO regulator to power and drive the USB transceiver. It also includes 3.3V brownout detection output signals that will be used by digital circuit to reset the chip. The LDO 5V to 3.3V can supply around 11mA for chip internal and supply the additional 80mA for external components.

8.3 Clock Generator

The clock generator module generates the 48MHz and 12MHz reference clock signals for internal chip logic. The internal clocks will be stopped while in suspend state.

8.4 USB FS SIE

The USB Full-Speed Serial Interface Engine (SIE) block performs the processing of USB DP/DM signals. It translates the internal parallel data to serial data and outputs to USB FS transceiver to generate external USB DP/DM signals timing. It also translates external USB DP/DM signals pass through USB FS transceiver to parallel data for internal circuit. This block supports USB packet decoding and encoding. It also generates and check packet CRC, bit stuffing, SYNC and EOP frame signal. The DPLL module will use the internal 48MHz clock to synchronize external DP/DM transitions to generate 12MHz clock for USB interface related circuit.

8.5 Power Management

This module will monitor the USB attachment and DP/DM signals state to create reset state, running state, suspend state, wakeup state, etc. Reset and suspend signals are generated from this module.

8.6 Control Endpoint

The Control Endpoint module handles control endpoint packet transfer protocols such as SETUP packet, DATA packet and return status packet.

8.7 Bulk Out Endpoint

The Bulk Out Endpoint module handles bulk-out endpoint packet transfer protocols such as DATA packet and return status packet. It also transfers USB host bulk-out data to chip outbound FIFO.

8.8 Bulk In Endpoint

The Bulk In Endpoint module handles bulk-in endpoint packet transfer protocols such as DATA packet and return status packet. It also transfers data inside the chip inbound FIFO to USB host through bulk-in DATA packet.

8.9 Interrupt In Endpoint

The Interrupt In Endpoint module handles interrupt-in endpoint packet transfer protocols such as DATA packet and return status packet. It transfers interrupt data generated inside the chip to USB host through interrupt-in DATA packet.

8.10 Command Sequencer

This module handles the USB standard requests and vendor requests. It dispatches control signals to relative peripheral modules and gather information from peripheral modules. When it received USB standard request commands, it may check ROM data or data latched from OTP and return them to USB host. When vendor requests are received, it dispatches to peripherals to set or get something.

8.11 Outbound FIFO

This buffer receives data from Bulk Out Endpoint and provides data to peripheral modules. It handles read and write pointers and calculate full and empty conditions. There are also near empty threshold check to notify peripheral module that FIFO is going to empty.

8.12 Inbound FIFO

This buffer receives data from peripheral modules and provides data to Bulk In Endpoint. It handles read and write pointers and calculate full and empty conditions. There are also near full threshold check to notify peripheral module that FIFO is going to full.

8.13 Event Generator

This module provides interrupt data to Interrupt In Endpoint. This module senses interrupt event toggle from UART peripheral.

8.14 Internal OTPROM

The OTPROM (One-Time Programming Read-Only Memory) for the PL2303GL is used to store chip function settings and USB descriptor related data. A one-time programming user area of the memory is available to allow customization of settings. The user area of the PL2303GL OTPROM can now be easily programmed using the Prolific OTPROM software through USB port without any additional voltage converter requirement. Refer to Section 9.0 for more information on the OTPROM configuration settings.

8.15 Mux/Demux

This module is designed to pass data between FIFO and UART peripheral module.

8.16 Descriptor ROM

This block contains the USB descriptor data for returning to USB host.

8.17 UART Control

The UART Control module handles the data transfer according to RS232 format and interface. Full set flow control is implemented including RTS/CTS, DTR/DSR and software flow control. Flow control circuit will check FIFO near full or near empty status to activate flow control signals. This module also includes a precise baud rate generator.

8.18 Control Registers

The Control Registers module contains the chip control registers read and set, and initially loads from OTPROM. USB host will use USB vendor command to read and write control registers to set chip function.

9. Chip Function Configuration

The default configuration descriptors are stored in the chip internal memory which will be loaded during power-on reset or USB bus reset whenever OTPROM (One-Time Programmable ROM) is empty. Several of the USB and configuration descriptors could be modified and programmed one-time into the chip's OTPROM using the PL2303GL OTPROM Writer utility program. These descriptors include Vendor ID, Product ID, Serial Number, Product String, and other USB configuration descriptors.

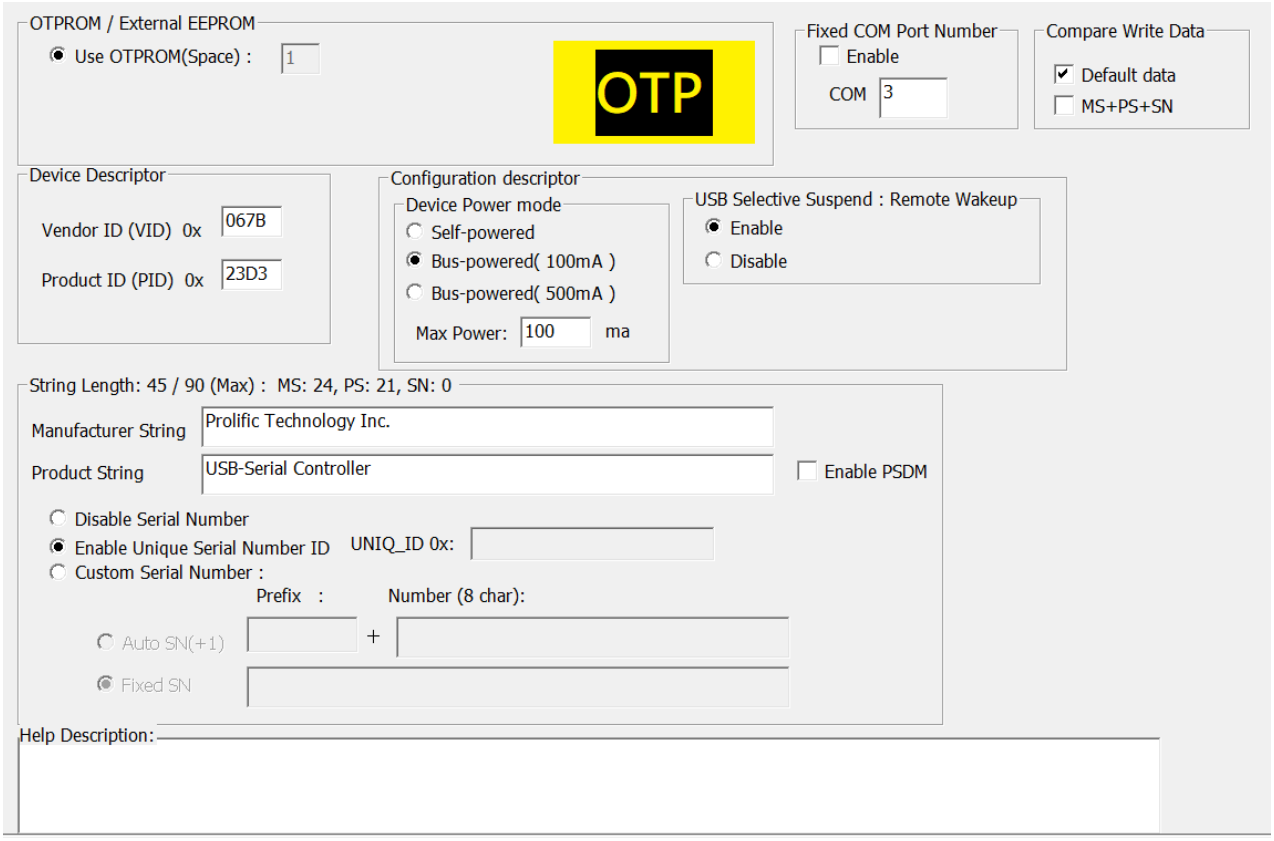


Figure 9-1 PL2303GL OTPROM Writer Tool

Table 9-1 USB Descriptor Configuration

Descriptors	Default Value	Description
OTPROM Space	1	This field indicates the space left for the OTPROM that can be written (1 or 0). The OTPROM can only be written once and cannot be erased. If value is 0, it means OTPROM has already been written once.
Vendor ID (VID)	067B (hex)	USB unique Vendor ID of Company or Manufacturer. This ID is applied and registered from USB-IF. Refer to this website for applying VID: http://www.usb.org/developers/vendor/
Product ID (PID)	23D3 (hex)	USB Product ID assigned by Company or Manufacturer.
Release No. (BCD)	0100 (hex)	This field reports the release number of the USB device. This item cannot be modified.
Device Power Mode	Bus Powered (100mA)	This field sets the USB device if bus-powered or self-powered device.
Max Power	100mA	This field sets the USB device maximum power in mA. Enter the value here if it is not 100mA or 500mA. Expressed in 2 mA units (i.e., 50 = 100 mA).
USB Selective Suspend	Enable	This field enables/disables the USB Selective Suspend function. When enabled, Windows OS will suspend the device when idle for few seconds (COM port not open).
Manufacturer String	Prolific Technology Inc.	This field contains the product manufacturer string.
Product String	USB-Serial Controller	This field when entered will be the device string displayed by Windows and other OS when device is first detected and before driver is loaded or driver not installed. After driver is loaded, Windows will show the product string written inside the driver INF file.

Serial Number	Enable Unique Serial Number ID	• Disable Serial Number – this option will disable the Serial Number. Operating System will assign a random serial number for the device.
		• Enable Unique Serial Number ID – this default option enables the unique serial number pre-programmed inside the chip.
		• Custom Serial Number – this option allows the customer to set own product serial numbering:
		  ○ Auto SN: allows to add prefix while the numbers auto increment after each write.
		  ○ Fixed SN: this will write the same number.
		Device with serial number enabled allows the device to be assigned with the same COM port number even when plug to other USB ports of the same PC.

NOTE: The total string length for the manufacturer + product + serial number string is up to 90 characters.

10. Design Application Examples

This section illustrates conceptual design application examples using the PL2303GL.

10.1 USB Bus Powered Design

The PL2303GL has a built-in 3.3V regulator. USB device power (pin VIN) can be supplied directly from USB VBUS pin. The capacitor behind the USB connector on VBUS is a defined requirement of USB specification. If the regulator output VO_33 needs to be maintained at 3.3V, VIN should be larger than 3.6V. It is also recommended to add capacitor at VO_33 pin, please refer to schematic.

This built-in 3.3V regulator can supply the chip operating power around 11mA and also supply the additional 80mA for external components.

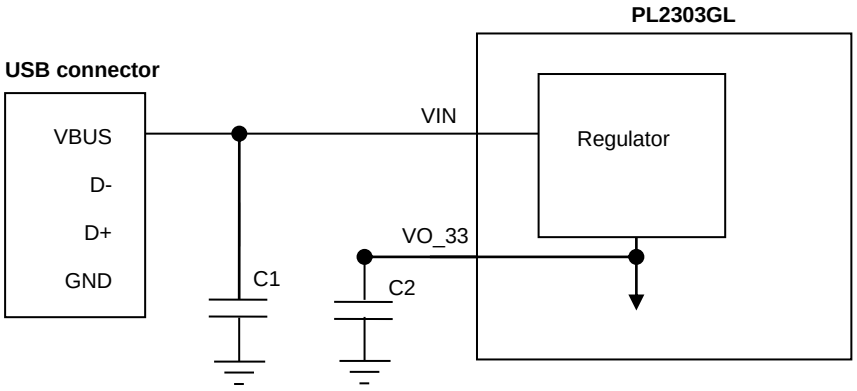


Figure 10-1 USB Bus Powered Design Example

10.2 I/O Power Supply to PL2303GL

The PL2303GL supports a wide range of I/O voltage. The simple way to supply IO voltage is to directly connect VDD_IO to VO_33 pin to provide 3.3V I/O voltage. Add capacitor to VDD_IO can help to reduce I/O noise. Please refer to schematic for the detailed capacitor value..

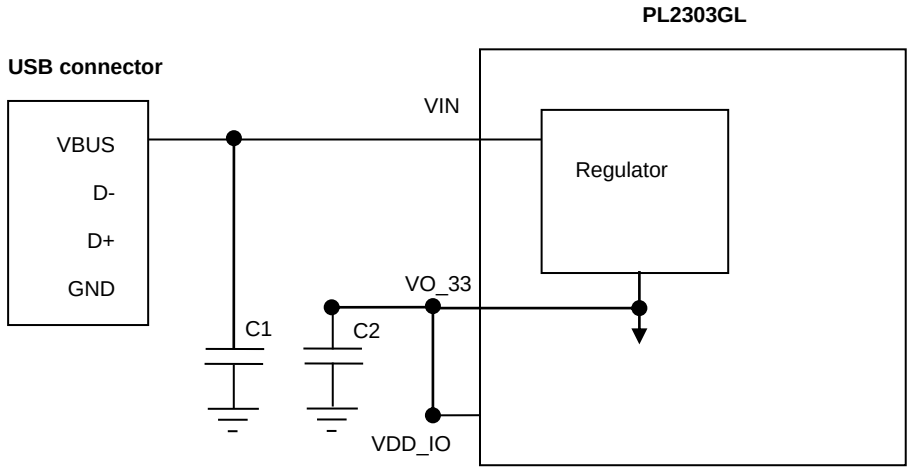


Figure 10-2a IO Power Supply

VDD_IO can also be supplied from other power source to provide different I/O voltage. This supplied VDD_IO voltage should not be larger than VIN voltage. All of the PL2303GL I/O pins use the same VDD_IO voltage. The I/O pins does not support mixed I/O voltages. Unless open-drain option is enabled, the I/O connection between two chips shall use the same VDD_IO voltage. PL2303GL I/O pin also supports 5V tolerance which allows 5V input signal level in different VDD_IO voltage.

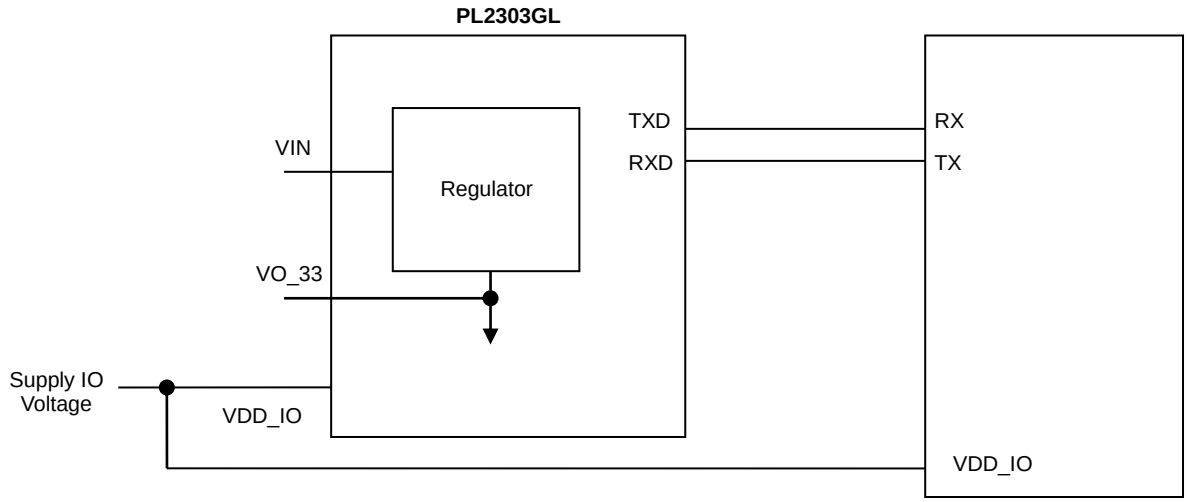


Figure 10-2b VDD_IO Voltage Supply

11. DC & Temperature Characteristics

11.1 Absolute Maximum Ratings

Table 11-1 Absolute Maximum Ratings

Items	Ratings
Power Supply Voltage – VIN	-0.3 to 6.0 V
Input Voltage of VDD_IO	-0.3 to VIN+0.3 V
Input Voltage of I/O with 5V Tolerance I/O	-0.3 to 6.0 V
Storage Temperature	-40 to 150 °C

Note: Permanent device damage may occur if the absolute maximum ratings are exceeded. These are stress rating only, and functional operation should be restricted to within the conditions. Exposure to absolute maximum rating conditions for extended periods may affect the device's reliability.

11.2 DC Characteristics

11.2.1 Operating Voltage and Suspend Current

Table 11-2a Operating Voltage and Suspend Current

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage Range	VIN	2.8	5	5.5	V
Power Supply for I/O Pins	VDD_IO	1.8	3.3	VIN+0.3	V
Output Voltage of Regulator	VO_33	2.97	3.3	3.63	V
Operating Current(1) (Power Consumption)	I_{DD}	-	9.5	15	mA
Suspend Current	I_{SUS}	-	250	450	μA

Note: (1) – No device connected.

11.2.2 I/O Pins

Table 11-2b I/O Pins

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltage (CMOS)					
Low	V_{IL}	--	--	0.4	V
High	V_{IH}	0.7* VDD_IO	--	--	V
Output Voltage					
Low	V_{OL}	--	--	0.4	V
High	V_{OH}	0.7*VDD_IO	--	--	V

11.3 Temperature Characteristics

Table 11-3 Temperature Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Operating Temperature (ambient)	--	-40	--	85	°C
Junction Operation Temperature	T_J	-40	25	125	°C

12. Outline Diagram

12.1 Chip Marking information

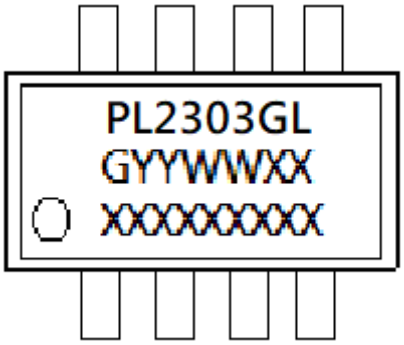


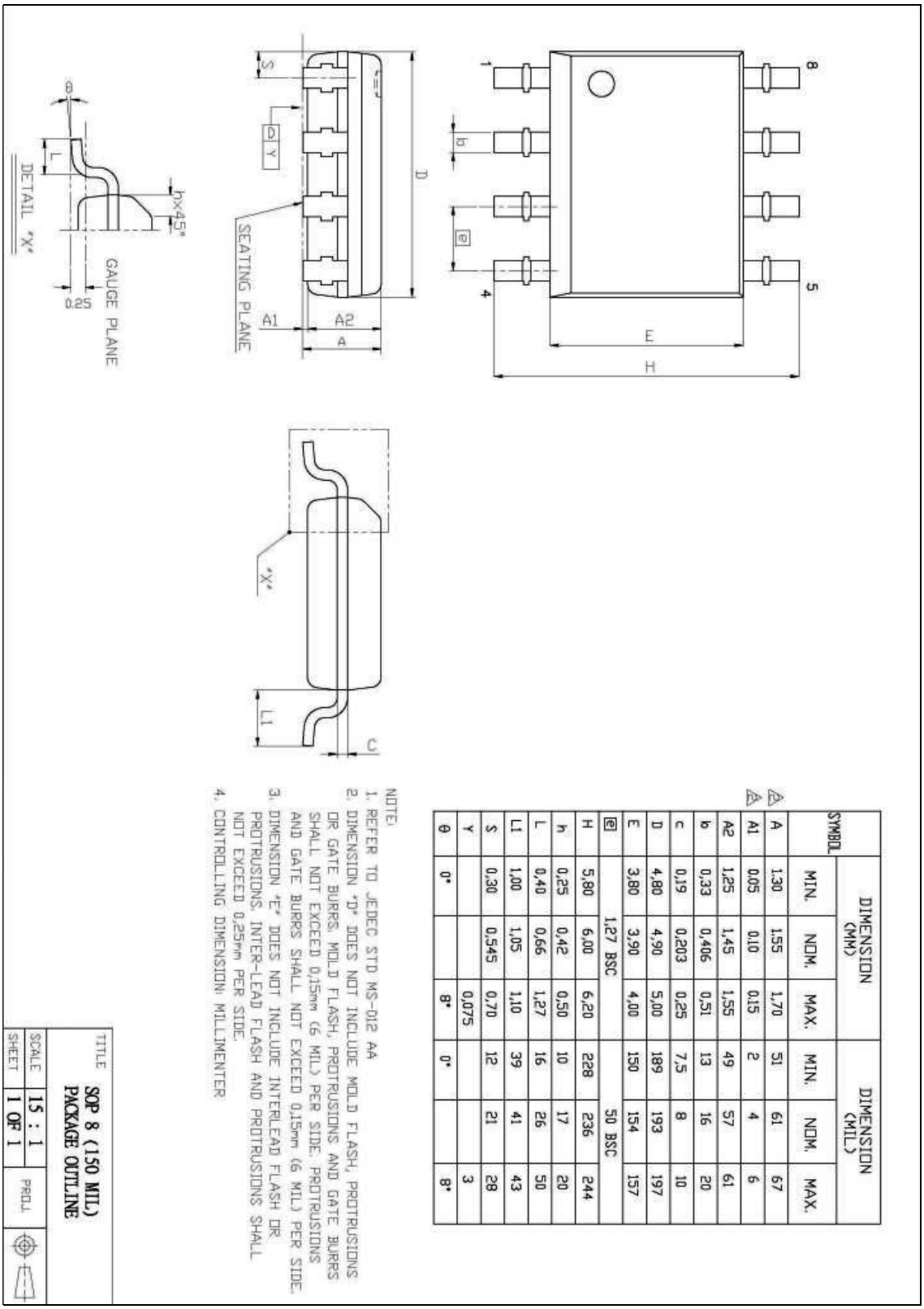
Figure 12-1 Chip Part Number Information (SOP)

Table 12-2 Chip Marking Information

Line	Marking	Description
First Line	PL2303GL	Chip Product Name
Second Line (GYYWWXX)	G	Green packing material
	YY	Last two digits of the manufacturing year
	WW	Week number of the manufacturing year
	XX	Chip Version
Third Line	XXXXXXXXX	Manufacturing LOT code

Example: "*G19361A*" – means Green packing + Year 2019 + Week no. 36 + 1A chip version.

12.2 SOP8 Package



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.30	1.55	1.70	51	61	67
A1	0.05	0.10	0.15	2	4	6
A2	1.25	1.45	1.55	49	57	61
b	0.33	0.406	0.51	13	16	20
c	0.19	0.203	0.25	7.5	8	10
D	4.80	4.90	5.00	189	193	197
E	3.80	3.90	4.00	150	154	157
e		1.27 BSC			50 BSC	
H	5.80	6.00	6.20	228	236	244
h	0.25	0.42	0.50	10	17	20
L	0.40	0.66	1.27	16	26	50
L1	1.00	1.05	1.10	39	41	43
S	0.30	0.545	0.70	12	21	28
Y			0.075			3
θ	0°		8°	0°		8°

Figure 12-1 PL2303GL Outline Diagram (SOP8)

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