# Remote16-BIT I²C AND SMBus I/O Expander with Interrupt Output

## Features


SSOP-24/QSOP-24

- I²C to Parallel-Port Expander
- Open-Drain Interrupt Output
- Low Standby-Current Consumption of 10μA Max
- Compatible With Most Micro controllers
- 400-kHz Fast I²C Bus
- Address by Three Hardware Address Pins for Use of up to Eight Devices
- Latched Outputs With High-Current Drive Capability for Directly Driving LEDs
- Current Source to Vcc for Actively Driving a High at the Output
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model
  - 200-V Machine Model
  - 1000-V Charged-Device Model

## Ordering Information

| DEVICE | Package Type | MARKING | Packing | Packing Qty |
|---|---|---|---|---|
| PCF8575MS/TR | SSOP-24/QSOP-24 | PCF8575 | REEL | 2500pcs/reel |

## Description

This 16-bit I/O expander for the two-line bidirectional bus ($I^2C$) is designed for 2.5-V to 5.5-V VCC operation.

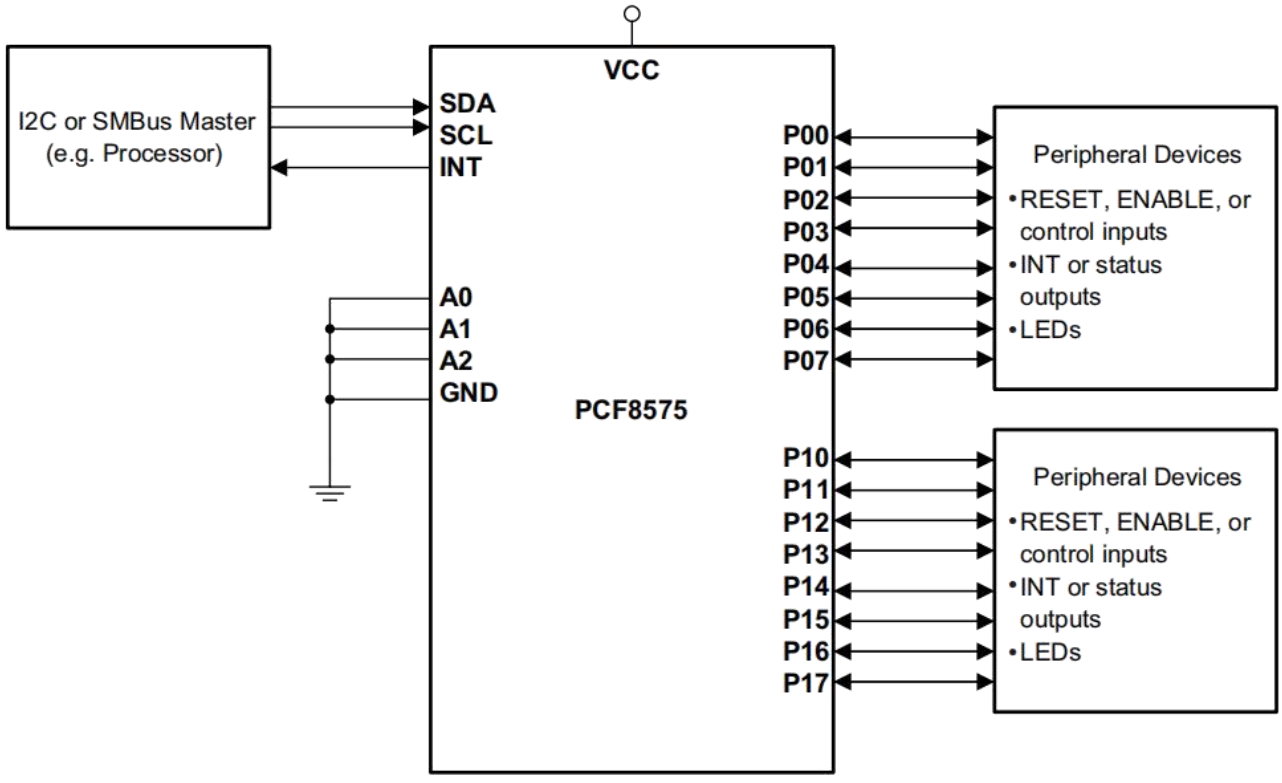
The PCF8575 device provides general-purpose remote I/O expansion for most microcontroller families by way of the $I^2C$ interface [serial clock (SCL), serial data (SDA)].

The device features a 16-bit quasi-bidirectional input/output (I/O) port (P07–P00, P17–P10), including latched outputs with high-current drive capability for directly driving LEDs. Each quasi-bidirectional I/O can be used as an input or output without the use of a data-direction control signal. At power on, the I/Os are high. In this mode, only a current source to VCC is active.

## Applications

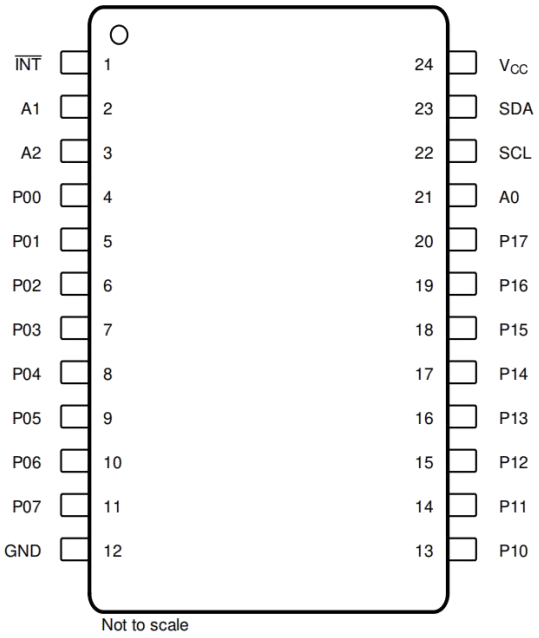
- Telecom Shelters: Filter Units
- Servers
- Routers (Telecom Switching Equipment)
- Personal Computers
- Personal Electronics
- Industrial Automation
- Products with GPIO-Limited Processors

## Simplified Schematic



## Pin Configuration and Functions

SSOP-24(QSOP24)（Top View）




Not to scale

## Pin Functions

| NAME | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| A0 | 21 | I | Address input 0. Connect directly to VCC or ground. Pull-up resistors are not needed. |
| A1 | 2 | I | Address input 1. Connect directly to VCC or ground. Pull-up resistors are not needed. |
| A2 | 3 | I | Address input 2. Connect directly to VCC or ground. Pull-up resistors are not needed. |
| $\overline{INT}$ | 1 | O | Interrupt output. Connect to VCC through a pull-up resistor. |
| P00 | 4 | I/O | P-port input/output. Push-pull design structure. |
| P01 | 5 | I/O | P-port input/output. Push-pull design structure. |
| P02 | 6 | I/O | P-port input/output. Push-pull design structure. |
| P03 | 7 | I/O | P-port input/output. Push-pull design structure. |
| P04 | 8 | I/O | P-port input/output. Push-pull design structure. |
| P05 | 9 | I/O | P-port input/output. Push-pull design structure. |
| P06 | 10 | I/O | P-port input/output. Push-pull design structure. |
| P07 | 11 | I/O | P-port input/output. Push-pull design structure. |
| GND | 12 | — | Ground |
| P10 | 13 | I/O | P-port input/output. Push-pull design structure. |
| P11 | 14 | I/O | P-port input/output. Push-pull design structure. |
| P12 | 15 | I/O | P-port input/output. Push-pull design structure. |
| P13 | 16 | I/O | P-port input/output. Push-pull design structure. |
| P14 | 17 | I/O | P-port input/output. Push-pull design structure. |
| P15 | 18 | I/O | P-port input/output. Push-pull design structure. |
| P16 | 19 | I/O | P-port input/output. Push-pull design structure. |
| P17 | 20 | I/O | P-port input/output. Push-pull design structure. |
| SCL | 22 | I | Serial clock line. Connect to VCC through a pull-up resistor |
| SDA | 23 | I/O | Serial data line. Connect to VCC through a pull-up resistor. |
| $V_{CC}$ | 24 | — | Supply voltage |

## Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| VCC | Supply voltage range | | –0.5 | 6.5 | V |
| VI | Input voltage range(2) | | –0.5 | $V_{CC}$ + 0.5 | V |
| VO | Output voltage range(2) | | –0.5 | $V_{CC}$ + 0.5 | V |
| IIK | Input clamp current | $V_I$ < 0 | | –20 | mA |
| IOK | Output clamp current | $V_O$ < 0 | | –20 | mA |
| IOK | Input/output clamp current | $V_O$ < 0 or $V_O$ > $V_{CC}$ | | –20 | mA |
| IOL | Continuous output low current | $V_O$ = 0 to $V_{CC}$ | | 50 | mA |
| IOH | Continuous output high current | $V_O$ = 0 to $V_{CC}$ | | –4 | mA |
| | Continuous current through VCC or GND | | | ±100 | mA |
| Tstg | Storage temperature range | | | 150 | °C |
| $T_L$ | Lead Temperature (Soldering, 10 seconds) | | - | 260 | °C |

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

## ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| V(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins | 2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22- C101, all pins | 1000 | |

## Recommended Operating Conditions

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 2.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 0.7 × $V_{CC}$ | $V_{CC}$ + 0.5 | V |
| $V_{IL}$ | Low-level input voltage | –0.5 | 0.3 × $V_{CC}$ | V |
| $I_{OH}$ | P-port high-level output current | | –1 | mA |
| $I_{OHT}$ | P-port transient pullup current | | –10 | mA |
| $I_{OL}$ | P-port low-level output current | | 25 | mA |
| $T_A$ | Operating free-air temperature | –40 | 85 | °C |

## Thermal Information

| THERMAL METRIC(1) | | PCF8575MS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 63 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | VCC | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | Input diode clamp voltage | $I_I$ = –18mA | 2.5 V to 5.5 V | -1.2 | | | V |
| $V_{POR}$ | Power-on reset voltage(2) | $V_I = V_{CC}$ or GND, $I_O$ = 0 | VPOR | | 1.2 | 1.8 | V |
| $I_{OH}$ | P port | $V_O$ = GND | 2.5 V to 5.5 V | -30 | | -300 | μA |
| $I_{OHT}$ | P-port transient pullup curren | High during ACK, $V_{OH}$ = GND | 2.5 V | -0.5 | -1 | | mA |
| $I_{OL}$ | SDA | $V_{OL}$ = 0.4 V | 2.5 V to 5.5 V | 3 | | | mA |
| | P port | $V_{OL}$ = 0.4 V | | 5 | 15 | | |
| | | $V_{OL}$ = 1 V | | 10 | 25 | | |
| | $\overline{INT}$ | $V_{OL}$ = 0.4 V | | 1.3 | | | |
| $I_I$ | SCL, SDA | $V_I = V_{CC}$ or GND | 2.5 V to 5.5 V | | | ±5 | μA |
| | A0, A1, A2 | | | | | ±1 | |
| $I_{IHL}$ | P port | $V_I \geq V_{CC}$ or VI ≤ GND | 2.5 V to 5.5 V | | | ±400 | μA |
| ICC | Operating mode | $V_I = V_{CC}$ or GND, IO = 0, fscl = 400 kHz | 5.5 V | | 100 | 200 | μA |
| | | | 3.6 V | | 30 | 75 | |
| | | | 2.7 V | | 20 | 50 | |
| | Standby mode | $V_I = V_{CC}$ or GND, $I_O$ = 0, fscl = 0 kHz | 5.5 V | | 2.5 | 10 | |
| | | | 3.6 V | | 2.5 | 10 | |
| | | | 2.7 V | | 2.5 | 10 | |
| $\Delta I_{CC}$ | Supply current increase | One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND | 2.5 V to 5.5 V | | | 200 | μA |
| $C_I$ | SCL | $V_I = V_{CC}$ or GND | 2.5 V to 5.5 V | | 3 | 7 | pF |
| Cio | SDA | $V_{IO} = V_{CC}$ or GND | 2.5 V to 5.5 V | | 3 | 7 | pF |
| | P port | | | | 4 | 10 | |

(1) All typical values are at nominal supply voltage (2.5V, 3.3V, or 5V $V_{CC}$) and $T_A$ = 25°C.

(2) The power-on reset circuit resets the I2C bus logic with $V_{CC} < V_{POR}$ and sets all I/Os to logic high (with current source to $V_{CC}$).

## I2C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 12)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| fscl | $I^2C$ clock frequency | | | 400 | kHz |
| tsch | $I^2C$ clock high time | | 0.6 | | μs |
| tscl | $I^2C$ clock low time | | 1.3 | | μs |
| tsp | $I^2C$ spike time | | | 50 | ns |
| tsds | $I^2C$ serial data setup time | | 100 | | ns |
| tsdh | $I^2C$ serial data hold time | | 0 | | ns |
| ticr | $I^2C$ input rise time | | $20+0.1C_b$ (1) | 300 | ns |
| ticf | $I^2C$ input fall time | | $20+0.1C_b$ (1) | 300 | ns |
| tocf | $I^2C$ output fall time | 10-pF to 400-pF bus | | 300 | ns |
| tbuf | $I^2C$ bus free time between Stop and Start | | 1.3 | | μs |
| tsts | $I^2C$ start or repeated Start condition setup | | 0.6 | | μs |
| tsth | $I^2C$ start or repeated Start condition hold | | 0.6 | | μs |
| tsps | $I^2C$ Stop condition setup | | 0.6 | | μs |
| tvd | Valid-data time | SCL low to SDA output valid | | 1.2 | μs |
| Cb | $I^2C$ bus capacitive load | | | 400 | pF |

## Switching Characteristics

over recommended operating free-air temperature range, CL ≤ 100 pF (unless otherwise noted) (see Figure 13 and Figure 14)

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| tiv | Interrupt valid time | P port | INT | | 4 | μs |
| tir | Interrupt reset delay time | SCL | INT | | 4 | μs |
| tpv | Output data valid | SCL | P port | | 4 | μs |
| tsu | Input data setup time | P port | SCL | 0 | | μs |
| th | Input data hold time | P port | SCL | 4 | | μs |

## Typical Characteristics

$T_A$ = 25°C (unless otherwise noted)

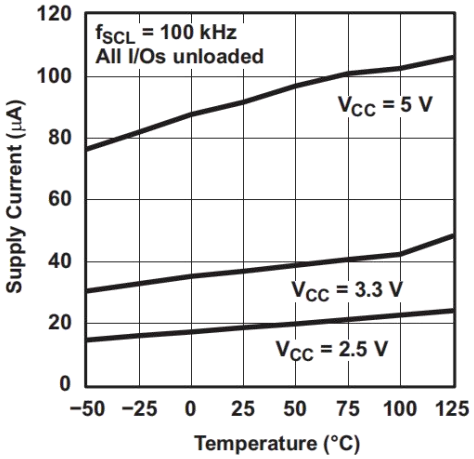



Figure 1. Supply Current vs Temperature

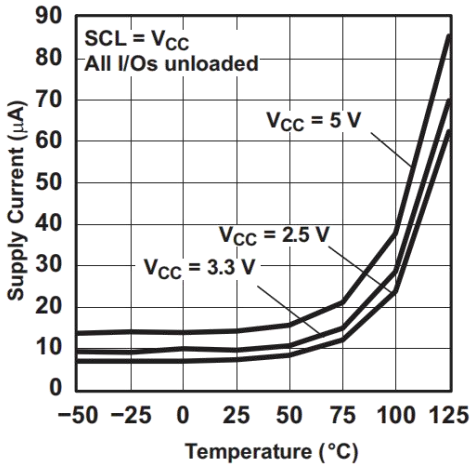



Figure 2. Standby Supply Current vs Temperature

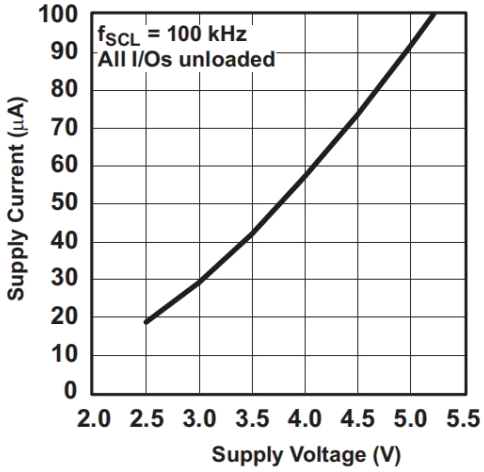



Figure 3. Supply Current vs Supply Voltage

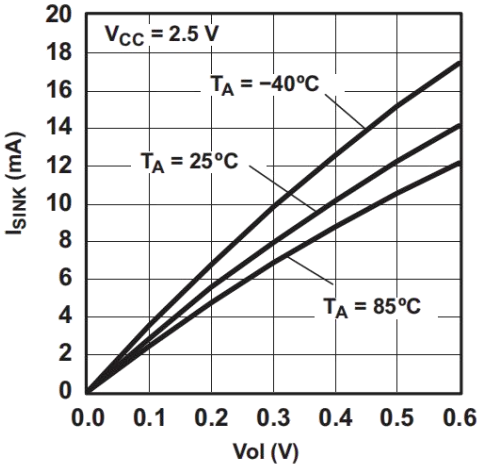



Figure 4. I/O Sink Current vs Output Low Voltage

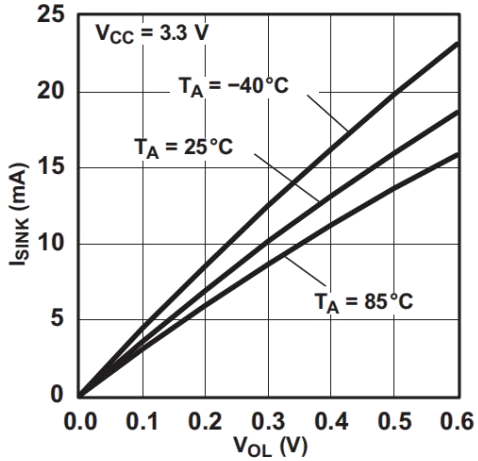



Figure 5. I/O Sink Current vs Output Low Voltage

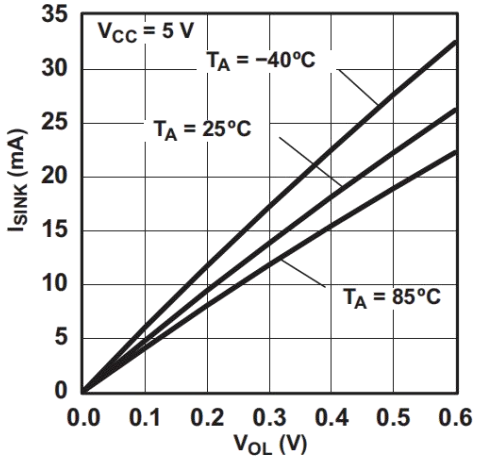



Figure 6. I/O Sink Current vs Output Low Voltage

## Typical Characteristics(continued)

$T_A$ = 25°C (unless otherwise noted)

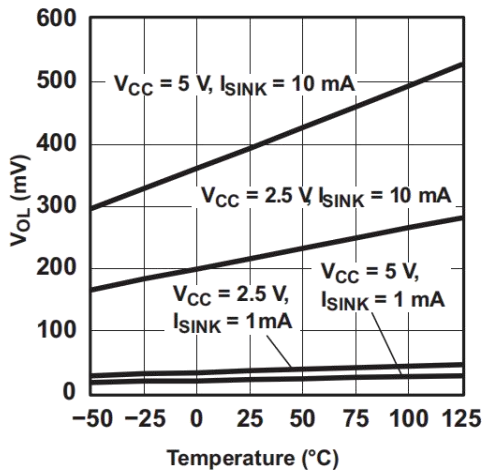



Figure 7. I/O Output Low Voltage vs Temperature

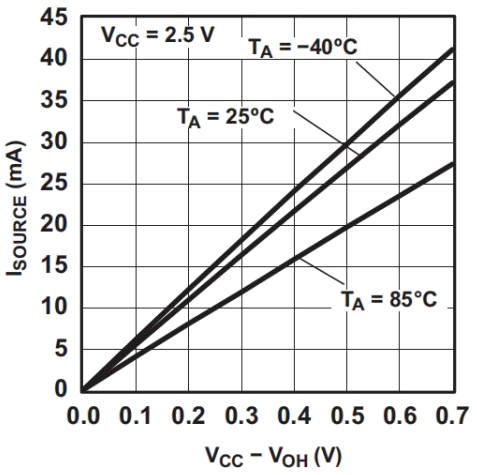



Figure 8. I/O Source Current vs Output High Voltage

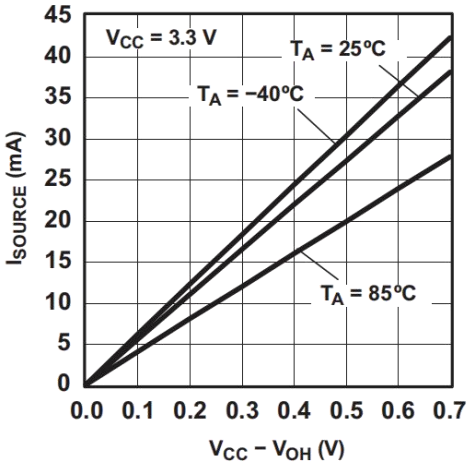



Figure 9. I/O Source Current vs Output High Voltage

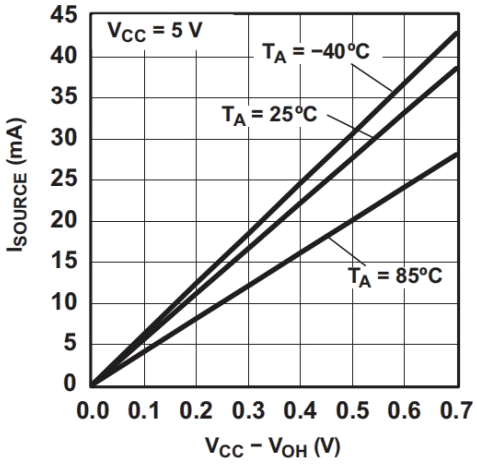



Figure 10. I/O Source Current vs Output High Voltage

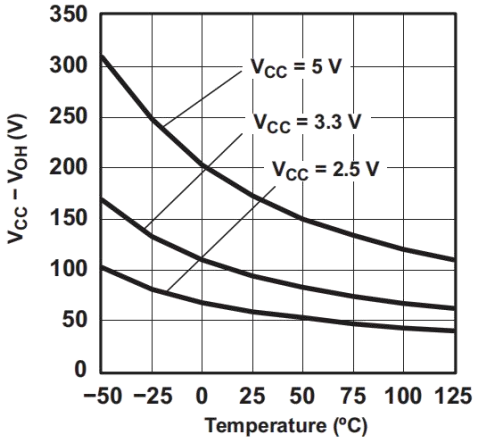
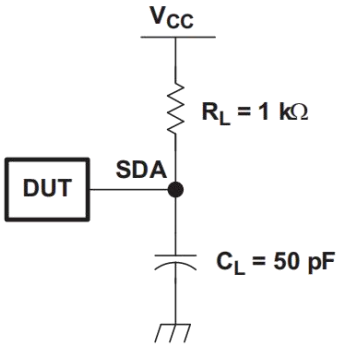
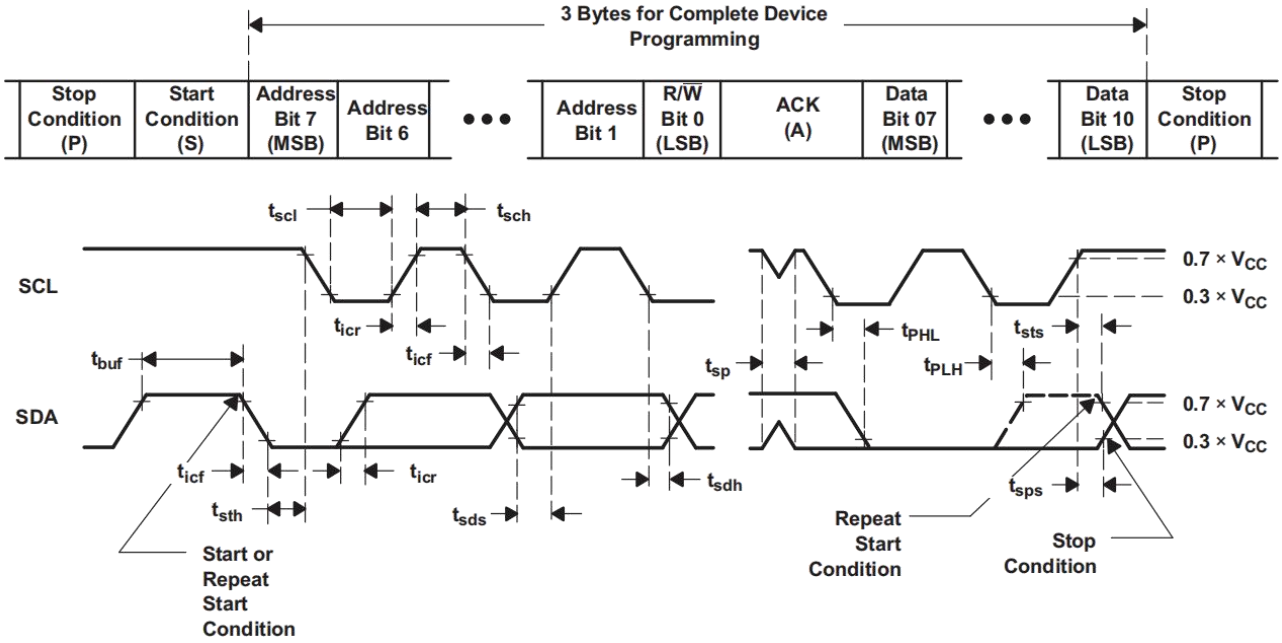



Figure 11. I/O High Voltage vs Temperature

## Parameter Measurement Information




SDA LOAD CONFIGURATION




VOLTAGE WAVEFORMS

| BYTE | DESCRIPTION |
|---|---|
| 1 | I²C address |
| 2, 3 | P-port data |

Figure 12. I²C Interface Load Circuit and Voltage Waveforms

## Parameter Measurement Information(continued)

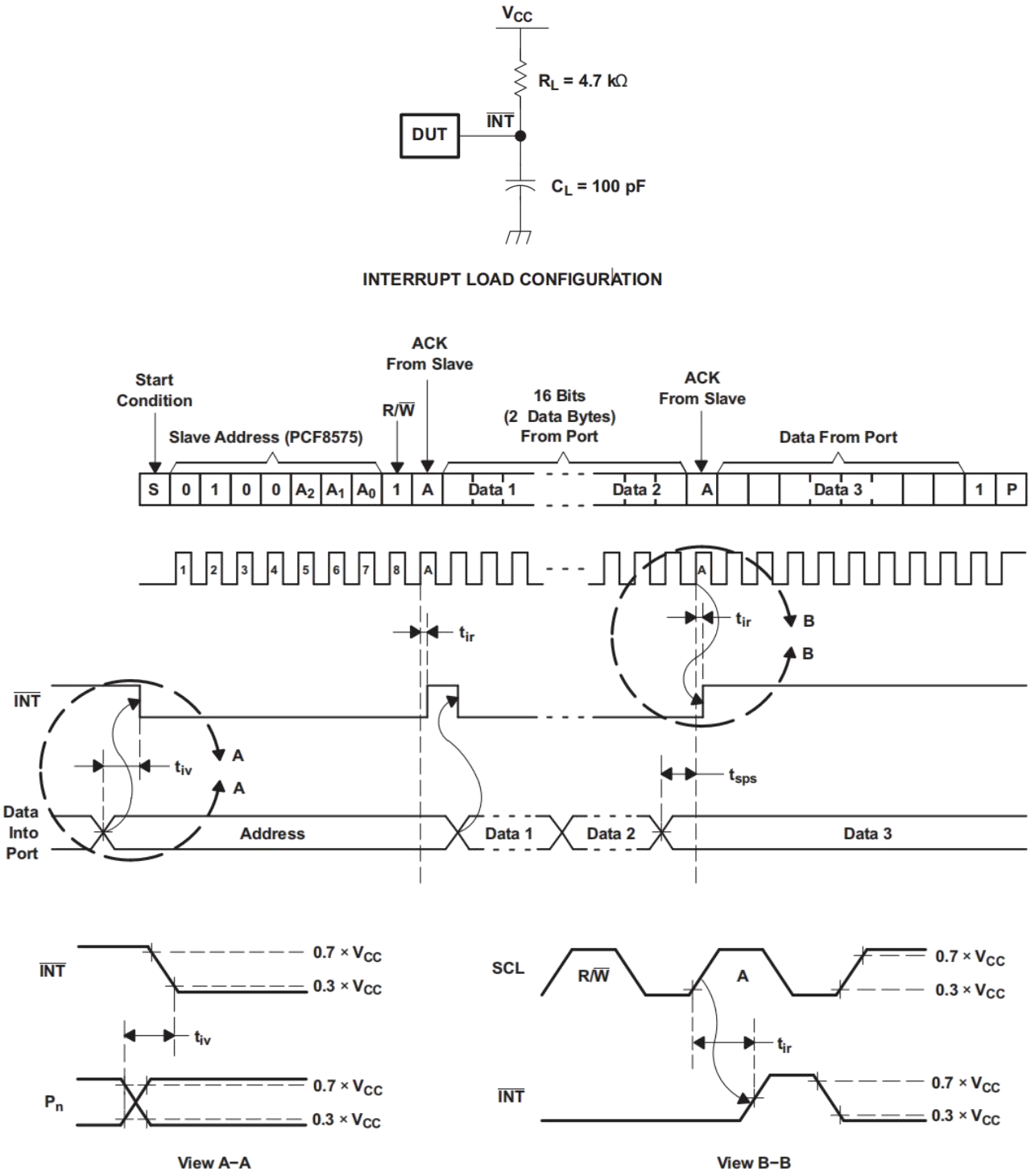
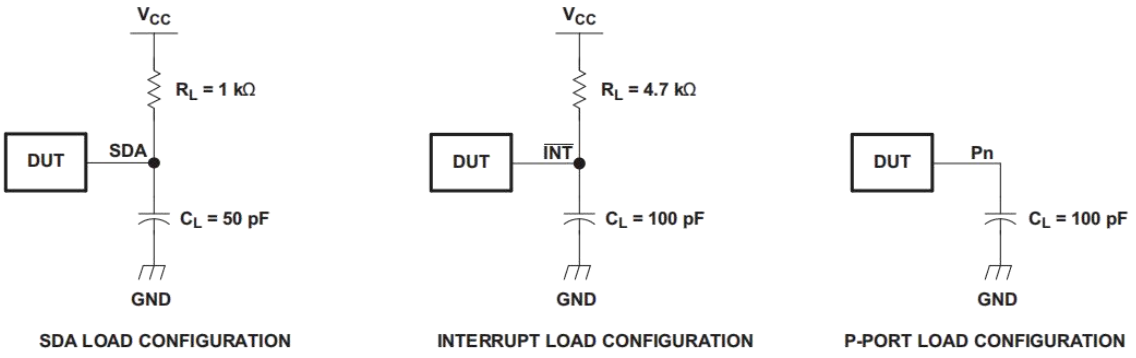
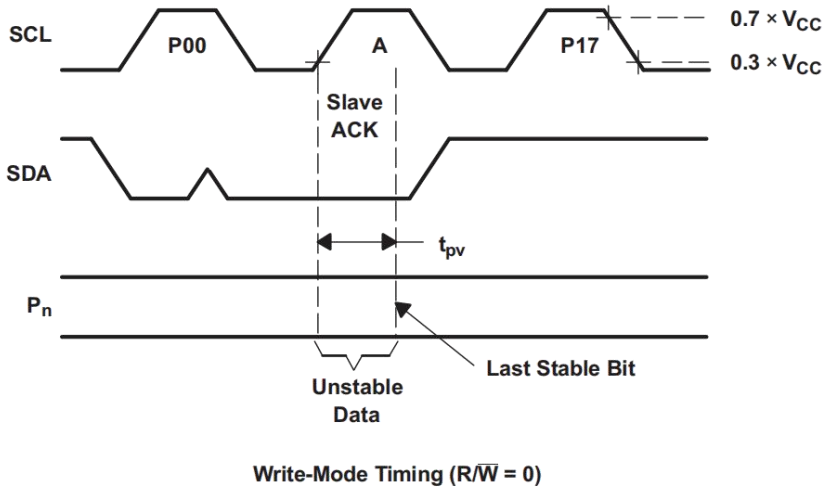



Figure 13. Interrupt Load Circuit and Voltage Waveforms

## Parameter Measurement Information(continued)



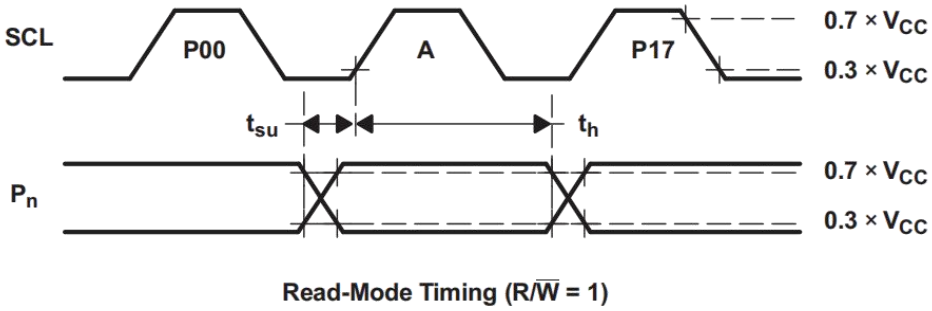




Figure 14. P-Port Load Circuits and Voltage Waveforms

# Detailed Description

## Overview

The PCF8575 provides general-purpose remote I/O expansion for most micro controller families via the I 2C interface serial clock (SCL) and serial data (SDA).

The device features a 16-bit quasi-bidirectional input/output (I/O) port (P07–P00, P17–P10), including latched outputs with high-current drive capability for directly driving LEDs. Each quasi-bidirectional I/O can be used as an input or output without the use of a data-direction control signal. At power on, the I/Os are high. In this mode, only a current source (IOH) to VCC is active. An additional strong pullup to VCC (IOHT) allows fast-rising edges into heavily loaded outputs. This device turns on when an output is written high and is switched off by the negative edge of SCL. The I/Os should be high before being used as inputs. After power on, as all the I/Os are set high, all of them can be used as inputs. Any change in setting of the I/Os as either input or outputs can be done with the write mode. If a high is applied externally to an I/O that has been written earlier to low, a large current (IOL) will flow to GND.

The PCF8575 provides an open-drain interrupt (INT) output, which can be connected to the interrupt input of a micro controller. An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time, tiv, the signal INT is valid. Resetting and reactivating the interrupt circuit is achieved when data on the port is changed to the original setting, or data is read from or written to the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) bit after the rising edge of the SCL signal or in the write mode at the ACK bit after the falling edge of the SCL signal. Interrupts that occur during the ACK clock pulse can be lost (or be very short), due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as INT. Reading from or writing to another device does not affect the interrupt circuit. This device does not have internal configuration or status registers. Instead, read or write to the device I/Os directly after sending the device address (see Figure 18 and Figure 19).

By sending an interrupt signal on this line, the remote I/O can inform the micro controller if there is incoming data on its ports, without having to communicate via the I 2C bus. Thus, the PCF8575 can remain a simple slave device.

Every data transmission to or from the PCF8575 must consist of an even number of bytes. The first data byte in every pair refers to port 0 (P07–P00), and the second data byte in every pair refers to port 1 (P17–P10). To write to the ports (output mode), the master first addresses the slave device, setting the last bit of the byte containing the slave address to logic 0. The PCF8575 acknowledges, and the master sends the first data byte for P07–P00.

After the first data byte is acknowledged by the PCF8575, the second data byte (P17–P10) is sent by the master.

Once again, the PCF8575 acknowledges the receipt of the data, after which this 16-bit data is presented on the port lines.

The number of data bytes that can be sent successively is not limited. After every two bytes, the previous data is overwritten. When the PCF8575 receives the pairs of data bytes, the first byte is referred to as P07–P00 and the second byte as P17–P10. The third byte is referred to as P07–P00, the fourth byte as P17–P10, and so on.

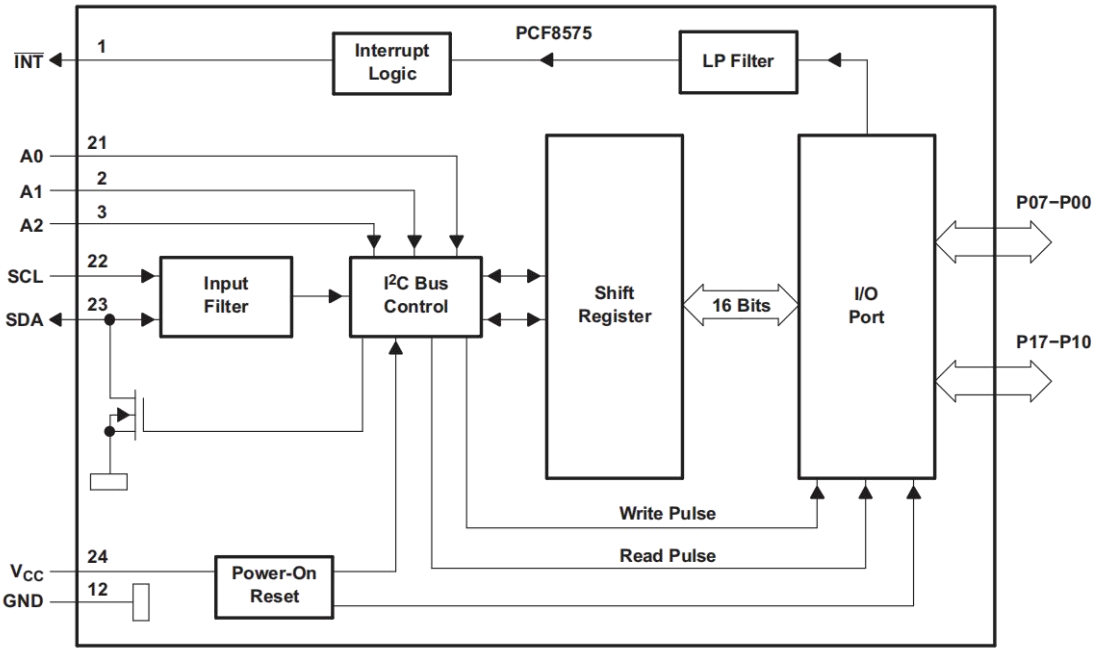
Before reading from the PCF8575, all ports desired as input should be set to logic 1. To read from the ports (input mode), the master first addresses the slave device, setting the last bit of the byte containing the slave address to logic 1. The data bytes that follow on the SDA are the values on the ports. If the data on the input port changes faster than the master can read, this data may be lost.

When power is applied to VCC, an internal power-on reset holds the PCF8575 in a reset state until VCC has reached VPOR. At that time, the reset condition is released, and the device I 2C-bus state machine initializes the bus to its default state.

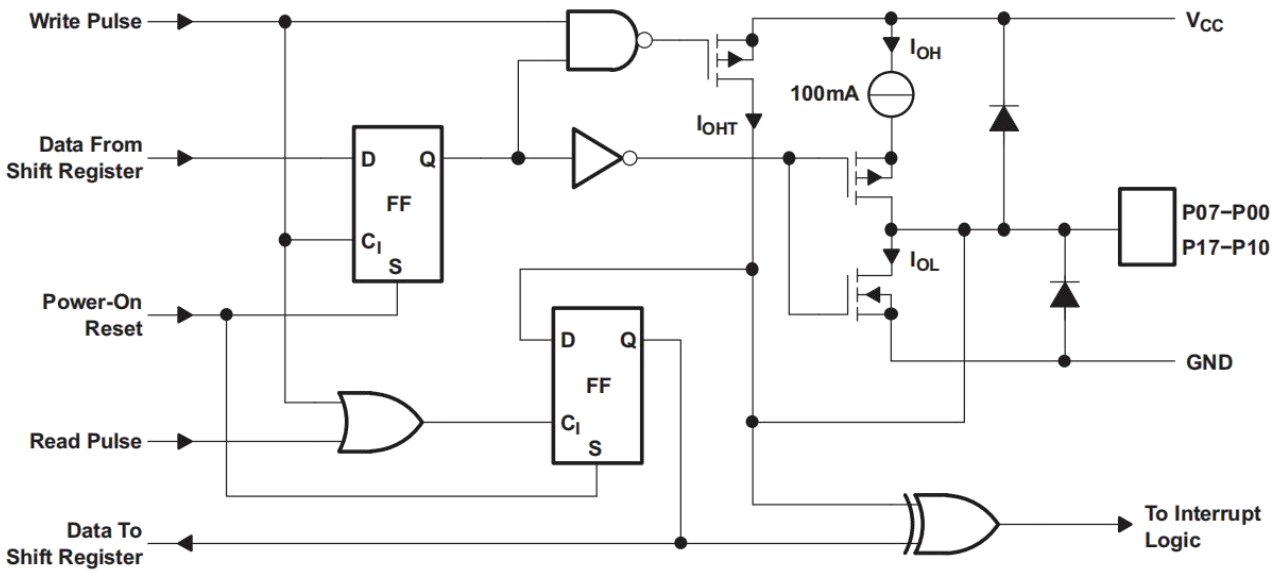
The hardware pins (A0, A1, and A2) are used to program and vary the fixed I 2C address and allow up to eight devices to share the same I 2C bus or SMBus. The fixed I 2C address of the PCF8575 is the same as the PCF8575C, PCF8574, PCA9535, and PCA9555, allowing up to eight of these devices, in any combination, to share the same I 2C bus or SMBus.

# Functional Block Diagram

## Logic Diagram (Positive Logic)




## Simplified Schematic Diagram of Each P-Port Input/Output



# Feature Description

## I²C Interface

The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply via a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I²C communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see Figure 15). After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/W). This device does not respond to the general call address. After receiving the valid address byte, this device responds with an ACK, a low on the SDA input/output during the high of the ACK-related clock pulse. The address inputs (A2–A0) of the slave device must not be changed between the Start and Stop conditions.

The data byte follows the address ACK. If the R/W bit is high, the data from this device are the values read from the P port. If the R/W bit is low, the data are from the master, to be output to the P port. The data byte is followed by an ACK sent from this device. If other data bytes are sent from the master, following the ACK, they are ignored by this device. Data are output only if complete bytes are received and acknowledged. The output data is valid at time (tpv) after the low-to-high transition of SCL, during the clock cycle for the ACK.

On the I 2C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop) (see Figure 16).

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see Figure 15).

The number of data bytes transferred between the Start and Stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit.

A slave receiver that is addressed must generate an ACK after the reception of each byte. Also, a master must generate an ACK after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 17). Setup and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge (NACK) after the last byte that has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.

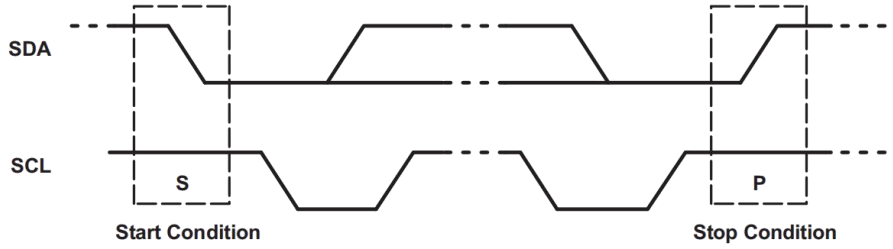



Figure 15. Definition of Start and Stop Conditions

## Feature Description (continued)

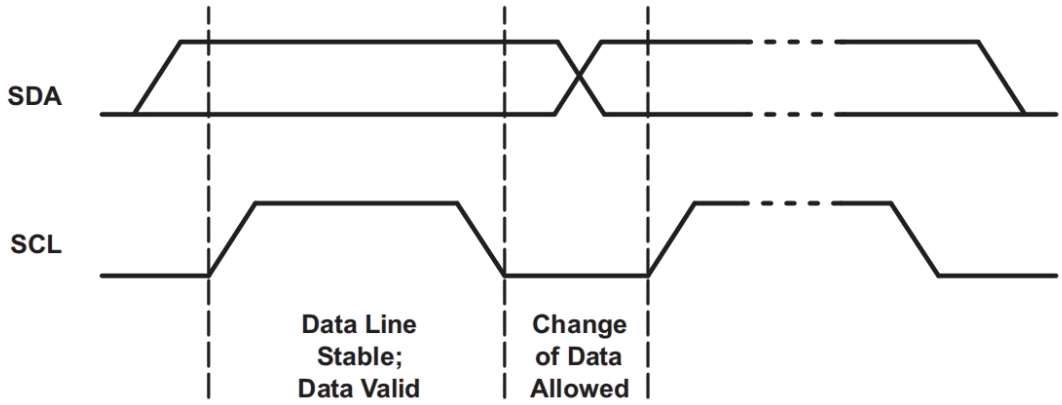



Figure 16. Bit Transfer

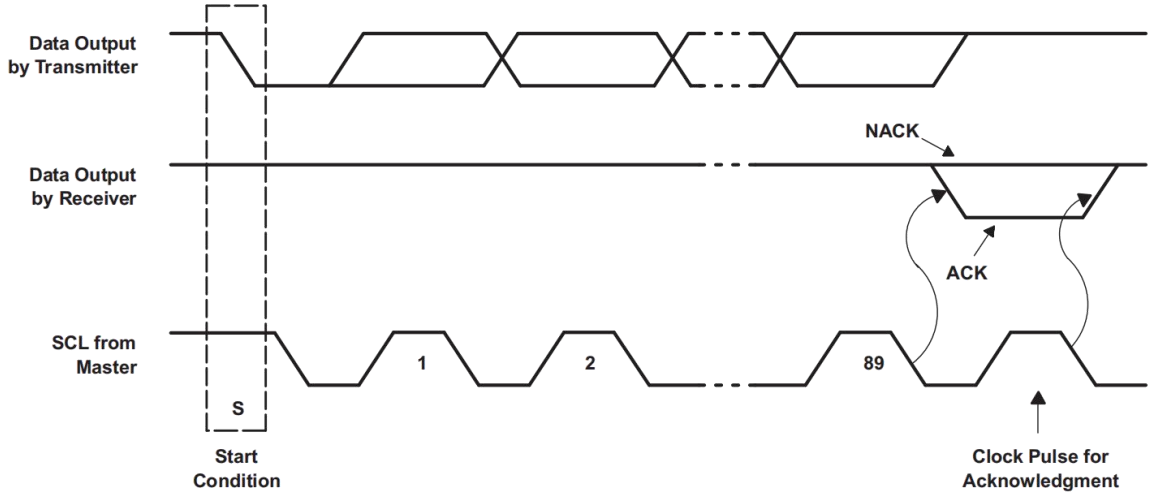



Figure 17. Acknowledgment on I²C Bus

### Interface Definition

| BYTE | BIT | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 (MSB) | 6 | 5 | 4 | 3 | 2 | 1 | 0 (LSB) |
| I²C slave address | L | H | L | L | A2 | A1 | A0 | R/W |
| P0x I/O data bus | P07 | P06 | P05 | P04 | P03 | P02 | P01 | P00 |
| P1x I/O data bus | P17 | P16 | P15 | P14 | P13 | P12 | P11 | P10 |

## Address Reference

| INPUTS | | | I2C BUS SLAVE 8-BIT READ ADDRESS | I2C BUS SLAVE 8- BIT WRITE ADDRESS |
|---|---|---|---|---|
| A2 | A1 | A0 | | |
| L | L | L | 65 (decimal), 41 (hexadecimal) | 64 (decimal), 40 (hexadecimal) |
| L | L | H | 67 (decimal), 43 (hexadecimal) | 66 (decimal), 42 (hexadecimal) |
| L | H | L | 69 (decimal), 45 (hexadecimal) | 68 (decimal), 44 (hexadecimal) |
| L | H | H | 71 (decimal), 47 (hexadecimal) | 70 (decimal), 46 (hexadecimal) |
| H | L | L | 73 (decimal), 49 (hexadecimal) | 72 (decimal), 48 (hexadecimal) |
| H | L | H | 75 (decimal), 4B (hexadecimal) | 74 (decimal), 4A (hexadecimal) |
| H | H | L | 77 (decimal), 4D (hexadecimal) | 76 (decimal), 4C (hexadecimal) |
| H | H | H | 79 (decimal), 4F (hexadecimal) | 78 (decimal), 4E (hexadecimal) |

## Device Functional Modes

Figure 18 and Figure 19 show the address and timing diagrams for the write and read modes, respectively.

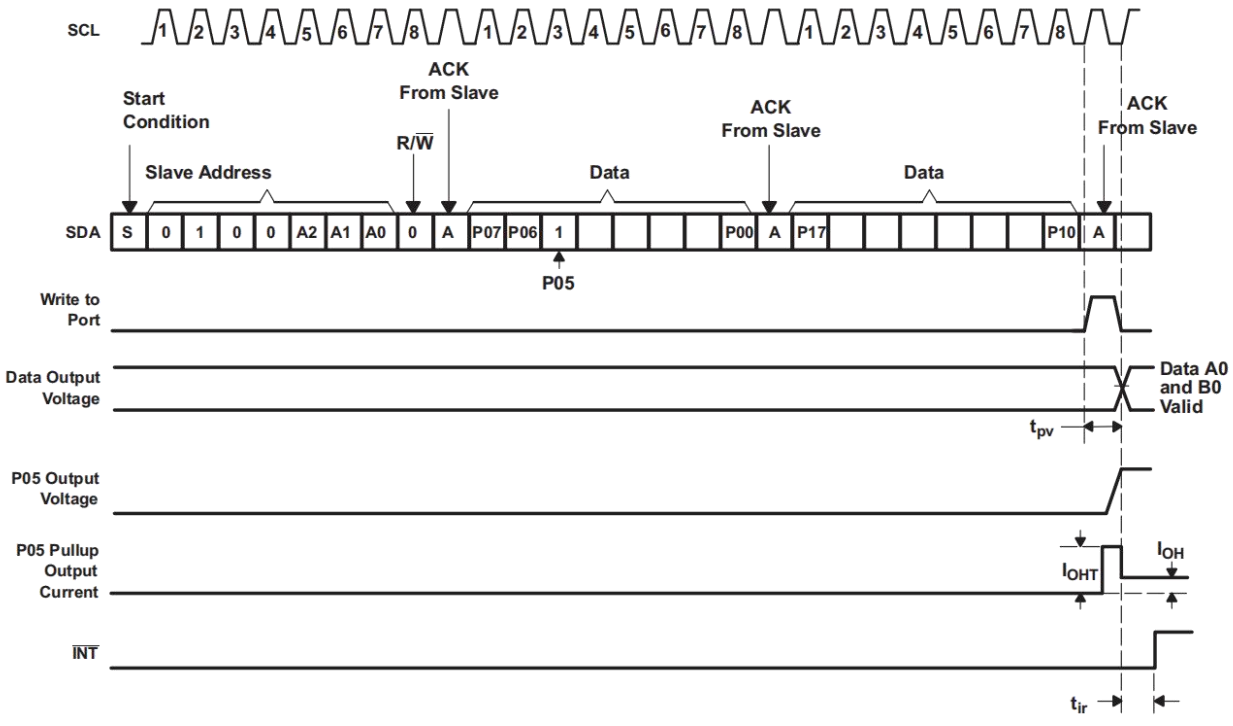



**Figure 18. Write Mode (Output)**

## Device Functional Modes (continued)

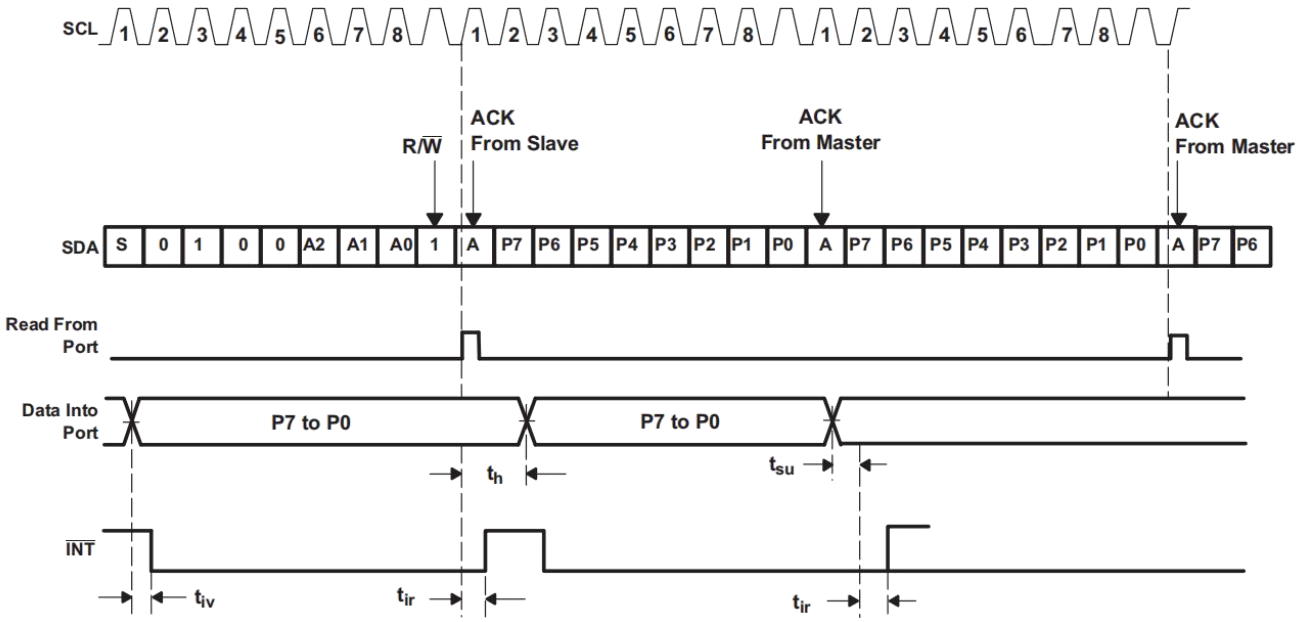
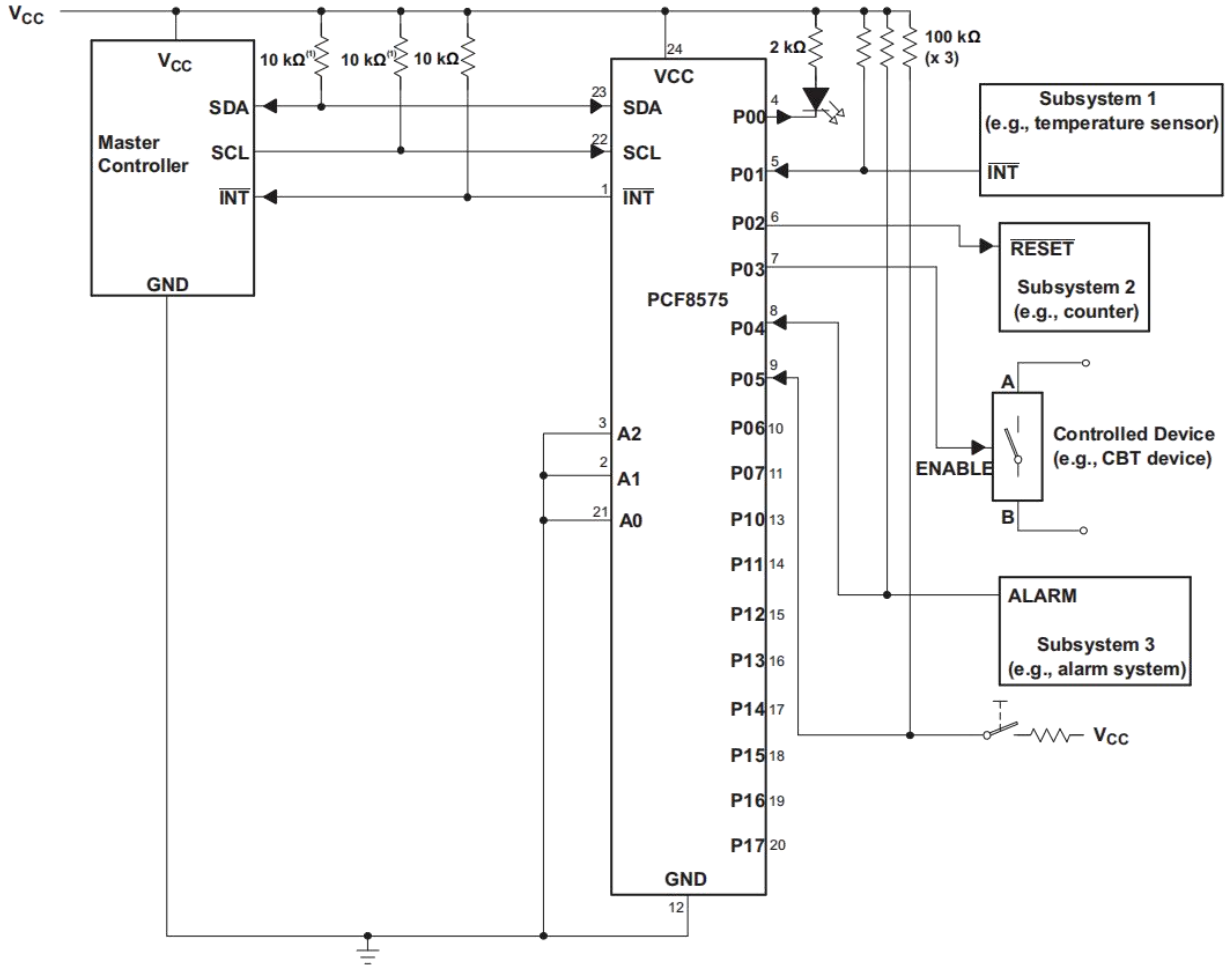



**Figure 19. Read Mode (Input)**

## Typical Application




The SCL and SDA pins must be tied directly to VCC because if SCL and SDA are tied to an auxiliary power supply that could be powered on while VCC is powered off, then the supply current, ICC, will increase as a result.

A. Device address is configured as 0100000 for this example.

B. P0, P2, and P3 are configured as outputs.

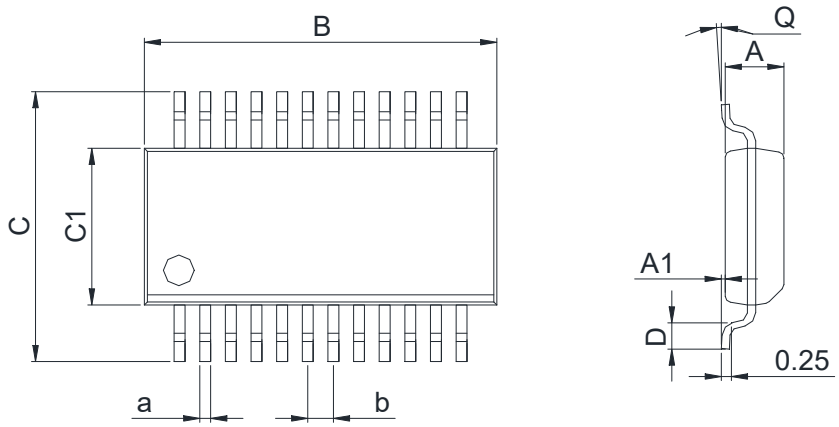
C. P1, P4, and P5 are configured as inputs.

D. P6 and P7 are not used and must be configured as outputs.

**Figure 20. Application Schematic**

## Physical Dimensions

SSOP-24(QSOP-24)




| Dimensions In Millimeters(SSOP-24)(QSOP-24) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Symbol:** | A | A1 | B | C | C1 | D | Q | a | b |
| **Min:** | 1.30 | 0.10 | 8.55 | 5.80 | 3.80 | 0.50 | 0° | 0.23 | 0.63 |
| **Max:** | 1.50 | 0.25 | 8.75 | 6.20 | 4.00 | 0.80 | 8° | 0.31 | TYP |

## Revision History

| DATE | REVISION | PAGE |
|---|---|---|
| 2013-3-5 | New | 1-22 |
| 2023-7-24 | Update encapsulation type | 1 |
| 2024-11-7 | Update Lead Temperature | 4 |

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