

Product Specification

XBLW SN74LS573

Octal D-type transparent latch; 3-state

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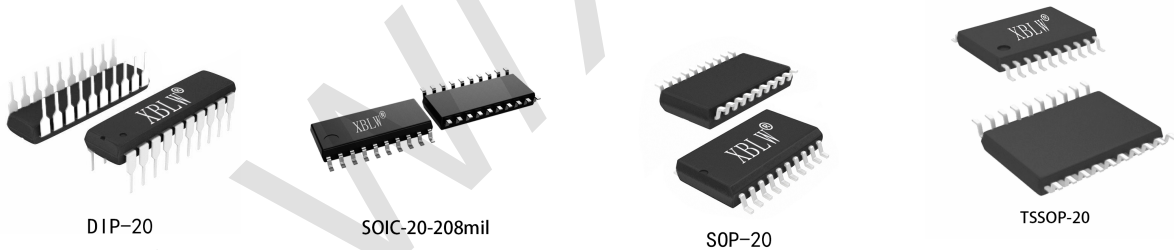


Description

The SN74LS573 is a 8-bit D-type transparent latch with 3-state outputs. The device features latch enable (LE) and output enable ($\overline{OE}$) inputs. When LE is HIGH, data at the inputs enter the latches. In this condition the latches are transparent, a latch output will change each time its corresponding D-input changes. When LE is LOW the latches store the information that was present at the inputs a set-up time preceding the HIGH-to-LOW transition of LE. A HIGH on $\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. Operation of the OE input does not affect the state of the latches. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

Features

- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors and microcomputers
- 3-state non-inverting outputs for bus-oriented applications
- Common 3-state output enable input
- Specified from -20°C to +85°C
- Packaging information: DIP-20/SOP-20/TSSOP-20/SOIC-20-208mil



Ordering Information

Product Model	Package Type	Marking	Packing	Packing Qty
XBLW SN74LS573N	DIP-20	74LS573N	Tube	720Pcs/Box
XBLW SN74LS573DTR	SOP-20	74LS573	Tape	2000Pcs/Reel
XBLW SN74LS573TDTR	TSSOP-20	74LS573	Tape	2000Pcs/Reel
XBLW SN74LS573NSDTR	SOIC-20-208mil	74LS573	Tape	2000Pcs/Reel

Block Diagram

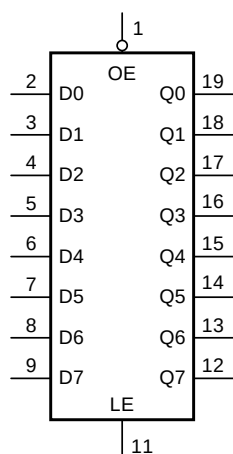


Figure 1. Logic symbol

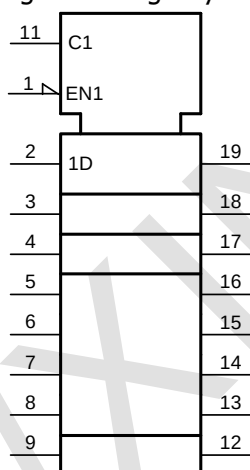


Figure 2. IEC logic symbol

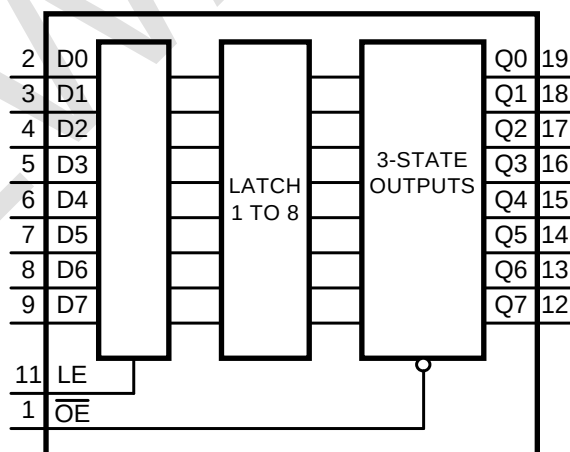


Figure 3. Functional diagram

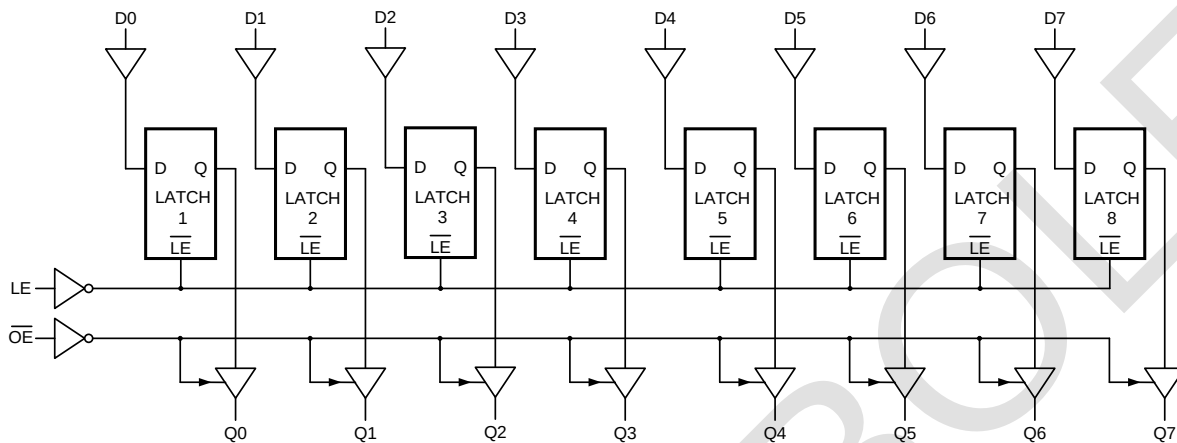
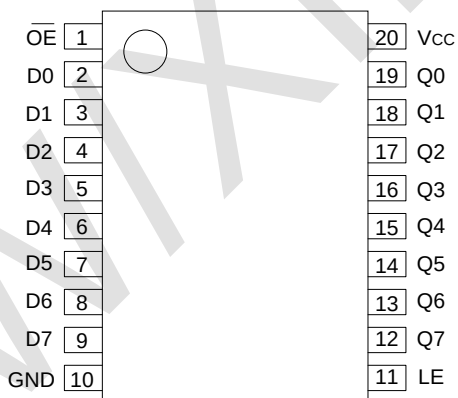


Figure 4. Logic diagram

Pin Configurations



Pin Description

Pin No.	Pin Name	Description
1	$\overline{\text{OE}}$	3-state output enable input (active LOW)
2	D0	data input
3	D1	data input
4	D2	data input
5	D3	data input
6	D4	data input
7	D5	data input
8	D6	data input
9	D7	data input
10	GND	ground (0V)
11	LE	latch enable input (active HIGH)
12	Q7	3-state latch output
13	Q6	3-state latch output
14	Q5	3-state latch output
15	Q4	3-state latch output
16	Q3	3-state latch output
17	Q2	3-state latch output
18	Q1	3-state latch output
19	Q0	3-state latch output
20	V _{CC}	supply voltage

Function Table

Operating mode	Control		Input	Internal latches	Output
	OE	LE	Dn		Qn
Enable and read register (transparent mode)	L	H	L	L	L
			H	H	H
Latch and read register	L	L	l	L	L
			h	H	H
Latch register and disable outputs	H	L	l	L	Z
			h	H	Z

Note: H=HIGH voltage level; L=LOW voltage level; Z=high-impedance OFF-state;

h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition; l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition.

Electrical Parameter

Absolute Maximum Ratings

(Voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage	V_{CC}	-	-0.5	+7.0	V
input clamping current	I_{IK}	$V_I < -0.5V$ or $V_I > V_{CC}+0.5V$	-	± 20	mA
output clamping current	I_{OK}	$V_O < -0.5V$ or $V_O > V_{CC}+0.5V$	-	± 20	mA
output current	I_O	$V_O = -0.5V$ to $(V_{CC}+0.5V)$	-	± 35	mA
supply current	I_{CC}	-	-	+70	mA
ground current	I_{GND}	-	-70	-	mA
storage temperature	T_{stg}	-	-65	+150	°C
total power dissipation	P_{tot}	-	-	500	mW
Soldering temperature	T_L	10s	DIP	245	°C
			SOP/TSSOP	260	°C

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{CC}	-	2.0	5.0	6.0	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
input transition rise and fall rate	$\Delta t/\Delta V$	$V_{CC}=2.0V$	-	-	625	ns/V
		$V_{CC}=4.5V$	-	1.67	139	ns/V
		$V_{CC}=6.0V$	-	-	83	ns/V
ambient temperature	T_{amb}	-	-20	-	+85	°C

Electrical Characteristics

DC Characteristics 1

($T_{amb}=25^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V _{IH}	V _{CC} =2.0V		1.5	1.2	-	V
		V _{CC} =4.5V		3.15	2.4	-	V
		V _{CC} =6.0V		4.2	3.2	-	V
LOW-level input voltage	V _{IL}	V _{CC} =2.0V		-	0.8	0.5	V
		V _{CC} =4.5V		-	2.1	1.35	V
		V _{CC} =6.0V		-	2.8	1.8	V
HIGH-level output voltage	V _{OH}	V _I = V _{IH} or V _{IL}	I _O =-20uA; V _{CC} =2.0V	1.9	2.0	-	V
			I _O =-20uA; V _{CC} =4.5V	4.4	4.5	-	V
			I _O =-20uA; V _{CC} =6.0V	5.9	6.0	-	V
			I _O =-6.0mA; V _{CC} =4.5V	3.98	4.32	-	V
			I _O =-7.8mA; V _{CC} =6.0V	5.48	5.81	-	V
LOW-level output voltage	V _{OL}	V _I = V _{IH} or V _{IL}	I _O =20uA; V _{CC} =2.0V	-	0	0.1	V
			I _O =20uA; V _{CC} =4.5V	-	0	0.1	V
			I _O =20uA; V _{CC} =6.0V	-	0	0.1	V
			I _O =6.0mA; V _{CC} =4.5V	-	0.15	0.26	V
			I _O =7.8mA; V _{CC} =6.0V	-	0.16	0.26	V
input leakage current	I _I	V _I =V _{CC} or GND; V _{CC} =6.0V		-	-	±1.0	uA
OFF-state output current	I _{OZ}	V _I =V _{IH} orV _{IL} ; V _{CC} =6.0V; V _O =V _{CC} or GND		-	-	±1.0	uA
supply current	I _{CC}	V _I =V _{CC} or GND; I _O =0A; V _{CC} =6.0V		-	-	8.0	uA
input capacitance	C _I	-		-	3.5	-	pF

DC Characteristics 2

($T_{amb} = -20^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	$V_{CC}=2.0\text{V}$	1.5	-	-	V
		$V_{CC}=4.5\text{V}$	3.15	-	-	V
		$V_{CC}=6.0\text{V}$	4.2	-	-	V
LOW-level input voltage	V_{IL}	$V_{CC}=2.0\text{V}$	-	-	0.5	V
		$V_{CC}=4.5\text{V}$	-	-	1.35	V
		$V_{CC}=6.0\text{V}$	-	-	1.8	V
HIGH-level output voltage	V_{OH}	$V_I = V_{IH} \text{ or } V_{IL}$	$I_O = -20\mu\text{A}; V_{CC}=2.0\text{V}$	1.9	-	V
			$I_O = -20\mu\text{A}; V_{CC}=4.5\text{V}$	4.4	-	V
			$I_O = -20\mu\text{A}; V_{CC}=6.0\text{V}$	5.9	-	V
			$I_O = -6.0\text{mA}; V_{CC}=4.5\text{V}$	3.84	-	V
			$I_O = -7.8\text{mA}; V_{CC}=6.0\text{V}$	5.34	-	V
LOW-level output voltage	V_{OL}	$V_I = V_{IH} \text{ or } V_{IL}$	$I_O = 20\mu\text{A}; V_{CC}=2.0\text{V}$	-	-	0.1
			$I_O = 20\mu\text{A}; V_{CC}=4.5\text{V}$	-	-	0.1
			$I_O = 20\mu\text{A}; V_{CC}=6.0\text{V}$	-	-	0.1
			$I_O = 6.0\text{mA}; V_{CC}=4.5\text{V}$	-	-	0.33
			$I_O = 7.8\text{mA}; V_{CC}=6.0\text{V}$	-	-	0.33
input leakage current	I_I	$V_I = V_{CC} \text{ or } \text{GND}; V_{CC}=6.0\text{V}$	-	-	± 1.0	μA
OFF-state	I_{OZ}	$V_I = V_{IH} \text{ or } V_{IL}; V_{CC}=6.0\text{V};$ $V_O = V_{CC} \text{ or } \text{GND}$	-	-	± 5.0	μA
output current		$V_O = V_{CC} \text{ or } \text{GND}$				
supply current	I_{CC}	$V_I = V_{CC} \text{ or } \text{GND}; I_O = 0\text{A}; V_{CC}=6.0\text{V}$	-	-	80	μA

AC Characteristics 1

($T_{amb}=25^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
propagation delay	t_{pd}	Dn to Qn; see Figure 6	$V_{CC}=2.0V$	-	47	150	ns
			$V_{CC}=4.5V$	-	17	30	ns
			$V_{CC}=5.0V$; $C_L=15pF$	-	14	-	ns
			$V_{CC}=6.0V$	-	14	26	ns
		LE to Qn; see Figure 7	$V_{CC}=2.0V$	-	50	150	ns
			$V_{CC}=4.5V$	-	18	30	ns
			$V_{CC}=5.0V$; $C_L=15pF$	-	15	-	ns
			$V_{CC}=6.0V$	-	14	26	ns
$\bar{OE}$ to Qn enable time	t_{en}	see Figure 8	$V_{CC}=2.0V$	-	44	140	ns
			$V_{CC}=4.5V$	-	16	28	ns
			$V_{CC}=6.0V$	-	13	24	ns
$\bar{OE}$ to Qn disable time	t_{dis}	see Figure 8	$V_{CC}=2.0V$	-	55	150	ns
			$V_{CC}=4.5V$	-	20	30	ns
			$V_{CC}=6.0V$	-	16	26	ns
transition time	t_t	Qn; see Figure 6	$V_{CC}=2.0V$	-	14	60	ns
			$V_{CC}=4.5V$	-	5	12	ns
			$V_{CC}=6.0V$	-	4	10	ns
pulse width	t_W	LE HIGH; see Figure 7	$V_{CC}=2.0V$	80	14	-	ns
			$V_{CC}=4.5V$	16	5	-	ns
			$V_{CC}=6.0V$	14	4	-	ns
set-up time	t_{su}	Dn to LE; see Figure 9	$V_{CC}=2.0V$	50	11	-	ns
			$V_{CC}=4.5V$	10	4	-	ns
			$V_{CC}=6.0V$	9	3	-	ns
hold time	t_h	Dn to LE; see Figure 9	$V_{CC}=2.0V$	5	3	-	ns
			$V_{CC}=4.5V$	5	1	-	ns
			$V_{CC}=6.0V$	5	1	-	ns
power dissipation capacitance	C_{PD}	$C_L=50pF$, $f=1MHz$; $V_i=GND$ to V_{CC}		-	26	-	pF

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL} .

[2] t_{en} is the same as t_{PZL} and t_{PZH} .

[3] t_{dis} is the same as t_{PLZ} and t_{PHZ} .

[4] t_t is the same as t_{THL} and t_{TLH} .

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D=C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where: f_i =input frequency in MHz;

f_o =output frequency in MHz;

C_L =output load capacitance in pF; V_{CC} =supply voltage in V;

N =number of inputs switching; $\Sigma(C_L \times V_{CC}^2 \times f_o)$ =sum of outputs.

AC Characteristics 2

($T_{amb} = -20^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
propagation delay	t_{pd}	Dn to Qn; see Figure 6	$V_{CC}=2.0\text{V}$	-	-	190 ns
			$V_{CC}=4.5\text{V}$	-	-	38 ns
			$V_{CC}=6.0\text{V}$	-	-	33 ns
		LE to Qn; see Figure 7	$V_{CC}=2.0\text{V}$	-	-	190 ns
			$V_{CC}=4.5\text{V}$	-	-	38 ns
			$V_{CC}=6.0\text{V}$	-	-	33 ns
$\overline{\text{OE}}$ to Qn enable time	t_{en}	see Figure 8	$V_{CC}=2.0\text{V}$	-	-	175 ns
			$V_{CC}=4.5\text{V}$	-	-	35 ns
			$V_{CC}=6.0\text{V}$	-	-	30 ns
$\overline{\text{OE}}$ to Qn disable time	t_{dis}	see Figure 8	$V_{CC}=2.0\text{V}$	-	-	190 ns
			$V_{CC}=4.5\text{V}$	-	-	38 ns
			$V_{CC}=6.0\text{V}$	-	-	33 ns
transition time	t_t	Qn; see Figure 6	$V_{CC}=2.0\text{V}$	-	-	75 ns
			$V_{CC}=4.5\text{V}$	-	-	15 ns
			$V_{CC}=6.0\text{V}$	-	-	13 ns
pulse width	t_w	LE HIGH; see Figure 7	$V_{CC}=2.0\text{V}$	100	-	- ns
			$V_{CC}=4.5\text{V}$	20	-	- ns
			$V_{CC}=6.0\text{V}$	17	-	- ns
set-up time	t_{su}	Dn to LE; see Figure 9	$V_{CC}=2.0\text{V}$	65	-	- ns
			$V_{CC}=4.5\text{V}$	13	-	- ns
			$V_{CC}=6.0\text{V}$	11	-	- ns
hold time	t_h	Dn to LE; see Figure 9	$V_{CC}=2.0\text{V}$	5	-	- ns
			$V_{CC}=4.5\text{V}$	5	-	- ns
			$V_{CC}=6.0\text{V}$	5	-	- ns

Note:

- [1] t_{pd} is the same as t_{PLH} and t_{PHL} .
- [2] t_{en} is the same as t_{PZL} and t_{PZH} .
- [3] t_{dis} is the same as t_{PLZ} and t_{PHZ} .
- [4] t_t is the same as t_{THL} and t_{TLH} .

Measurement Points

Type	Input V_M	Output V_M
SN74LS573	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$

Test Data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
SN74LS573	V_{CC}	6ns	15pF, 50pF	1k Ω	open	GND	V_{CC}

Testing Circuit

AC Testing Circuit

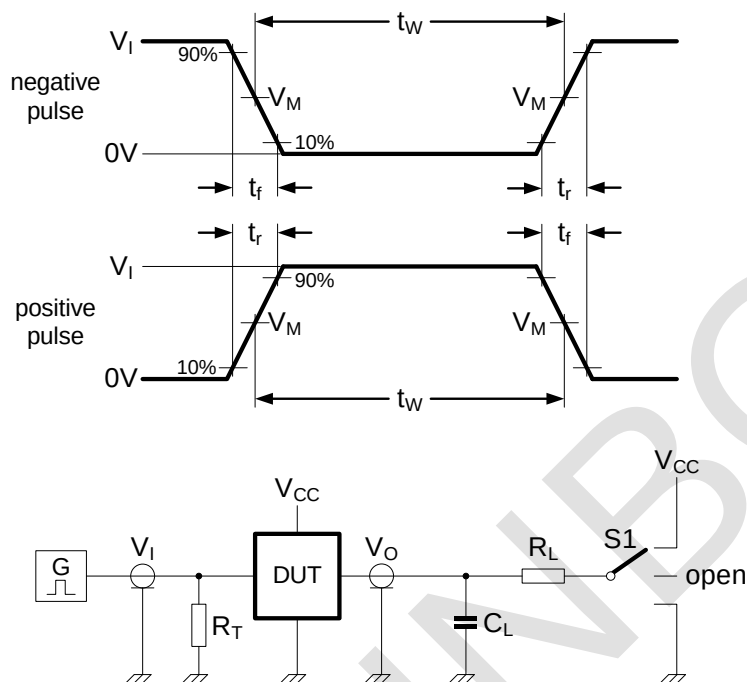


Figure 5. Test circuit for measuring switching times

Definitions for test circuit: R_L =Load resistance.

C_L =Load capacitance including jig and probe capacitance.

R_T =Termination resistance should be equal to the output impedance Z_o of the pulse generator.

S1=Test selection switch.

AC Testing Waveforms

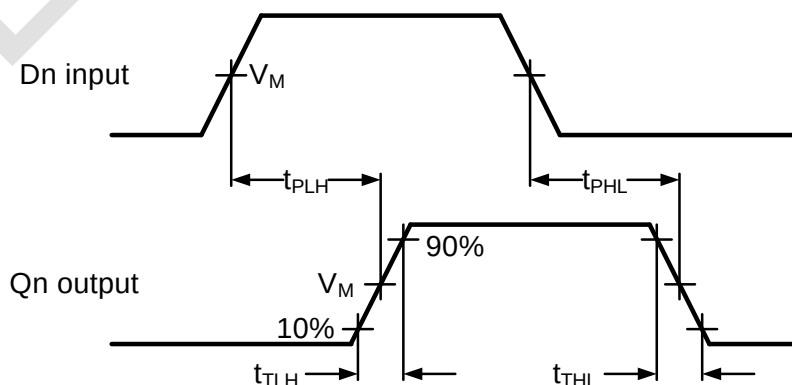


Figure 6. Propagation delay data input (Dn) to output (Qn) and output transition time

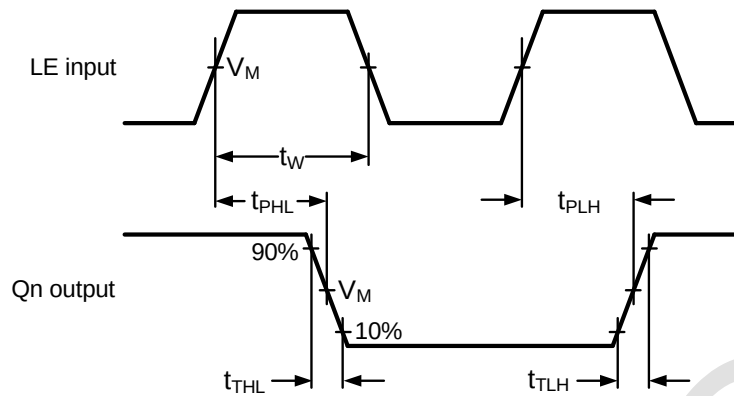


Figure 7. Pulse width latch enable input (LE), propagation delay latch enable input (LE) to output (Qn) and output transition time

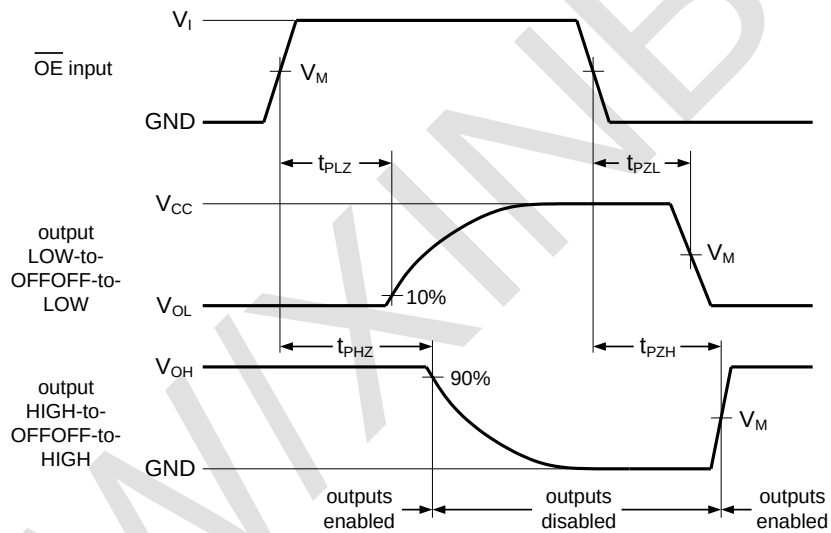


Figure 8. Enable and disable times

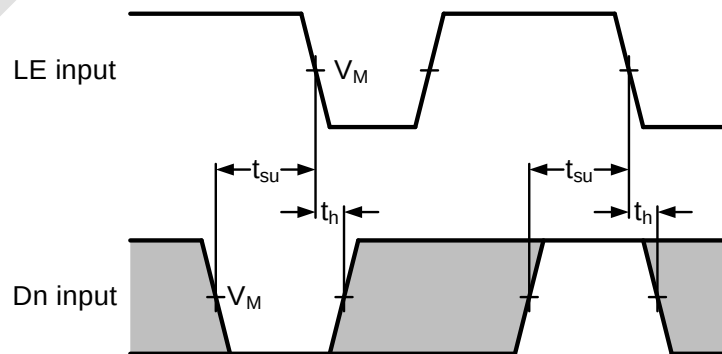
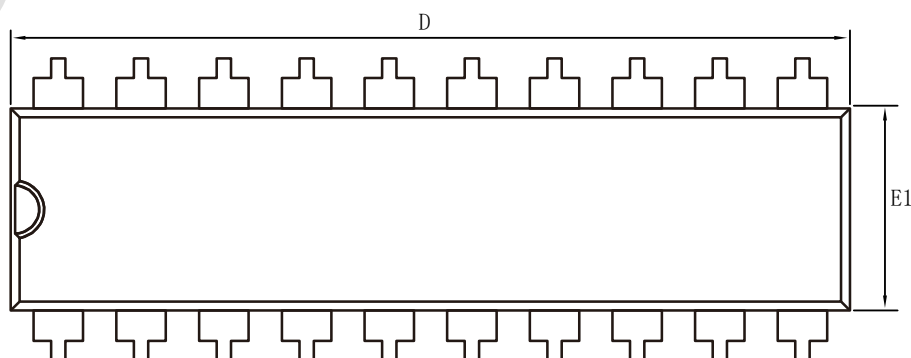
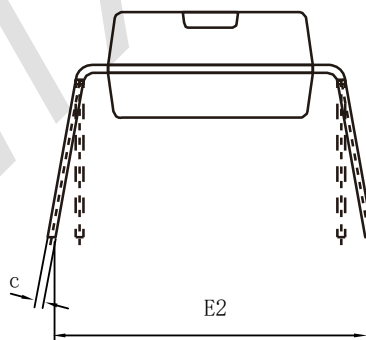
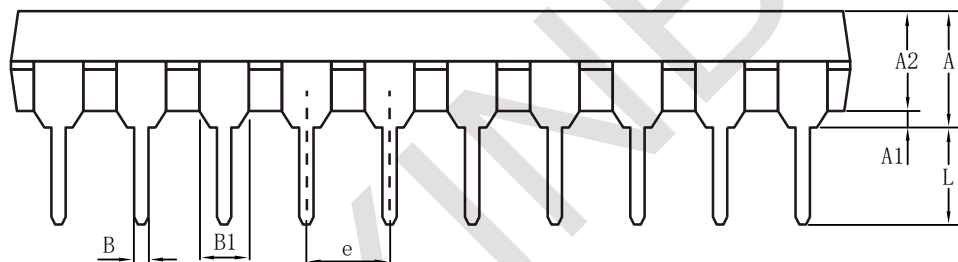


Figure 9. Set-up and hold times for data input (Dn) to latch input (LE)

Package Information

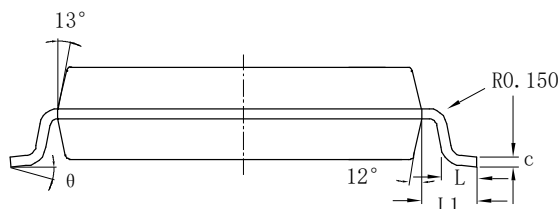
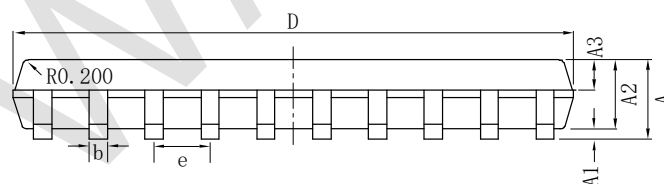
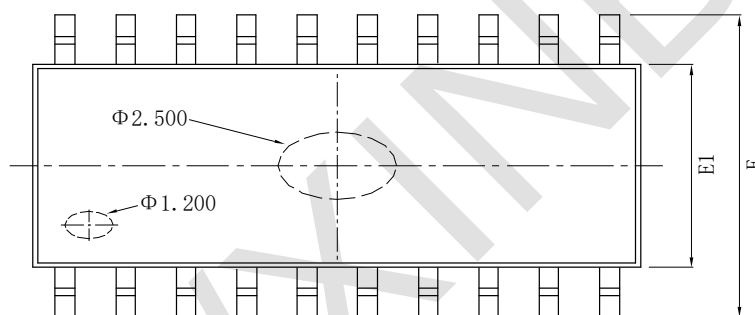
· DIP-20

Symbol	Size	Dimensions In Millimeters		Symbol	Size	Dimensions In Inches	
		Min (mm)	Max (mm)			Min (in)	Max (in)
A		3.600	5.330	A		0.142	0.210
A1		0.510		A1		0.020	
A2		3.200	3.600	A2		0.126	0.142
B		0.360	0.530	B		0.014	0.021
B1		1.52 (BSC)		B1		0.060 (BSC)	
c		0.204	0.360	c		0.008	0.014
D		25.70	26.54	D		1.010	1.040
E1		6.200	6.750	E1		0.244	0.260
E2		7.620	9.300	E2		0.300	0.366
e		2.54 (BSC)		e		0.100 (BSC)	
L		3.000	3.600	L		0.118	0.142



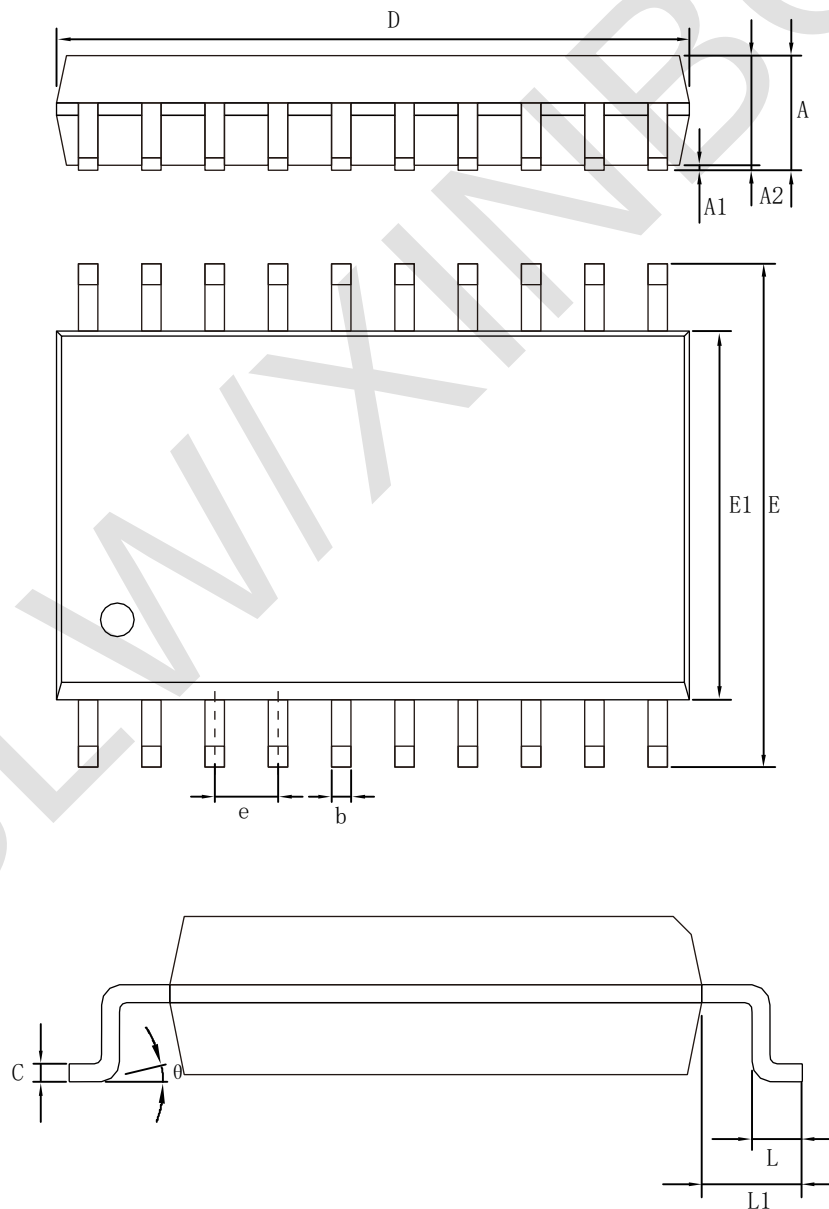
• S01C-20-208mil

Size Symbol	Dimensions In Millimeters		Size Symbol	Dimensions In Inches	
	Min (mm)	Max (mm)		Min (in)	Max (in)
A		2.000	A		0.079
A1	0.050	0.250	A1	0.002	0.010
A2	1.650	1.850	A2	0.065	0.073
b	0.350	0.550	b	0.014	0.022
c	0.150	0.200	c	0.006	0.008
D	12.25	12.65	D	0.482	0.498
E	7.600	8.000	E	0.299	0.315
E1	5.100	5.500	E1	0.201	0.217
e	1.270		e	0.050	
L	0.550	0.950	L	0.022	0.037
L1	1.250		L1	0.049	
θ	0°	8°	θ	0°	8°



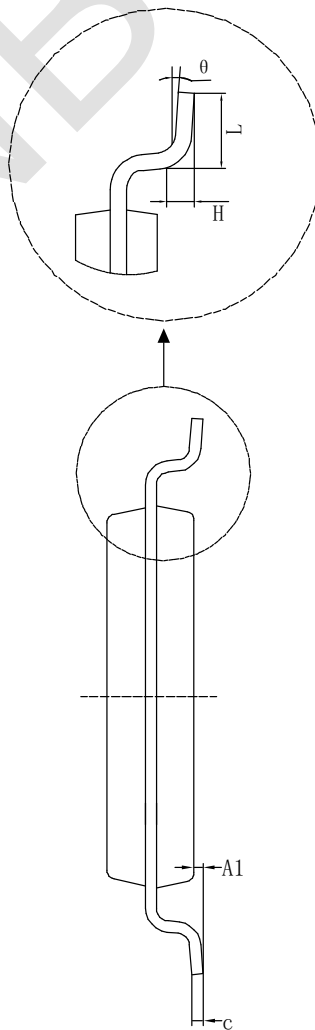
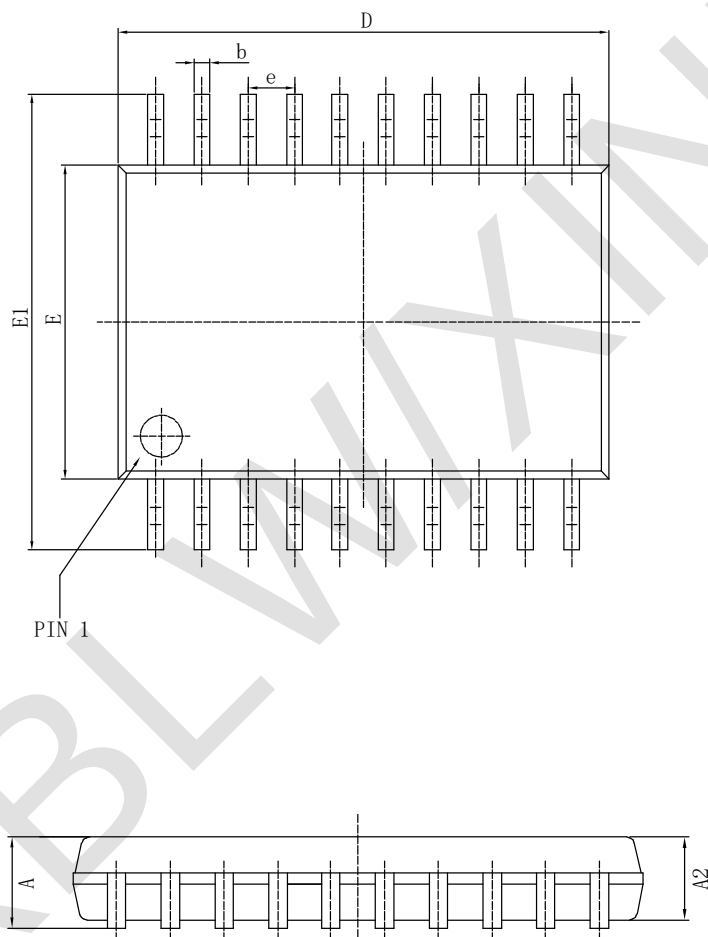
▪ SOP-20

Size Symbol	Dimensions In Millimeters		Size Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A	2.470	2.650	A	0.097	0.104
A1	0.050	0.300	A1	0.002	0.012
A2	2.200	2.440	A2	0.087	0.096
b	0.350	0.500	b	0.014	0.020
c	0.150	0.300	c	0.006	0.012
D	12.54	12.94	D	0.494	0.509
E	10.00	10.60	E	0.394	0.417
E1	7.300	7.700	E1	0.287	0.303
e	1.270(BSC)		e	0.050(BSC)	
L	0.400	1.050	L	0.016	0.041
L1	1.300	1.500	L1	0.051	0.059
θ	0°	8°	θ	0°	8°



· TSSOP-20

Size Symbol	Dimensions In Millimeters		Size Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
D	6.400	6.600	D	0.252	0.259
E	4.300	4.500	E	0.169	0.177
b	0.190	0.300	b	0.007	0.012
c	0.090	0.200	c	0.004	0.008
E1	6.250	6.550	E1	0.246	0.258
A		1.200	A		0.047
A2	0.800	1.000	A2	0.031	0.039
A1	0.050	0.150	A1	0.002	0.006
e	0.65 (BSC)		e	0.026 (BSC)	
L	0.500	0.700	L	0.020	0.028
H	0.25 (TYP)		H	0.01 (TYP)	
θ	1°	7°	θ	1°	7°



Statement

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