

Product Specification

XBLW SN74LS595

8-bit Serial-in, Serial or Parallel-out Shift Register with Output Latches; 3-state

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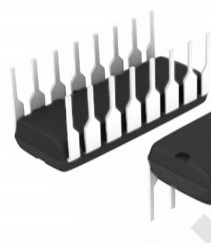
Description

The SN74LS595 is an 8-bit serial-in/serial or parallel-out shift register with a storage register and 3-state outputs. Both the shift and storage register have separate clocks. The device features a serial input (DS) and a serial output (Q7S) to enable cascading and an asynchronous reset $\bar{MR}$ input. A LOW on $\bar{MR}$ will reset the shift register. Data is shifted on the LOW-to-HIGH transitions of the SHCP input. The data in the shift register is transferred to the storage register on a LOW-to-HIGH transition of the STCP input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register. Data in the storage register appears at the output whenever the output enable input ($\bar{OE}$) is LOW.

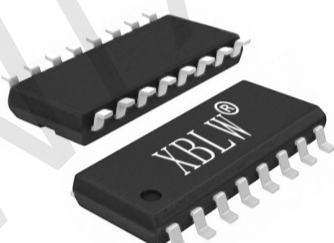
A HIGH on $\bar{OE}$ causes the outputs to assume a high-impedance OFF-state. Operation of the $\bar{OE}$ input does not affect the state of the registers. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

Features

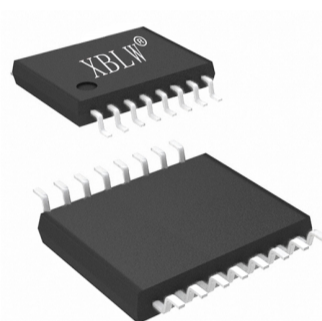
- 8-bit serial input
- 8-bit serial or parallel output
- Storage register with 3-state outputs
- Shift register with direct clear
- Specified from -20°C to +85°C
- Packaging information: DIP-16/SOP-16/TSSOP-16



DIP-16



SOP-16



TSSOP-16

Ordering Information

Product Model	Package Type	Marking	Packing	Packing Qty
XBLW SN74LS595N	DIP-16	74LS595N	Tube	1000Pcs/Box
XBLW SN74LS595DTR	SOP-16	74LS595	Tape	2500Pcs/Reel
XBLW SN74LS595TDTR	TSSOP-16	74LS595	Tape	3000Pcs/Reel

Block Diagram

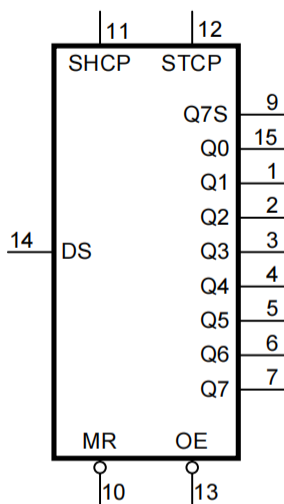


Figure 1. Logic symbol

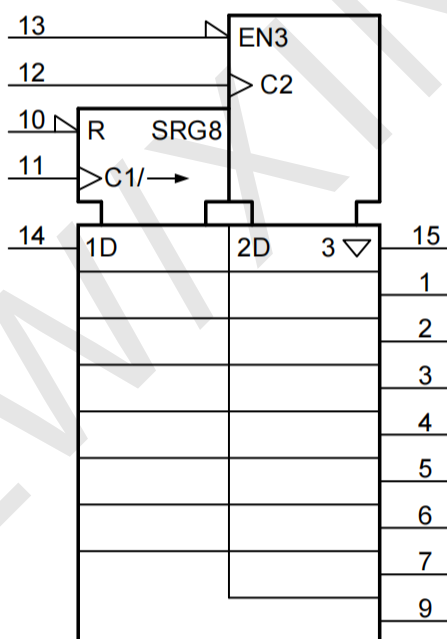


Figure 2. IEC logic symbol

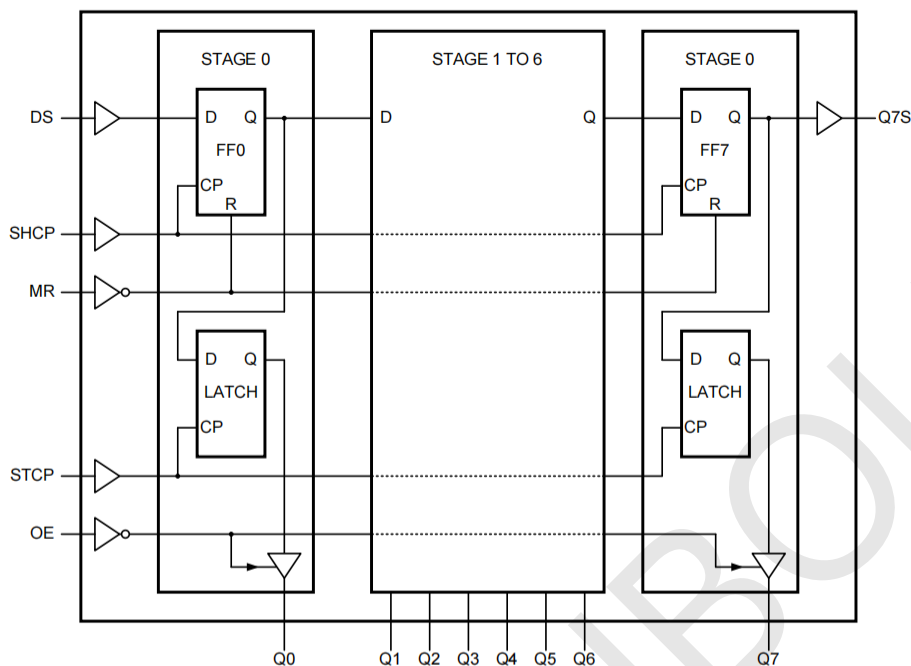


Figure 3. Logic diagram

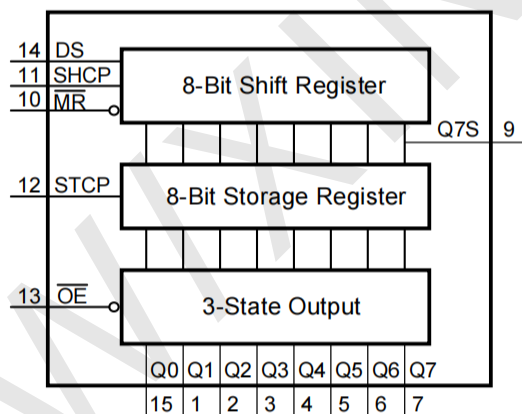
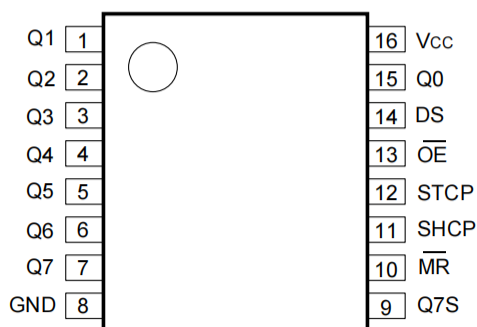


Figure 4. Functional diagram

Pin Configurations



Pin Description

Pin No.	Pin Name	Description
1	Q1	parallel data output
2	Q2	parallel data output
3	Q3	parallel data output
4	Q4	parallel data output
5	Q5	parallel data output
6	Q6	parallel data output
7	Q7	parallel data output
8	GND	ground (0V)
9	Q7S	serial data output
10	$\overline{MR}$	master reset (active LOW)
11	SHCP	shift register clock input
12	STCP	storage register clock input
13	$\overline{OE}$	output enable input (active LOW)
14	DS	serial data input
15	Q0	parallel data output
16	V _{CC}	supply voltage

Function Table

Control				Input	Output		Function
SHCP	STCP	$\bar{OE}$	$\bar{MR}$	DS	Q7S	Qn	
X	X	L	L	X	L	NC	a LOW-level on $\bar{MR}$ only affects the shift registers
X	↑	L	L	X	L	L	empty shift register loaded into storage register
X	X	H	L	X	L	Z	shift register clear; parallel outputs in high-impedance OFF-state
↑	X	L	H	H	Q6S	NC	Logic HIGH-level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q6S) appears on the serial output (Q7S)
X	↑	L	H	X	NC	QnS	Contents of shift register stages (internal QnS) are transferred to the storage register and parallel output stages
↑	↑	L	H	X	Q6S	QnS	Contents of shift register shifted through; previous contents of the shift register is transferred to the storage register and the parallel output stages

Note: H=HIGH voltage level; L=LOW voltage level; Z=high-impedance OFF-state;
↑=LOW-to-HIGH transition; X=don't care; NC=no change.

Electrical Parameter

Absolute Maximum Ratings

(Voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage	V_{CC}	-	-0.5	+7.0	V
input clamping current	I_{IK}	$V_I < -0.5V$ or $V_I > V_{CC}+0.5V$	-	± 20	mA
output clamping current	I_{OK}	$V_O < -0.5V$ or $V_O > V_{CC}+0.5V$	-	± 20	mA
output current	I_O	$V_O = -0.5V$ to $(V_{CC}+0.5V)$	-	± 25	mA
		pin Q7S pins Qn		± 35	mA
supply current	I_{CC}	-	-	70	mA
ground current	I_{GND}	-	-70	-	mA
storage temperature	T_{stg}	-	-65	+150	°C
total power dissipation	P_{tot}	-	-	500	mW
soldering emperature	T_L	10s	DIP	245	°C
			SOP/TSSOP	260	°C

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
SN74LS595						
supply voltage	V_{CC}	-	2.0	5.0	6.0	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
ambient temperature	T_{amb}	-	-20	-	+85	°C

Electrical Characteristics

DC Characteristics 1

($T_{amb} = -20^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V _{IH}	V _{CC} =2.0V		1.5	1.2	-	V
		V _{CC} =4.5V		3.15	2.4	-	V
		V _{CC} =6.0V		4.2	3.2	-	V
LOW-level input voltage	V _{IL}	V _{CC} =2.0V		-	0.8	0.5	V
		V _{CC} =4.5V		-	1.35	1.0	V
		V _{CC} =6.0V		-	1.8	1.5	V
HIGH-level output voltage	V _{OH}	V _I = V _{IH} or V _{IL}	all outputs; I _O =-20uA; V _{CC} =2.0V	1.9	2.0	-	V
			all outputs; I _O =-20uA; V _{CC} =4.5V	4.4	4.5	-	V
			all outputs; I _O =-20uA; V _{CC} =6.0V	5.9	6.0	-	V
			Q7S output; I _O =-4.0mA; V _{CC} =4.5V	3.84	4.32	-	V
			Q7S output; I _O =-5.2mA; V _{CC} =6.0V	5.34	5.81	-	V
			Qn bus driver outputs; I _O =- 6.0mA; V _{CC} =4.5V	3.84	4.32	-	V
			Qn bus driver outputs; I _O =-7.8mA; V _{CC} =6.0V	5.34	5.81	-	V
LOW-level output voltage	V _{OL}	V _I = V _{IH} or V _{IL}	all outputs; I _O =20uA; V _{CC} =2.0V	-	0	0.1	V
			all outputs; I _O =20uA; V _{CC} =4.5V	-	0	0.1	V
			all outputs; I _O =20uA; V _{CC} =6.0V	-	0	0.1	V
			Q7S output; I _O =4.0mA; V _{CC} =4.5V	-	0.15	0.33	V
			Q7S output; I _O =5.2mA; V _{CC} =6.0V	-	0.16	0.33	V
			Qn bus driver outputs; I _O =6.0mA; V _{CC} =4.5V	-	0.15	0.33	V
			Qn bus driver outputs; I _O =7.8mA; V _{CC} =6.0V	-	0.16	0.33	V
input leakage current	I _I	V _I =V _{CC} or GND; V _{CC} =6.0V		-	-	±1.0	uA
OFF-state output current	I _{OZ}	V _I =V _{IH} or V _{IL} ; V _{CC} =6.0V; V _O =V _{CC} or GND		-	-	±5.0	uA
supply current	I _{CC}	V _I =V _{CC} or GND; I _O =0A; V _{CC} =6.0V		-	-	80	uA
input capacitance	C _I	-		-	3.5	-	pF

AC Characteristics 1

($T_{amb}=25^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ. ^[1]	Max.	Unit
propagation delay	t_{PLH}, t_{PHL}	SHCP to Q7S; see Figure 6	$V_{CC}=2.0\text{V}$	-	75	160 ns
			$V_{CC}=4.5\text{V}$	-	19	32 ns
			$V_{CC}=6.0\text{V}$	-	15	27 ns
		STCP to Qn; see Figure 7	$V_{CC}=2.0\text{V}$	-	85	175 ns
			$V_{CC}=4.5\text{V}$	-	20	35 ns
			$V_{CC}=6.0\text{V}$	-	16	30 ns
HIGH to LOW propagation delay	t_{PHL}	MR to Q7S; see Figure 9	$V_{CC}=2.0\text{V}$	-	47	175 ns
			$V_{CC}=4.5\text{V}$	-	17	35 ns
			$V_{CC}=6.0\text{V}$	-	14	30 ns
$\overline{\text{OE}}$ to Qn enable time	t_{PZH}, t_{PZL}	see Figure 10	$V_{CC}=2.0\text{V}$	-	47	150 ns
			$V_{CC}=4.5\text{V}$	-	17	30 ns
			$V_{CC}=6.0\text{V}$	-	14	26 ns
$\overline{\text{OE}}$ to Qn disable time	t_{PLZ}, t_{PHZ}	see Figure 10	$V_{CC}=2.0\text{V}$	-	41	150 ns
			$V_{CC}=4.5\text{V}$	-	15	30 ns
			$V_{CC}=6.0\text{V}$	-	12	27 ns
pulse width	t_w	SHCP HIGH or LOW; see Figure 6	$V_{CC}=2.0\text{V}$	75	17	- ns
			$V_{CC}=4.5\text{V}$	15	6	- ns
			$V_{CC}=6.0\text{V}$	13	5	- ns
		STCP HIGH or LOW; see Figure 7	$V_{CC}=2.0\text{V}$	75	11	- ns
			$V_{CC}=4.5\text{V}$	15	4	- ns
			$V_{CC}=6.0\text{V}$	13	3	- ns
		MR LOW; see Figure 9	$V_{CC}=2.0\text{V}$	75	17	- ns
			$V_{CC}=4.5\text{V}$	15	6	- ns
			$V_{CC}=6.0\text{V}$	13	5	- ns
set-up time	t_{su}	DS to SHCP; see Figure 8	$V_{CC}=2.0\text{V}$	50	11	- ns
			$V_{CC}=4.5\text{V}$	10	4	- ns
			$V_{CC}=6.0\text{V}$	9	3	- ns
		SHCP to STCP; see Figure 7	$V_{CC}=2.0\text{V}$	75	22	- ns
			$V_{CC}=4.5\text{V}$	15	8	- ns
			$V_{CC}=6.0\text{V}$	13	7	- ns
DS to SHCP hold time	t_h	see Figure 8	$V_{CC}=2.0\text{V}$	3	-6	- ns
			$V_{CC}=4.5\text{V}$	3	-2	- ns
			$V_{CC}=6.0\text{V}$	3	-2	- ns
$\overline{\text{MR}}$ to SHCP recovery time	t_{rec}	see Figure 9	$V_{CC}=2.0\text{V}$	50	-19	- ns
			$V_{CC}=4.5\text{V}$	10	-7	- ns
			$V_{CC}=6.0\text{V}$	9	-6	- ns
maximum frequency	f_{max}	SHCP or STCP; see Figure 6 and Figure 7	$V_{CC}=2.0\text{V}$	9	-	- MHz
			$V_{CC}=4.5\text{V}$	30	-	- MHz
			$V_{CC}=6.0\text{V}$	35	-	- MHz

Note:

[1] Typical values are measured at nominal supply voltage.

AC Characteristics 2

($T_{amb} = -20^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
propagation delay	t_{PLH}, t_{PHL}	SHCP to Q7S; see Figure 6	$V_{CC}=2.0\text{V}$	-	-	200 ns
			$V_{CC}=4.5\text{V}$	-	-	40 ns
			$V_{CC}=6.0\text{V}$	-	-	34 ns
		STCP to Qn; see Figure 7	$V_{CC}=2.0\text{V}$	-	-	220 ns
			$V_{CC}=4.5\text{V}$	-	-	44 ns
			$V_{CC}=6.0\text{V}$	-	-	37 ns
HIGH to LOW propagation delay	t_{PHL}	$\overline{\text{MR}}$ to Q7S; see Figure 9	$V_{CC}=2.0\text{V}$	-	-	220 ns
			$V_{CC}=4.5\text{V}$	-	-	44 ns
			$V_{CC}=6.0\text{V}$	-	-	37 ns
$\overline{\text{OE}}$ to Qn enable time	t_{PZH}, t_{PZL}	see Figure 10	$V_{CC}=2.0\text{V}$	-	-	190 ns
			$V_{CC}=4.5\text{V}$	-	-	38 ns
			$V_{CC}=6.0\text{V}$	-	-	33 ns
$\overline{\text{OE}}$ to Qn disable time	t_{PLZ}, t_{PHZ}	see Figure 10	$V_{CC}=2.0\text{V}$	-	-	190 ns
			$V_{CC}=4.5\text{V}$	-	-	38 ns
			$V_{CC}=6.0\text{V}$	-	-	33 ns
pulse width	t_W	SHCP HIGH or LOW; see Figure 6	$V_{CC}=2.0\text{V}$	95	-	- ns
			$V_{CC}=4.5\text{V}$	19	-	- ns
			$V_{CC}=6.0\text{V}$	16	-	- ns
		STCP HIGH or LOW; see Figure 7	$V_{CC}=2.0\text{V}$	95	-	- ns
			$V_{CC}=4.5\text{V}$	19	-	- ns
			$V_{CC}=6.0\text{V}$	16	-	- ns
		$\overline{\text{MR}}$ LOW; see Figure 9	$V_{CC}=2.0\text{V}$	95	-	- ns
			$V_{CC}=4.5\text{V}$	19	-	- ns
			$V_{CC}=6.0\text{V}$	16	-	- ns
set-up time	t_{su}	DS to SHCP; see Figure 8	$V_{CC}=2.0\text{V}$	65	-	- ns
			$V_{CC}=4.5\text{V}$	13	-	- ns
			$V_{CC}=6.0\text{V}$	11	-	- ns
		SHCP to STCP; see Figure 7	$V_{CC}=2.0\text{V}$	95	-	- ns
			$V_{CC}=4.5\text{V}$	19	-	- ns
			$V_{CC}=6.0\text{V}$	16	-	- ns
DS to SHCP hold time	t_h	see Figure 8	$V_{CC}=2.0\text{V}$	3	-	- ns
			$V_{CC}=4.5\text{V}$	3	-	- ns
			$V_{CC}=6.0\text{V}$	3	-	- ns
$\overline{\text{MR}}$ to SHCP recovery time	t_{rec}	see Figure 9	$V_{CC}=2.0\text{V}$	65	-	- ns
			$V_{CC}=4.5\text{V}$	13	-	- ns
			$V_{CC}=6.0\text{V}$	11	-	- ns
maximum frequency	f_{max}	SHCP or STCP; see Figure 6 and Figure 7	$V_{CC}=2.0\text{V}$	4.8	-	- MHz
			$V_{CC}=4.5\text{V}$	24	-	- MHz
			$V_{CC}=6.0\text{V}$	28	-	- MHz

Testing Circuit

AC Testing Circuit

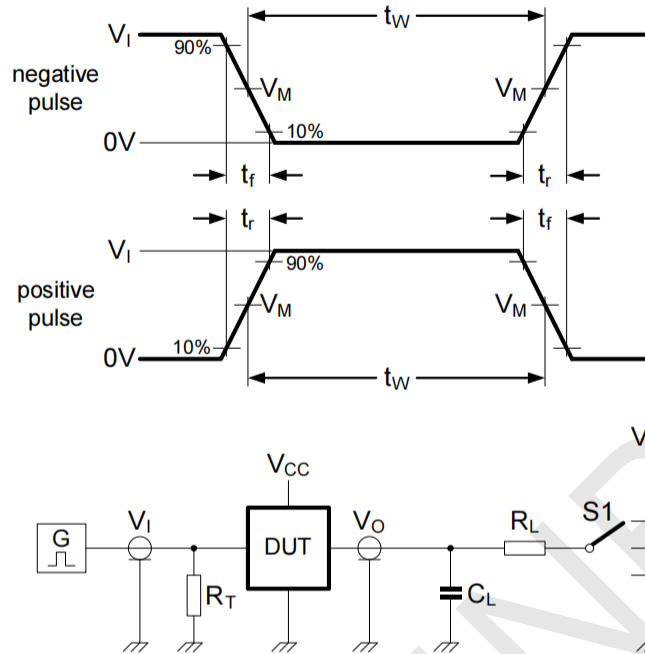


Figure 5. Test circuit for measuring switching times

Definitions for test circuit: R_L =Load resistance.

C_L =Load capacitance including jig and probe capacitance.

R_T =Termination resistance should be equal to the output impedance Z_o of the pulse generator.

S1=Test selection switch.

AC Testing Waveforms

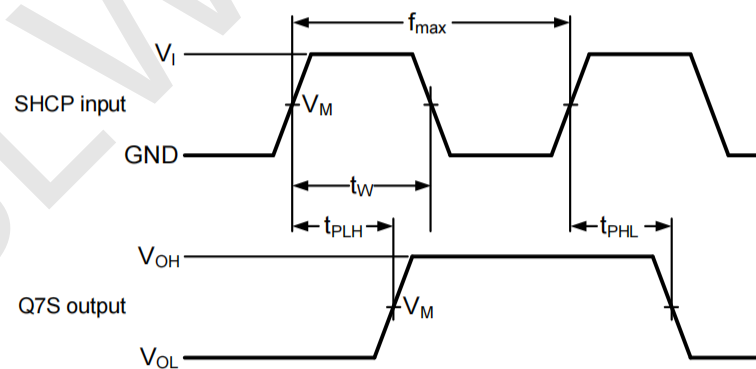


Figure 6. Shift clock pulse, maximum frequency and input to output propagation delays

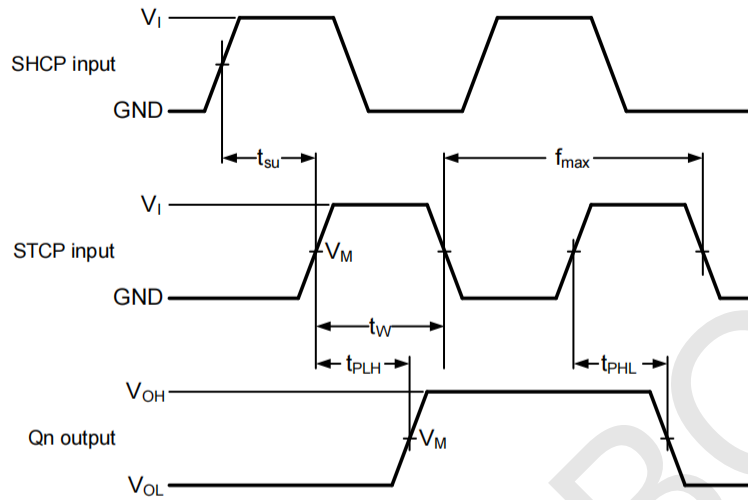


Figure 7. Storage clock to output propagation delays

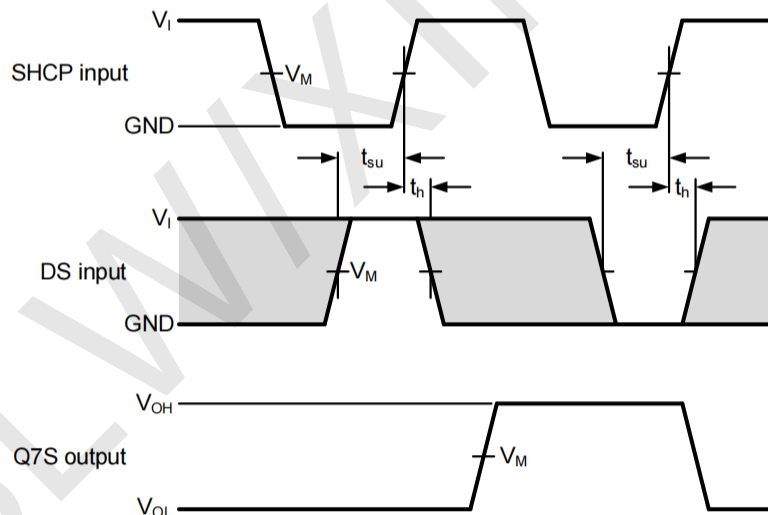


Figure 8. Data set-up and hold times

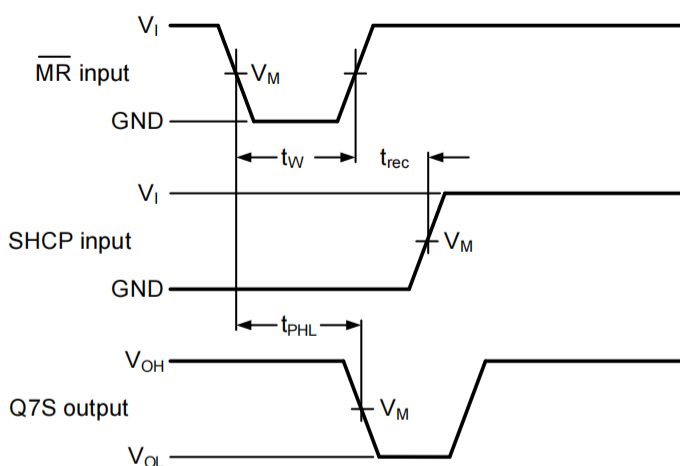


Figure 9. Master reset to output propagation delays

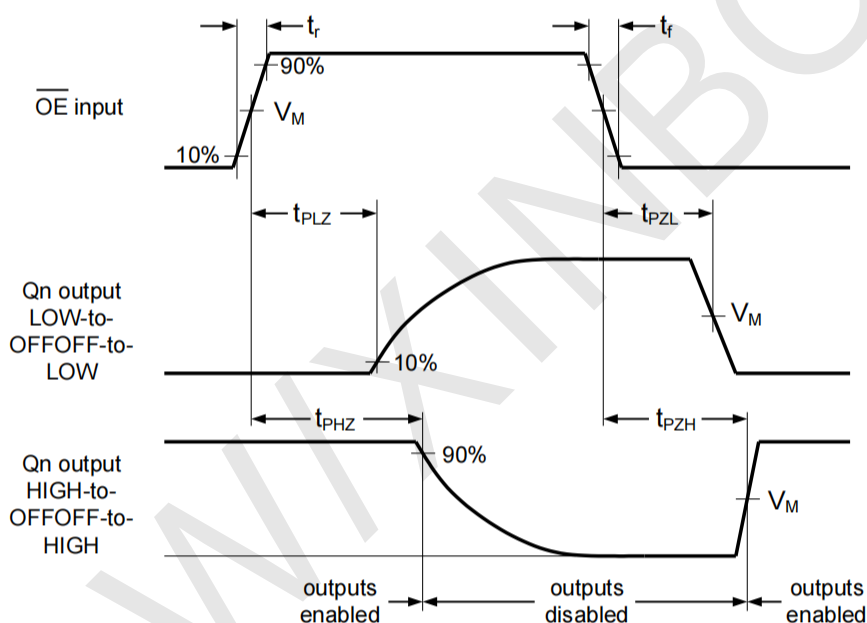


Figure 10. Enable and disable times

Measurement Points

Type	Input	Output
	V_M	V_M
SN74LS595	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$

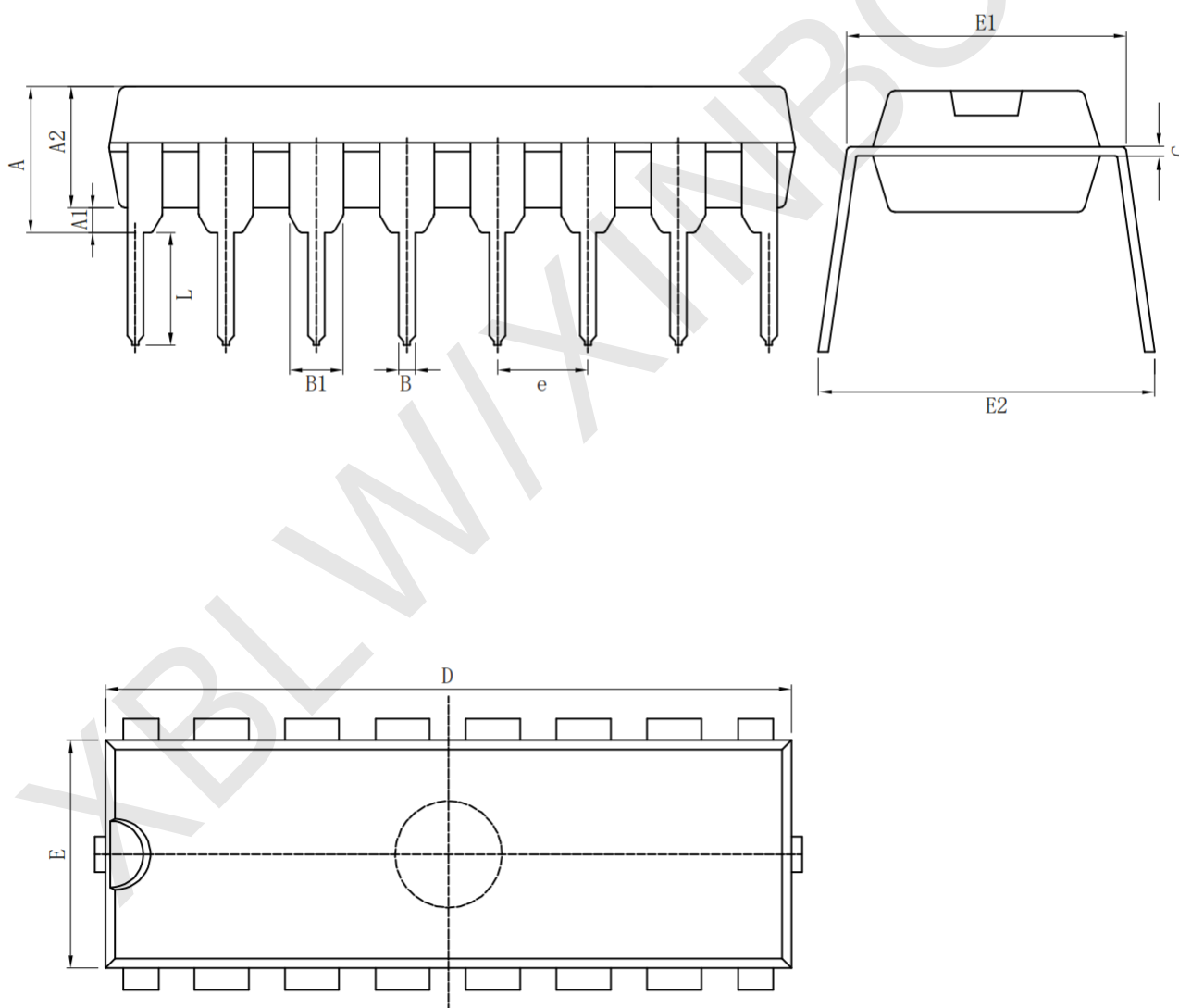
Test Data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
SN74LS595	V_{CC}	6ns	50pF	1kΩ	open	GND	V_{CC}

Package Information

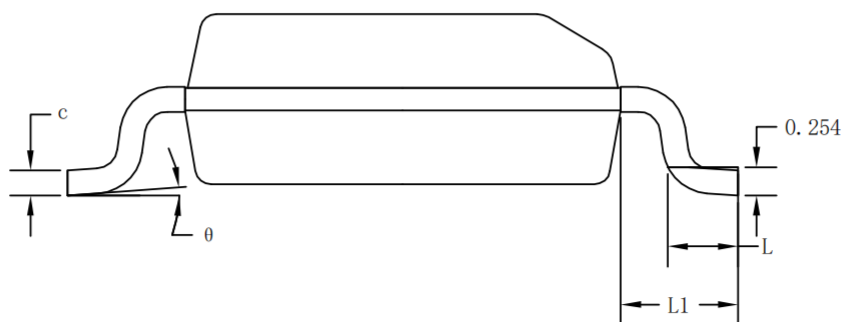
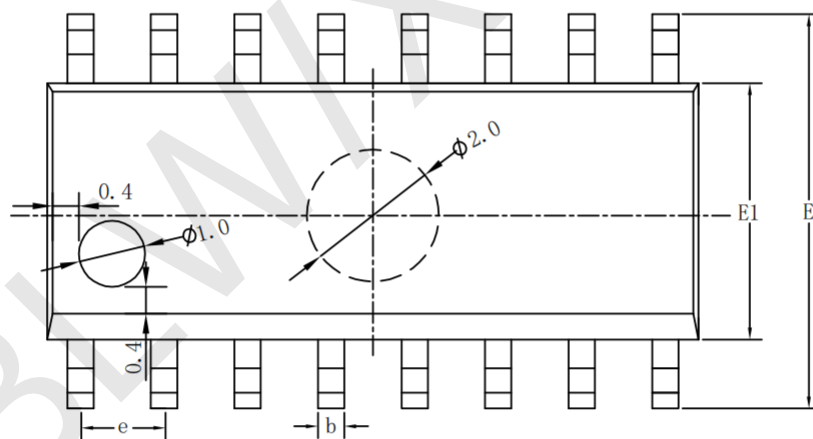
· DIP-16

Symbol	Size	Dimensions In Millimeters		Symbol	Size	Dimensions In Inches	
		Min(mm)	Max(mm)			Min(in)	Max(in)
A		3.710	4.310	A		0.146	0.170
A1		0.510		A1		0.020	
A2		3.200	3.600	A2		0.126	0.142
B		0.380	0.570	B		0.015	0.022
B1		1.524 (BSC)		B1		0.060 (BSC)	
C		0.204	0.360	C		0.008	0.014
D		18.80	19.20	D		0.740	0.756
E		6.200	6.600	E		0.244	0.260
E1		7.320	7.920	E1		0.288	0.312
e		2.540 (BSC)		e		0.100 (BSC)	
L		3.000	3.600	L		0.118	0.142
E2		8.400	9.000	E2		0.331	0.354



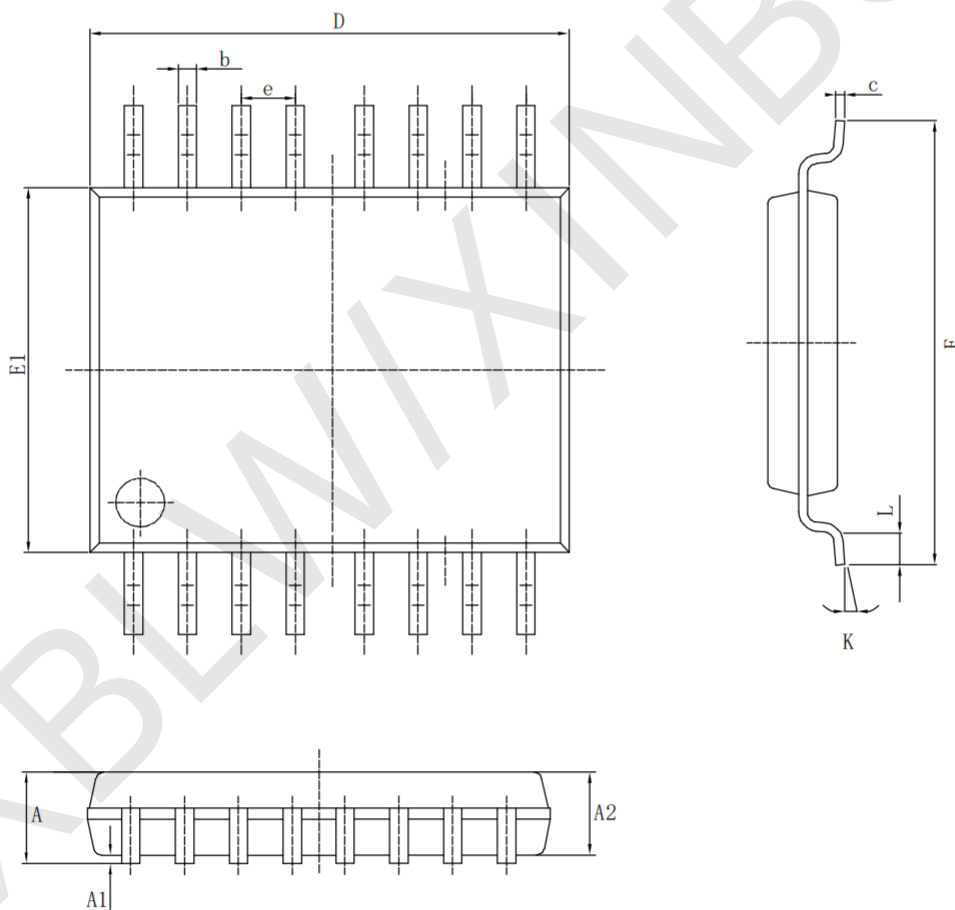
· SOP-16

Symbol	Size	Dimensions In Millimeters			Symbol	Size	Dimensions In Inches		
		Min (mm)	Nom (mm)	Max (mm)			Min (in)	Nom (in)	Max (in)
A		1.500	1.600	1.700	A		0.059	0.063	0.067
A1		0.100	0.150	0.250	A1		0.004	0.006	0.010
A2		1.400	1.450	1.500	A2		0.055	0.057	0.059
A3		0.600	0.650	0.700	A3		0.024	0.026	0.028
b		0.300	0.400	0.500	b		0.012	0.016	0.020
c		0.150	0.200	0.250	c		0.006	0.008	0.010
D		9.800	9.900	10.00	D		0.386	0.390	0.394
E		5.800	6.000	6.200	E		0.228	0.236	0.244
E1		3.850	3.900	3.950	E1		0.152	0.154	0.156
e		1.27 (BSC)			e		0.050 (BSC)		
L		0.500	0.600	0.700	L		0.020	0.024	0.028
L1		1.05 (BSC)			L1		0.041 (BSC)		
θ		0°	4°	8°	θ		0°	4°	8°



· TSSOP-16

Symbol	Dimensions In Millimeters		Symbol	Dimensions In Inches	
	Min (mm)	Max (mm)		Min (in)	Max (in)
A		1.200	A		0.047
A1	0.050	0.150	A1	0.002	0.006
A2	0.800	1.050	A2	0.031	0.041
b	0.190	0.300	b	0.007	0.012
c	0.090	0.200	c	0.004	0.0089
D	4.900	5.100	D	0.193	0.201
E	6.200	6.600	E	0.244	0.260
E1	4.300	4.480	E1	0.169	0.176
e	0.65 (BSC)		e	0.0256 (BSC)	
K	0°	8°	K	0°	8°
L	0.450	0.750	L	0.018	0.030



Statement

- XBLW reserves the right to modify the product manual without prior notice! Before placing an order, customers need to confirm whether the obtained information is the latest version and verify the completeness of the relevant information.
- Any semi-guide product is subject to failure or malfunction under specified conditions. It is the buyer's responsibility to comply with safety standards when using XBLW products for system design and whole machine manufacturing. And take the appropriate safety measures to avoid the potential in the risk of loss of personal injury or loss of property situation!
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