

Product Specification

XBLW SN74LS259

8-bit addressable latch

WEB | www.xinboleic.com

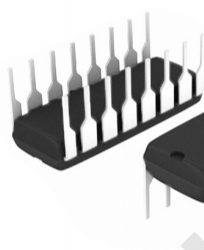


Description

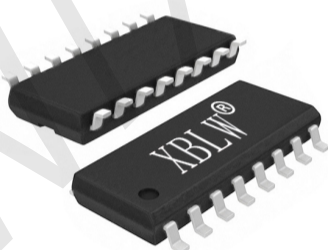
The SN74LS259 is an 8-bit addressable latch. The device features four modes of operation. In the addressable latch mode, data on the D input is written into the latch addressed by the inputs A0 to A3. The addressed latch will follow the data input, non-addressed latches will retain their previous states. In memory mode, all latches retain their previous states and are unaffected by the data or address inputs. In the 3-to-8 decoding or demultiplexing mode, the addressed output follows the D input and all other outputs are LOW. In the reset mode, all outputs are forced LOW and unaffected by the data or address inputs. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

Features

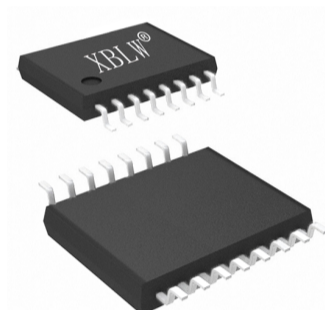
- Combined demultiplexer and 8-bit latch
- Serial-to-parallel capability
- Output from each storage bit available
- Random (addressable) data entry
- Easily expandable
- Common reset input
- Useful as a 3-to-8 active HIGH decoder
- Specified from -20°C to +85°C
- Packaging information: DIP-16/SOP-16/TSSOP-16



DIP-16



SOP-16



TSSOP-16

Ordering Information

Product Model	Package Type	Marking	Packing	Packing Qty
XBLW SN74LS259N	DIP-16	74LS259N	Tube	1000Pcs/Box
XBLW SN74LS259DTR	SOP-16	74LS259	Tape	2500Pcs/Reel
XBLW SN74LS259TDTR	TSSOP-16	74LS259	Tape	3000Pcs/Reel

Block Diagram

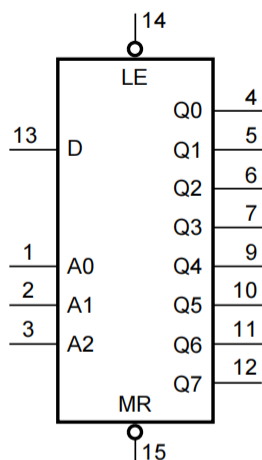


Figure 1. Logic symbol

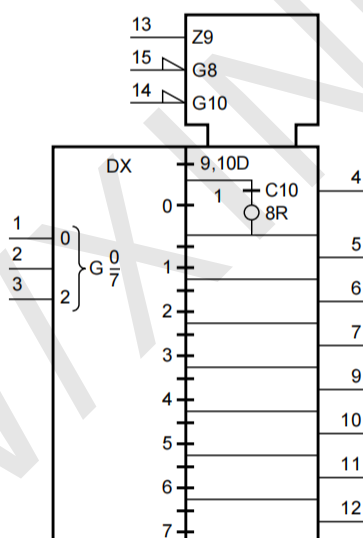


Figure 2. Functional diagram

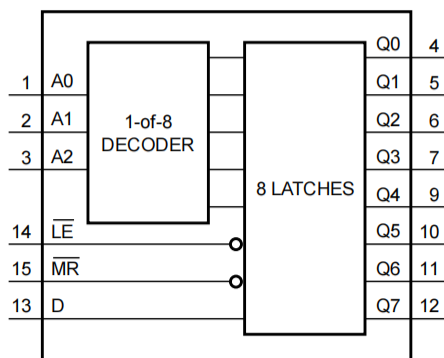
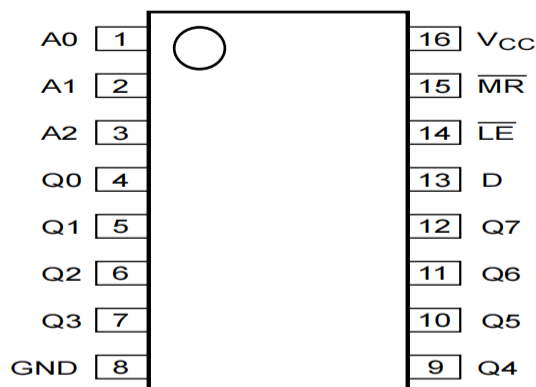


Figure 3. Functional diagram

Pin Configurations



Pin Description

Pin No.	Pin Name	Description
1	A0	address input
2	A1	address input
3	A2	address input
4	Q0	latch output
5	Q1	latch output
6	Q2	latch output
7	Q3	latch output
8	GND	ground (0V)
9	Q4	latch output
10	Q5	latch output
11	Q6	latch output
12	Q7	latch output
13	D	data input
14	$\overline{LE}$	latch enable input (active LOW)
15	$\overline{MR}$	conditional reset input (active LOW)
16	V _{CC}	supply voltage

Function Table

Operating mode	Input						Output							
	$\overline{\text{MR}}$	$\overline{\text{LE}}$	D	A0	A1	A2	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
Reset (clear)	L	H	X	X	X	X	L	L	L	L	L	L	L	L
Demultiplexer (active HIGH 8-channel) decoder (when D=H)	L	L	d	L	L	L	Q=d	L	L	L	L	L	L	L
	L	L	d	H	L	L	L	Q=d	L	L	L	L	L	L
	L	L	d	L	H	L	L	L	Q=d	L	L	L	L	L
	L	L	d	H	H	L	L	L	L	Q=d	L	L	L	L
	L	L	d	L	L	H	L	L	L	L	Q=d	L	L	L
	L	L	d	H	L	H	L	L	L	L	L	Q=d	L	L
	L	L	d	L	H	H	L	L	L	L	L	L	Q=d	L
	L	L	d	H	H	H	L	L	L	L	L	L	L	Q=d
Memory (no action)	H	H	X	X	X	X	q ₀	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
Addressable latch	H	L	d	L	L	L	Q=d	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
	H	L	d	H	L	L	q ₀	Q=d	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
	H	L	d	L	H	L	q ₀	q ₁	Q=d	q ₃	q ₄	q ₅	q ₆	q ₇
	H	L	d	H	H	L	q ₀	q ₁	q ₂	Q=d	q ₄	q ₅	q ₆	q ₇
	H	L	d	L	L	H	q ₀	q ₁	q ₂	q ₃	Q=d	q ₅	q ₆	q ₇
	H	L	d	H	L	H	q ₀	q ₁	q ₂	q ₃	q ₄	Q=d	q ₆	q ₇
	H	L	d	L	H	H	q ₀	q ₁	q ₂	q ₃	q ₄	q ₅	Q=d	q ₇
	H	L	d	H	H	H	q ₀	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	Q=d

Note:

[1] H=HIGH voltage level; L=LOW voltage level; X=don't care.

[2] d=HIGH or LOW data one set-up time prior to the LOW-to-HIGH $\overline{\text{LE}}$ transition.

[3] q=lower case letter indicates the state of the referenced input one set-up time prior to the LOW-to-HIGH transition.

Operating Mode Select Table

$\overline{\text{LE}}$	$\overline{\text{MR}}$	Mode
L	H	Addressable latch mode
H	H	Memory mode
L	L	Demultiplexer mode
H	L	Reset mode

Note: H=HIGH voltage level; L=LOW voltage level.

Electrical Parameter

Absolute Maximum Ratings

(Voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage	V_{CC}	-	-0.5	+7.0	V
input clamping current	I_{IK}	$V_I < -0.5V$ or $V_I > V_{CC}+0.5V$	-	± 20	mA
output clamping current	I_{OK}	$V_O < -0.5V$ or $V_O > V_{CC}+0.5V$	-	± 20	mA
output current	I_O	$V_O = -0.5V$ to $(V_{CC}+0.5V)$	-	± 25	mA
supply current	I_{CC}	-	-	+70	mA
ground current	I_{GND}	-	-70	-	mA
storage temperature	T_{stg}	-	-65	+150	°C
total power dissipation	P_{tot}	-	-	500	mW
Soldering temperature	T_L	10s	DIP	245	°C
			SOP/TSSOP	260	°C

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{CC}	-	2.0	5.0	6.0	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
input transition rise and fall rate	$\Delta t/\Delta V$	$V_{CC}=2.0V$	-	-	625	ns/V
		$V_{CC}=4.5V$	-	1.67	139	ns/V
		$V_{CC}=6.0V$	-	-	83	ns/V
ambient temperature	T_{amb}	-	-20	-	+85	°C

Electrical Characteristics

DC Characteristics 1

($T_{amb}=25^{\circ}C$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	$V_{CC}=2.0V$		1.5	1.2	-	V
		$V_{CC}=4.5V$		3.15	2.4	-	V
		$V_{CC}=6.0V$		4.2	3.2	-	V
LOW-level input voltage	V_{IL}	$V_{CC}=2.0V$		-	0.8	0.5	V
		$V_{CC}=4.5V$		-	2.1	1.35	V
		$V_{CC}=6.0V$		-	2.8	1.8	V
HIGH-level output voltage	V_{OH}	$V_I = V_{IH} \text{ or } V_{IL}$	$I_O=-20\mu A; V_{CC}=2.0V$	1.9	2.0	-	V
			$I_O=-20\mu A; V_{CC}=4.5V$	4.4	4.5	-	V
			$I_O=-20\mu A; V_{CC}=6.0V$	5.9	6.0	-	V
			$I_O=-4.0mA; V_{CC}=4.5V$	3.98	4.32	-	V
			$I_O=-5.2mA; V_{CC}=6.0V$	5.48	5.81	-	V
LOW-level output voltage	V_{OL}	$V_I = V_{IH} \text{ or } V_{IL}$	$I_O=20\mu A; V_{CC}=2.0V$	-	0	0.1	V
			$I_O=20\mu A; V_{CC}=4.5V$	-	0	0.1	V
			$I_O=20\mu A; V_{CC}=6.0V$	-	0	0.1	V
			$I_O=4.0mA; V_{CC}=4.5V$	-	0.15	0.26	V
			$I_O=5.2mA; V_{CC}=6.0V$	-	0.16	0.26	V
input leakage current	I_I	$V_I=V_{CC} \text{ or } GND; V_{CC}=6.0V$		-	-	± 1.0	μA
supply current	I_{CC}	$V_I=V_{CC} \text{ or } GND; I_O=0A; V_{CC}=6.0V$		-	-	8.0	μA
Input capacitance	C_I	-		-	3.5	-	pF

DC Characteristics 2

($T_{amb} = -20^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	$V_{CC}=2.0\text{V}$	1.5	-	-	V
		$V_{CC}=4.5\text{V}$	3.15	-	-	V
		$V_{CC}=6.0\text{V}$	4.2	-	-	V
LOW-level input voltage	V_{IL}	$V_{CC}=2.0\text{V}$	-	-	0.5	V
		$V_{CC}=4.5\text{V}$	-	-	1.35	V
		$V_{CC}=6.0\text{V}$	-	-	1.8	V
HIGH-level output voltage	V_{OH}	$V_I = V_{IH} \text{ or } V_{IL}$	$I_O = -20\mu\text{A}; V_{CC}=2.0\text{V}$	1.9	-	V
			$I_O = -20\mu\text{A}; V_{CC}=4.5\text{V}$	4.4	-	V
			$I_O = -20\mu\text{A}; V_{CC}=6.0\text{V}$	5.9	-	V
			$I_O = -4.0\text{mA}; V_{CC}=4.5\text{V}$	3.84	-	V
			$I_O = -5.2\text{mA}; V_{CC}=6.0\text{V}$	5.34	-	V
LOW-level output voltage	V_{OL}	$V_I = V_{IH} \text{ or } V_{IL}$	$I_O = 20\mu\text{A}; V_{CC}=2.0\text{V}$	-	-	0.1
			$I_O = 20\mu\text{A}; V_{CC}=4.5\text{V}$	-	-	0.1
			$I_O = 20\mu\text{A}; V_{CC}=6.0\text{V}$	-	-	0.1
			$I_O = 4.0\text{mA}; V_{CC}=4.5\text{V}$	-	-	0.33
			$I_O = 5.2\text{mA}; V_{CC}=6.0\text{V}$	-	-	0.33
input leakage current	I_I	$V_I = V_{CC} \text{ or } \text{GND}; V_{CC}=6.0\text{V}$	-	-	± 1.0	μA
supply current	I_{CC}	$V_I = V_{CC} \text{ or } \text{GND}; I_O = 0\text{A}; V_{CC}=6.0\text{V}$	-	-	80	μA
input capacitance	C_I	-	-	-	-	pF

AC Characteristics 1

($T_{amb}=25^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
propagation delay	t_{pd}	D to Qn; see Figure 5	$V_{CC}=2.0\text{V}$	-	58	185 ns
			$V_{CC}=4.5\text{V}$	-	21	37 ns
			$V_{CC}=5.0\text{V}; C_L=15\text{pF}$	-	18	- ns
			$V_{CC}=6.0\text{V}$	-	17	31 ns
		An to Qn; see Figure 6	$V_{CC}=2.0\text{V}$	-	58	185 ns
			$V_{CC}=4.5\text{V}$	-	21	37 ns
			$V_{CC}=5.0\text{V}; C_L=15\text{pF}$	-	17	- ns
			$V_{CC}=6.0\text{V}$	-	17	31 ns
		$\overline{\text{LE}}$ to Qn; see Figure 7	$V_{CC}=2.0\text{V}$	-	55	170 ns
			$V_{CC}=4.5\text{V}$	-	20	34 ns
			$V_{CC}=5.0\text{V}; C_L=15\text{pF}$	-	17	- ns
			$V_{CC}=6.0\text{V}$	-	16	29 ns
HIGH to LOW propagation delay	t_{PHL}	$\overline{\text{MR}}$ to Qn; see Figure 8	$V_{CC}=2.0\text{V}$	-	50	155 ns
			$V_{CC}=4.5\text{V}$	-	18	31 ns
			$V_{CC}=5.0\text{V}; C_L=15\text{pF}$	-	15	- ns
			$V_{CC}=6.0\text{V}$	-	14	26 ns
transition time	t_t	see Figure 7	$V_{CC}=2.0\text{V}$	-	19	75 ns
			$V_{CC}=4.5\text{V}$	-	7	15 ns
			$V_{CC}=6.0\text{V}$	-	6	13 ns
pulse width	t_w	$\overline{\text{LE}}$ HIGH or LOW; see Figure 7	$V_{CC}=2.0\text{V}$	70	17	- ns
			$V_{CC}=4.5\text{V}$	14	6	- ns
			$V_{CC}=6.0\text{V}$	12	5	- ns
		$\overline{\text{MR}}$ LOW; see Figure 8	$V_{CC}=2.0\text{V}$	70	17	- ns
			$V_{CC}=4.5\text{V}$	14	6	- ns
			$V_{CC}=6.0\text{V}$	12	5	- ns
set-up time	t_{su}	D, An to $\overline{\text{LE}}$; see Figure 9 and Figure 10	$V_{CC}=2.0\text{V}$	80	19	- ns
			$V_{CC}=4.5\text{V}$	16	7	- ns
			$V_{CC}=6.0\text{V}$	14	6	- ns
hold time	t_h	D to $\overline{\text{LE}}$; see Figure 9 and Figure 10	$V_{CC}=2.0\text{V}$	0	-19	- ns
			$V_{CC}=4.5\text{V}$	0	-6	- ns
			$V_{CC}=6.0\text{V}$	0	-5	- ns
		An to $\overline{\text{LE}}$; see Figure 9 and Figure 10	$V_{CC}=2.0\text{V}$	2	-11	- ns
			$V_{CC}=4.5\text{V}$	2	-4	- ns
			$V_{CC}=6.0\text{V}$	2	-3	- ns
power dissipation capacitance	C_{PD}	$f_i=1\text{MHz}; V_I=\text{GND to } V_{CC}$	-	19	-	pF

Note:

[1] Typical values are measured at nominal supply voltage ($V_{CC}=3.3\text{V}$ and $V_{CC}=5.0\text{V}$).

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

[3] t_t is the same as t_{THL} and t_{TLH} .

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D=C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

f_i =input frequency in MHz; f_o =output frequency in MHz;

C_L =output load capacitance in pF; V_{CC} =supply voltage in V;

N =number of inputs switching; $\sum (C_L \times V_{CC}^2 \times f_o)$ =sum of outputs.

AC Characteristics 2

($T_{amb} = -20^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
propagation delay	t_{pd}	D to Qn; see Figure 5	$V_{CC}=2.0\text{V}$	-	-	230 ns
			$V_{CC}=4.5\text{V}$	-	-	46 ns
			$V_{CC}=5.0\text{V}; C_L=15\text{pF}$	-	-	- ns
			$V_{CC}=6.0\text{V}$	-	-	39 ns
		An to Qn; see Figure 6	$V_{CC}=2.0\text{V}$	-	-	230 ns
			$V_{CC}=4.5\text{V}$	-	-	46 ns
			$V_{CC}=5.0\text{V}; C_L=15\text{pF}$	-	-	- ns
			$V_{CC}=6.0\text{V}$	-	-	39 ns
		$\overline{\text{LE}}$ to Qn; see Figure 7	$V_{CC}=2.0\text{V}$	-	-	215 ns
			$V_{CC}=4.5\text{V}$	-	-	43 ns
			$V_{CC}=5.0\text{V}; C_L=15\text{pF}$	-	-	- ns
			$V_{CC}=6.0\text{V}$	-	-	37 ns
HIGH to LOW propagation delay	t_{PHL}	$\overline{\text{MR}}$ to Qn; see Figure 8	$V_{CC}=2.0\text{V}$	-	-	195 ns
			$V_{CC}=4.5\text{V}$	-	-	39 ns
			$V_{CC}=5.0\text{V}; C_L=15\text{pF}$	-	-	- ns
			$V_{CC}=6.0\text{V}$	-	-	33 ns
transition time	t_t	see Figure 7	$V_{CC}=2.0\text{V}$	-	-	95 ns
			$V_{CC}=4.5\text{V}$	-	-	19 ns
			$V_{CC}=6.0\text{V}$	-	-	16 ns
pulse width	t_w	$\overline{\text{LE}}$ HIGH or LOW; see Figure 7	$V_{CC}=2.0\text{V}$	90	-	- ns
			$V_{CC}=4.5\text{V}$	18	-	- ns
			$V_{CC}=6.0\text{V}$	15	-	- ns
		$\overline{\text{MR}}$ LOW; see Figure 8	$V_{CC}=2.0\text{V}$	90	-	- ns
			$V_{CC}=4.5\text{V}$	18	-	- ns
			$V_{CC}=6.0\text{V}$	15	-	- ns
set-up time	t_{su}	D, An to $\overline{\text{LE}}$; see Figure 9 and Figure 10	$V_{CC}=2.0\text{V}$	100	-	- ns
			$V_{CC}=4.5\text{V}$	20	-	- ns
			$V_{CC}=6.0\text{V}$	17	-	- ns
hold time	t_h	D to $\overline{\text{LE}}$; see Figure 9 and Figure 10	$V_{CC}=2.0\text{V}$	0	-	- ns
			$V_{CC}=4.5\text{V}$	0	-	- ns
			$V_{CC}=6.0\text{V}$	0	-	- ns
		An to $\overline{\text{LE}}$; see Figure 9 and Figure 10	$V_{CC}=2.0\text{V}$	2	-	- ns
			$V_{CC}=4.5\text{V}$	2	-	- ns
			$V_{CC}=6.0\text{V}$	2	-	- ns
power dissipation capacitance	C_{PD}	$f_i=1\text{MHz}; V_I=\text{GND to } V_{CC}$	-	-	-	pF

Note:

[1] Typical values are measured at nominal supply voltage ($V_{CC}=3.3\text{V}$ and $V_{CC}=5.0\text{V}$).

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

[3] t_t is the same as t_{THL} and t_{TLH} .

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

f_i =input frequency in MHz;

f_o =output frequency in MHz;

C_L =output load capacitance in pF; V_{CC} =supply voltage in V;

N =number of inputs switching; $\sum (C_L \times V_{CC}^2 \times f_o)$ =sum of outputs.

Testing Circuit

AC Testing Circuit

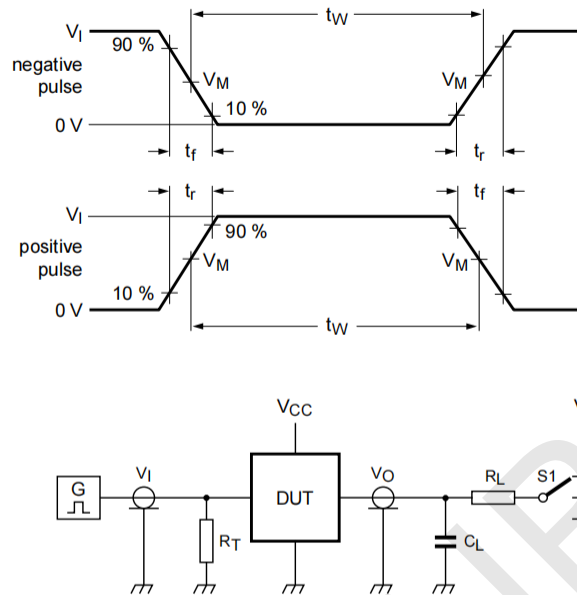


Figure 4. Test circuit for measuring switching times

Definitions for test circuit:

C_L =Load capacitance including jig and probe capacitance.

R_T =Termination resistance should be equal to the output impedance Z_o of the pulse generator.

R_L =Load resistance.

S1=Test selection switch.

AC Testing Waveforms

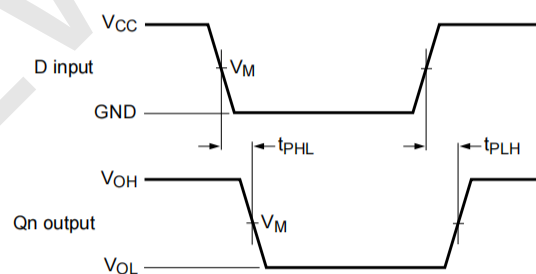


Figure 5. Data input to output propagation delays

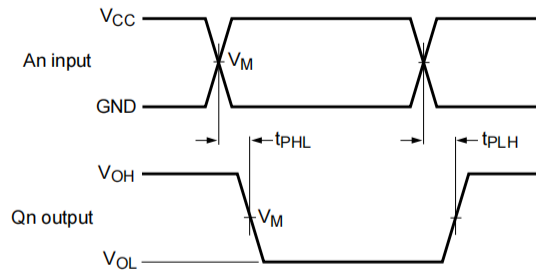


Figure 6. Address input to output propagation delays

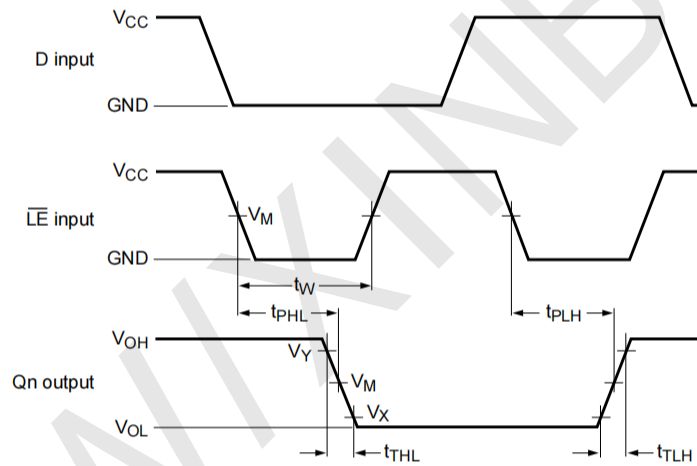


Figure 7. Enable input to output propagation delays and pulse width

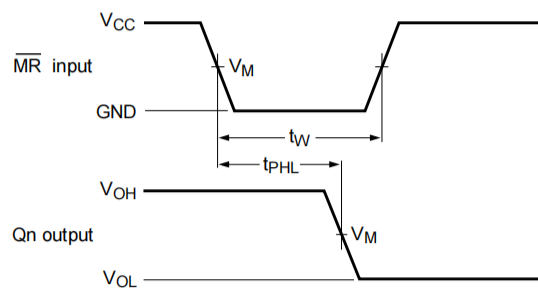


Figure 8. Master reset input to output propagation delay

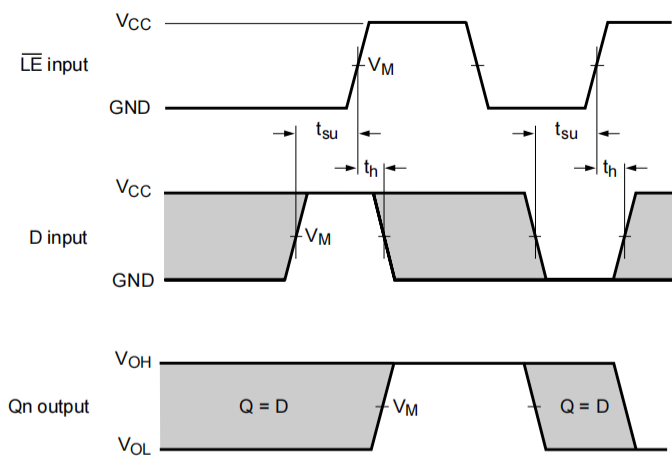


Figure 9. Data input to latch enable input set-up and hold times

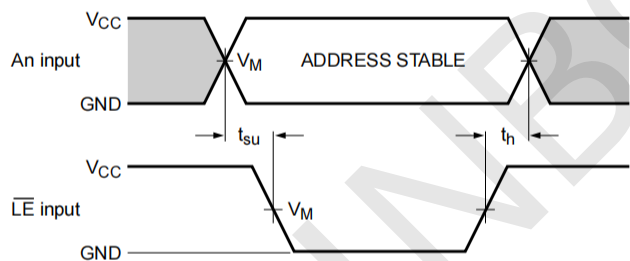


Figure 10. Address input to latch enable input set-up and hold times

Measurement Points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
SN74LS259	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$0.1 \times V_{CC}$	$0.9 \times V_{CC}$

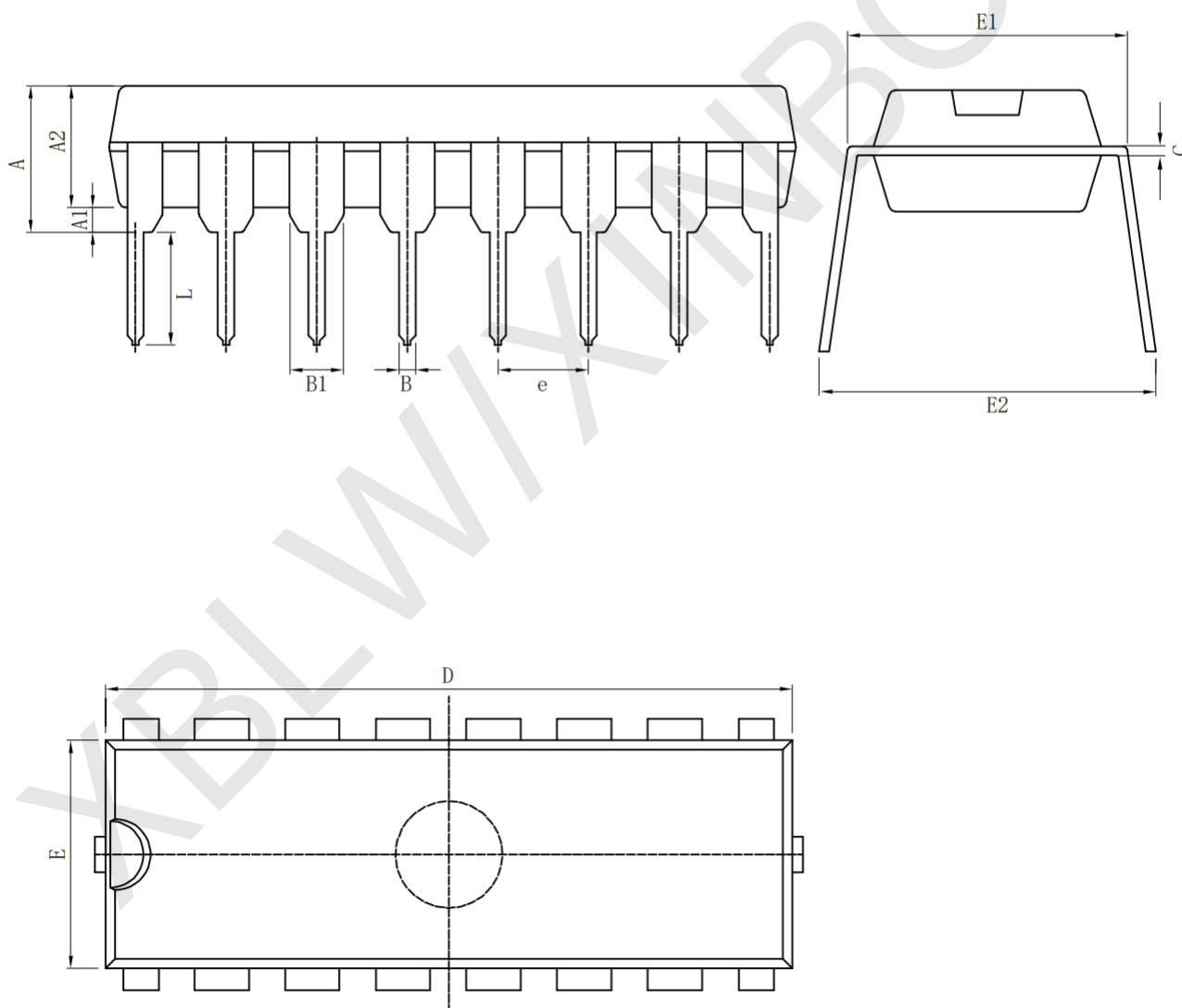
Test Data

Type	Input		Load		S1 position
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
SN74LS259	V_{CC}	6ns	15pF, 50pF	1kΩ	open

Package Information

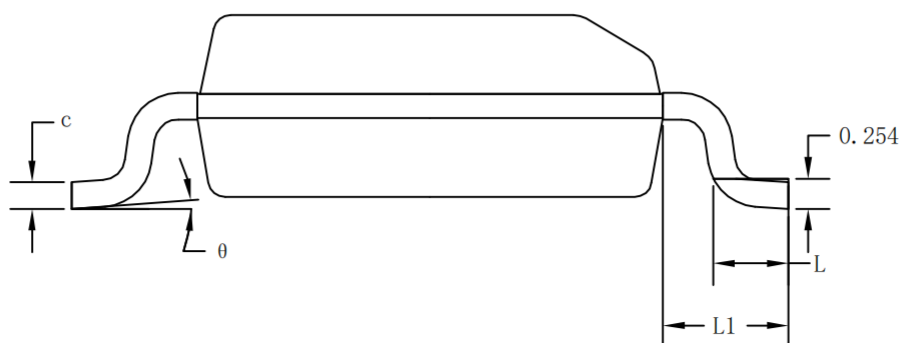
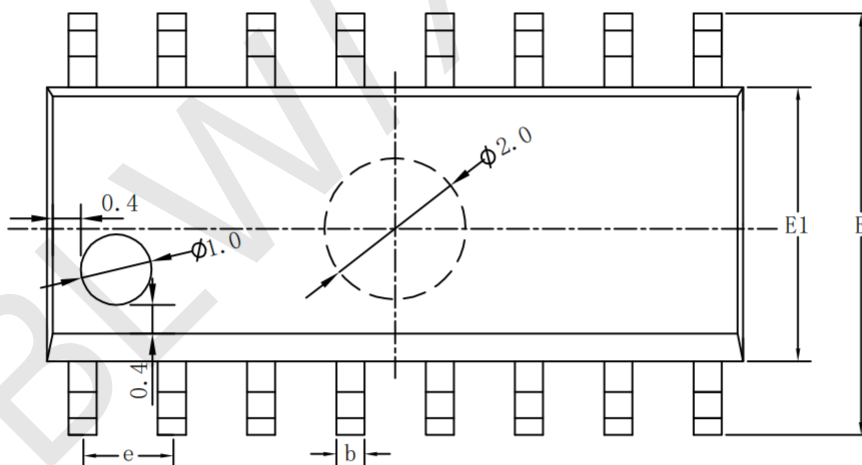
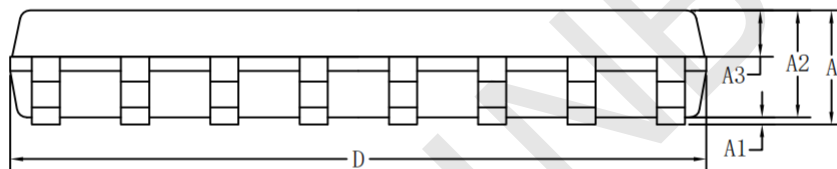
· DIP-16

Symbol \ Size	Dimensions In Millimeters		Symbol \ Size	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A	3.710	4.310	A	0.146	0.170
A1	0.510		A1	0.020	
A2	3.200	3.600	A2	0.126	0.142
B	0.380	0.570	B	0.015	0.022
B1	1.524 (BSC)		B1	0.060 (BSC)	
C	0.204	0.360	C	0.008	0.014
D	18.80	19.20	D	0.740	0.756
E	6.200	6.600	E	0.244	0.260
E1	7.320	7.920	E1	0.288	0.312
e	2.540 (BSC)		e	0.100 (BSC)	
L	3.000	3.600	L	0.118	0.142
E2	8.400	9.000	E2	0.331	0.354



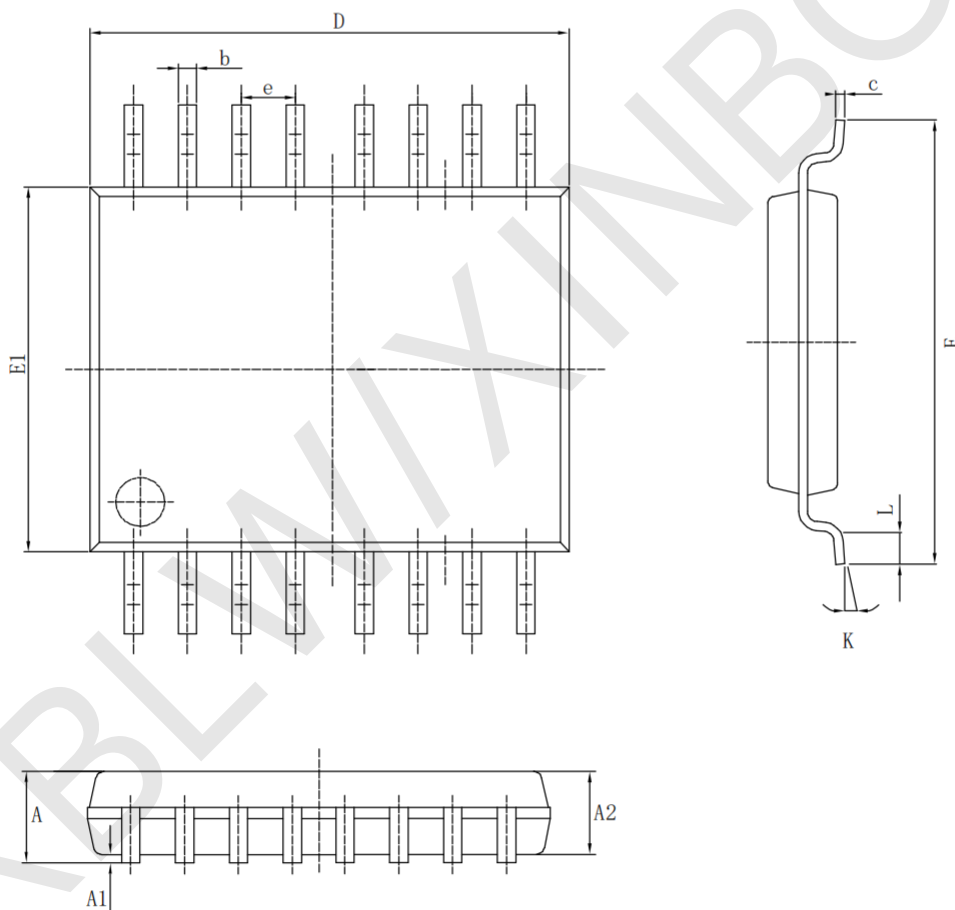
· SOP-16

Symbol \ Size	Dimensions In Millimeters			Symbol \ Size	Dimensions In Inches		
	Min (mm)	Nom (mm)	Max (mm)		Min (in)	Nom (in)	Max (in)
A	1.500	1.600	1.700	A	0.059	0.063	0.067
A1	0.100	0.150	0.250	A1	0.004	0.006	0.010
A2	1.400	1.450	1.500	A2	0.055	0.057	0.059
A3	0.600	0.650	0.700	A3	0.024	0.026	0.028
b	0.300	0.400	0.500	b	0.012	0.016	0.020
c	0.150	0.200	0.250	c	0.006	0.008	0.010
D	9.800	9.900	10.00	D	0.386	0.390	0.394
E	5.800	6.000	6.200	E	0.228	0.236	0.244
E1	3.850	3.900	3.950	E1	0.152	0.154	0.156
e	1.27 (BSC)			e	0.050 (BSC)		
L	0.500	0.600	0.700	L	0.020	0.024	0.028
L1	1.05 (BSC)			L1	0.041 (BSC)		
θ	0°	4°	8°	θ	0°	4°	8°



· TSSOP-16

Size Symbol	Dimensions In Millimeters		Size Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A		1.200	A		0.047
A1	0.050	0.150	A1	0.002	0.006
A2	0.800	1.050	A2	0.031	0.041
b	0.190	0.300	b	0.007	0.012
c	0.090	0.200	c	0.004	0.0089
D	4.900	5.100	D	0.193	0.201
E	6.200	6.600	E	0.244	0.260
E1	4.300	4.480	E1	0.169	0.176
e	0.65 (BSC)		e	0.0256 (BSC)	
K	0°	8°	K	0°	8°
L	0.450	0.750	L	0.018	0.030



Statement

- XBLW reserves the right to modify the product manual without prior notice! Before placing an order, customers need to confirm whether the obtained information is the latest version and verify the completeness of the relevant information.
- Any semi-guide product is subject to failure or malfunction under specified conditions. It is the buyer's responsibility to comply with safety standards when using XBLW products for system design and whole machine manufacturing. And take the appropriate safety measures to avoid the potential in the risk of loss of personal injury or loss of property situation!
- XBLW product has not been licensed for life support, military and aerospace applications, and therefore XBLW is not responsible for any consequences arising from its use in these areas.
- If any or all XBLW products (including technical data, services) described or contained in this document are subject to any applicable local export control laws and regulations, they may not be exported without an export license from the relevant authorities in accordance with such laws.
- The specifications of any and all XBLW products described or contained in this document specify the performance, characteristics, and functionality of said products in their standalone state, but do not guarantee the performance, characteristics, and functionality of said products installed in Customer's products or equipment. In order to verify symptoms and conditions that cannot be evaluated in a standalone device, the Customer should ultimately evaluate and test the device installed in the Customer's product device.
- XBLW documentation is only allowed to be copied without any alteration of the content and with the relevant authorization. XBLW assumes no responsibility or liability for altered documents.
- XBLW is committed to becoming the preferred semiconductor brand for customers, and XBLW will strive to provide customers with better performance and better quality products.