

SE30P50B

P-Channel Enhancement-Mode MOSFET

Revision: A

General Description

Thigh Density Cell Design For Ultra Low On-Resistance Fully Characterized Avalanche Voltage and Current Improved Shoot-Through FOM

- Simple Drive Requirement
- Small Package Outline
- Surface Mount Device

Features

For a single MOSFET

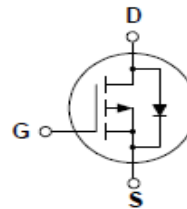
- $V_{DS} = -30V$
- $R_{DS(ON)} = 5.8m\Omega @ V_{GS}=-10$

Pin configurations

See Diagram below



TO-252-2L



Absolute Maximum Ratings

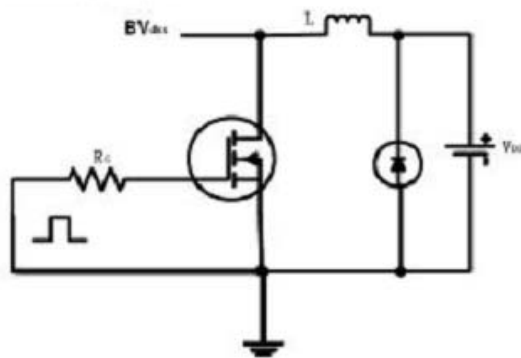
Parameter		Symbol	Rating	Units
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	± 20	V
Drain Current	Continuous	I_D	-50	A
	Pulsed		-120	
Total Power Dissipation	@TA=25°C	P_D	90	W
Operating Junction Temperature Range		T_J	-55 to 150	°C

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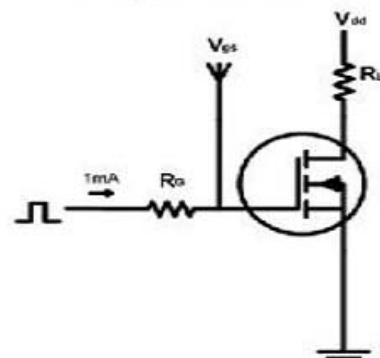
Electrical Characteristics (TJ=25°C unless otherwise noted)						
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS (Note 2)						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0 V	-30			V
I _{DSS}	Drain to Source Leakage Current	V _{DS} = -30V, V _{GS} =0V			1	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =20 V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D =250μA	-0.4	-1.5	-2.2	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =-10V, I _D =-20A	-	5.8	7	mΩ
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz		7032		pF
C _{oss}	Output Capacitance			898		pF
C _{rss}	Reverse Transfer Capacitance			743		pF
SWITCHING PARAMETERS						
Q _g	Total Gate Charge ²	V _{GS} =10V, V _{DS} =15V, I _D =30A		80		nC
Q _{gs}	Gate Source Charge			19		nC
Q _{gd}	Gate Drain Charge			38		nC
t _{d(on)}	Turn-On Delay Time	V _{GS} =10V, V _{DS} =15V, R _{GEN} =1Ω I _D =1A		20		ns
t _{d(off)}	Turn-Off Delay Time			80		ns
t _{d(r)}	Turn-On Rise Time			36		ns
t _{d(f)}	Turn-Off Fall Time			33		ns
Thermal Resistance						
Symbol	Parameter	Typ		Max	Units	
R _{θJC}	Junction to Case	-		2	°C/W	
R _{θJA}	Junction to Ambient (t ≤ 10s)	-		50	°C/W	

Test Circuits and Waveform

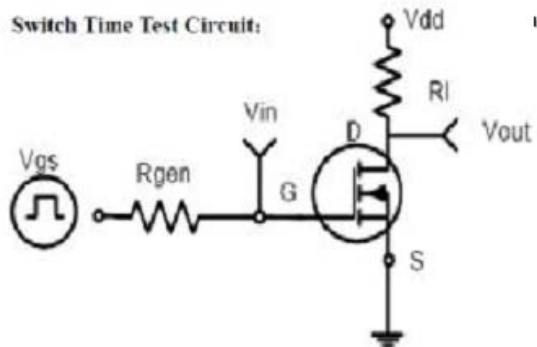
EAS test circuits:



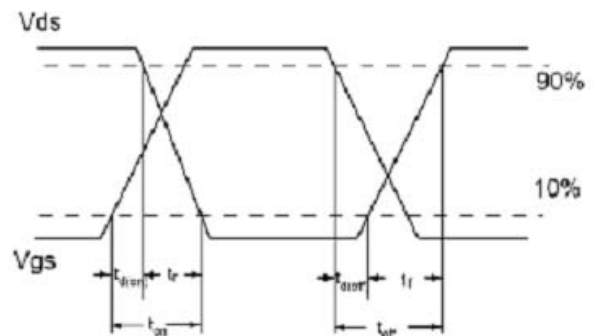
Gate charge test circuit:



Switch Time Test Circuit:



Waveforms:



Typical Characteristics

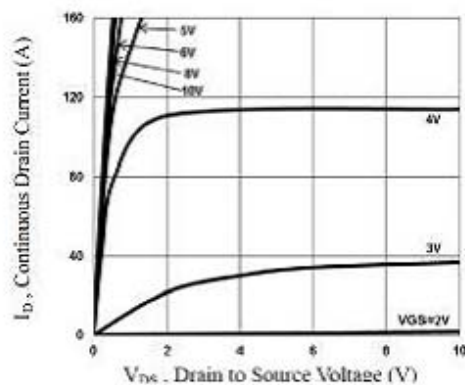


Figure 1: Typical Output Characteristics

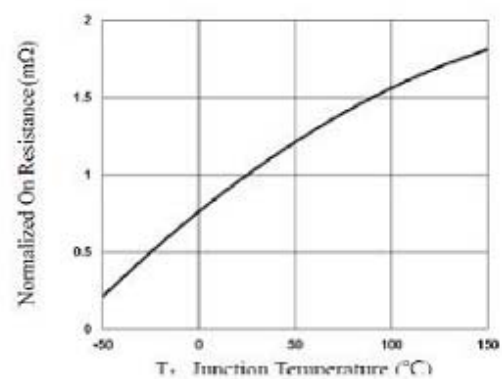


Figure 2: Normalized RDSON vs. TJ

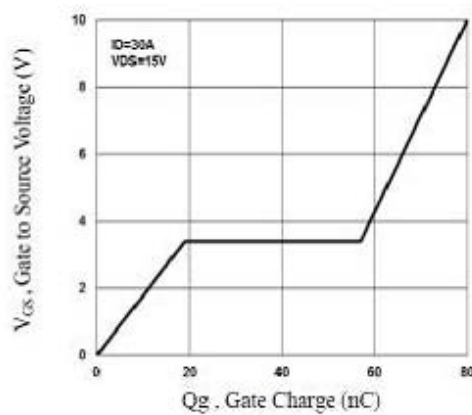


Figure 3: Gate-Charge Characteristics

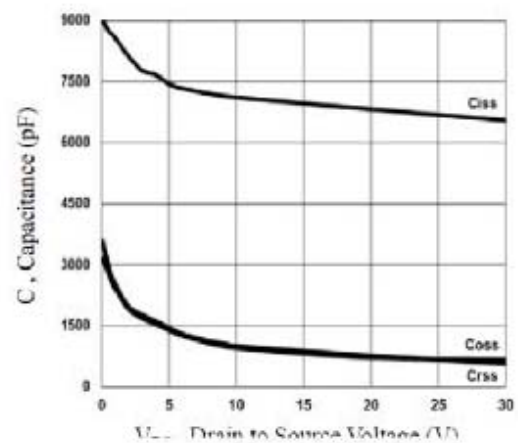


Figure 4: Capacitance Characteristics

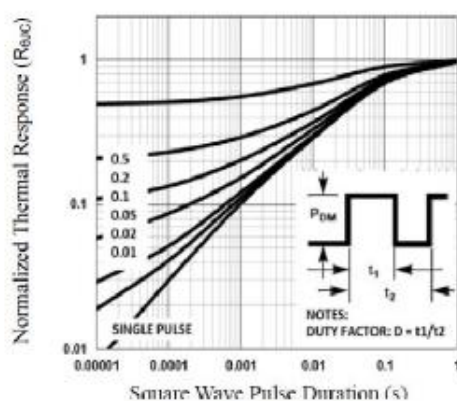


Figure 5: Normalized Thermal transient Impedance Curve

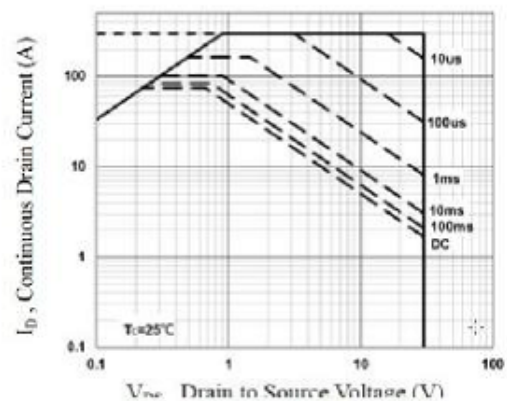
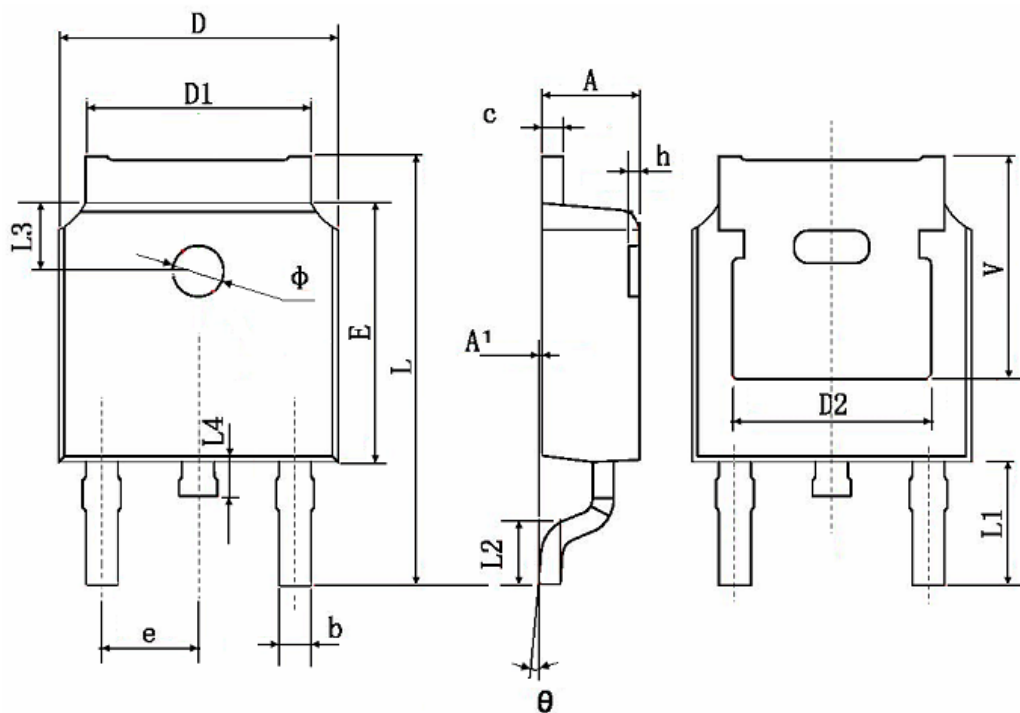


Figure 6: Maximum Safe Operation Area

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Package Outline Dimension

TO-252



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	0.483 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	

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