

## SI2337DS-T1-GE3-VB Datasheet

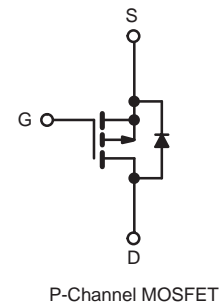
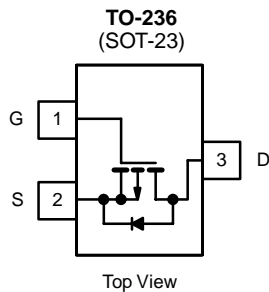
### P-Channel 60-V (D-S) MOSFET

#### PRODUCT SUMMARY

$V_{DS}$ (V)	- 60	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = -10\text{ V}$	0.05
$Q_g$ (Max.) (nC)	12	
$Q_{gs}$ (nC)	3.8	
$Q_{gd}$ (nC)	5.1	
Configuration	Single	

#### FEATURES

- Isolated Package
- High Voltage Isolation = 2.5 kV<sub>RMS</sub> (t = 60 s; f = 60 Hz)
- Sink to Lead Creepage Distance = 4.8 mm
- P-Channel
- 175 °C Operating Temperature
- Dynamic dV/dt Rating
- Low Thermal Resistance
- Lead (Pb)-free Available


**RoHS\***  
 COMPLIANT


#### ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ °C}$ , unless otherwise noted

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	- 60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current	$V_{GS} \text{ at } -10\text{ V}$	$T_C = 25\text{ °C}$	A
		$T_C = 100\text{ °C}$	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	- 21	
Linear Derating Factor		0.18	W/°C
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	120	mJ
Repetitive Avalanche Current <sup>a</sup>	$I_{AR}$	- 5.2	A
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	2.7	mJ
Maximum Power Dissipation	$P_D$	$T_C = 25\text{ °C}$	W
Peak Diode Recovery dV/dt <sup>c</sup>	dV/dt	- 4.5	V/ns
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 175	°C
Soldering Recommendations (Peak Temperature)	for 10 s	300 <sup>d</sup>	
Mounting Torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m


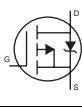
#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = -25\text{ V}$ , starting  $T_J = 25\text{ °C}$ ,  $L = 5.0\text{ mH}$ ,  $R_G = 25\text{ }\Omega$ ,  $I_{AS} = -5.3\text{ A}$  (see fig. 12).
- $I_{SD} \leq -6.7\text{ A}$ ,  $dI/dt \leq 90\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 175\text{ °C}$ .
- 1.6 mm from case.

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	65	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	5.5	

**SPECIFICATIONS**  $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = - 250 μA		- 60	-	-	V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = - 1 mA		-	- 0.060	-	V/°C
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = - 250 μA		- 1.0	-	- 2.5	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = - 60 V, V <sub>GS</sub> = 0 V		-	-	- 100	μA
		V <sub>DS</sub> = - 48 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 150 °C		-	-	- 500	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 10 V	I <sub>D</sub> = - 3.2 A <sup>b</sup>	-	0.05	-	Ω
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = - 25 V, I <sub>D</sub> = - 3.2 A <sup>b</sup>		1.6	-	-	S
Dynamic							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = - 25 V, f = 1.0 MHz, see fig. 5		-	270	-	pF
Output Capacitance	C <sub>oss</sub>			-	170	-	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	31	-	
Drain to Sink Capacitance	C	f = 1.0 MHz		-	12	-	
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = - 10 V	I <sub>D</sub> = - 4.7 A, V <sub>DS</sub> = - 48 V, see fig. 6 and 13 <sup>b</sup>	-	-	12	nC
Gate-Source Charge	Q <sub>gs</sub>			-	-	3.8	
Gate-Drain Charge	Q <sub>gd</sub>			-	-	5.1	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = - 30 V, I <sub>D</sub> = - 4.7 A, R <sub>G</sub> = 24 Ω, R <sub>D</sub> = 4.0 Ω, see fig. 10 <sup>b</sup>		-	11	-	ns
Rise Time	t <sub>r</sub>			-	63	-	
Turn-Off Delay Time	t <sub>d(off)</sub>			-	9.6	-	
Fall Time	t <sub>f</sub>			-	31	-	
Internal Drain Inductance	L <sub>D</sub>	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal Source Inductance	L <sub>S</sub>			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	- 5.2	A
Pulsed Diode Forward Current <sup>a</sup>	I <sub>SM</sub>			-	-	- 21	
Body Diode Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = - 5.2 A, V <sub>GS</sub> = 0 V <sup>b</sup>		-	-	- 5.5	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = - 4.7 A, dI/dt = 100 A/μs <sup>b</sup>		-	80	160	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			-	0.096	0.19	μC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> and L <sub>D</sub> )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).  
 b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

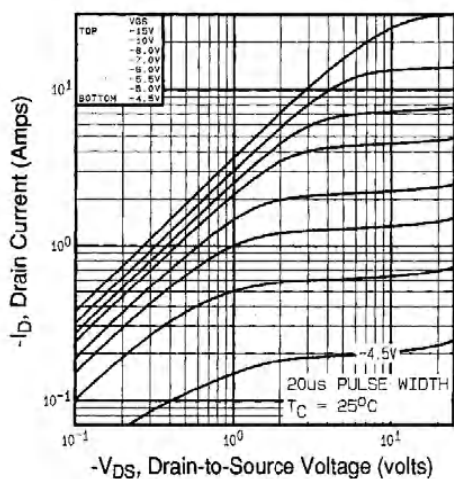
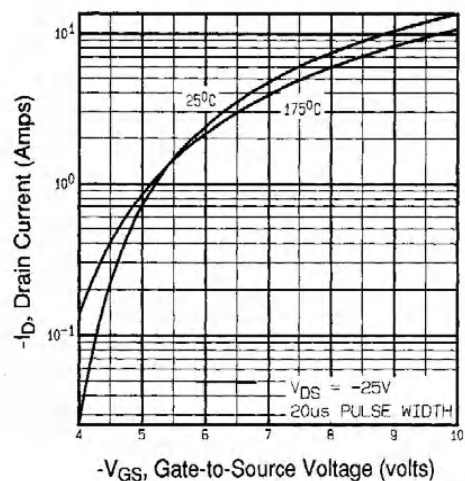
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted
Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ }^{\circ}\text{C}$ 

Fig. 3 - Typical Transfer Characteristics

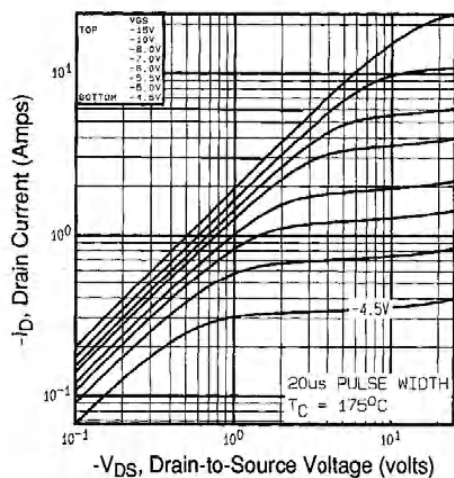
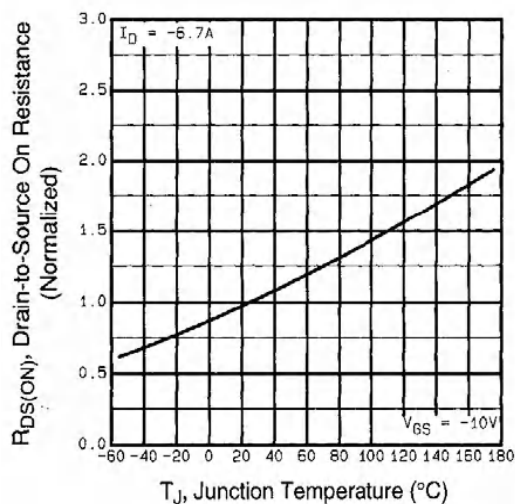
Fig. 2 - Typical Output Characteristics,  $T_C = 175\text{ }^{\circ}\text{C}$ 

Fig. 4 - Normalized On-Resistance vs. Temperature

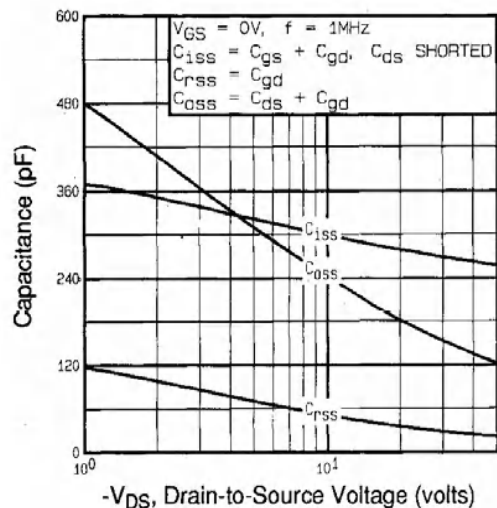


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

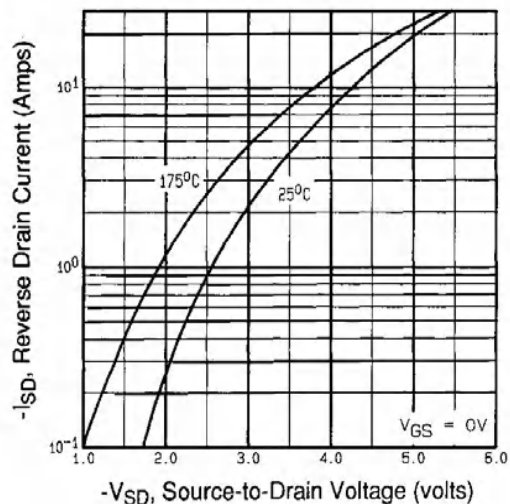


Fig. 7 - Typical Source-Drain Diode Forward Voltage

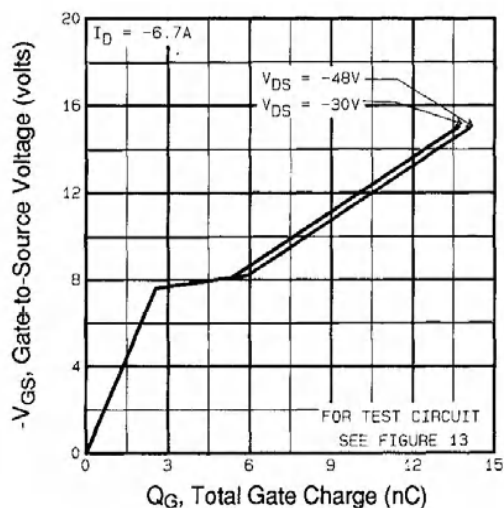


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

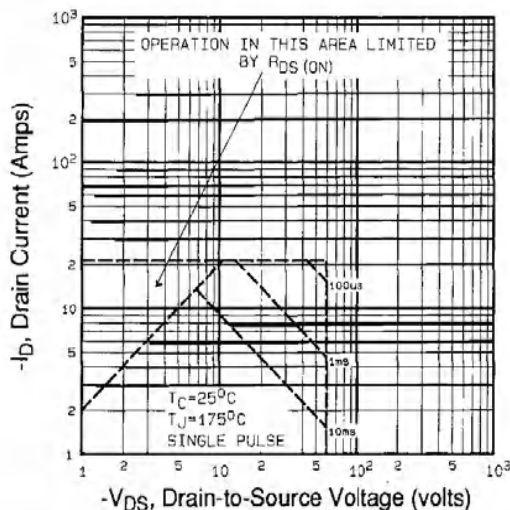


Fig. 8 - Maximum Safe Operating Area

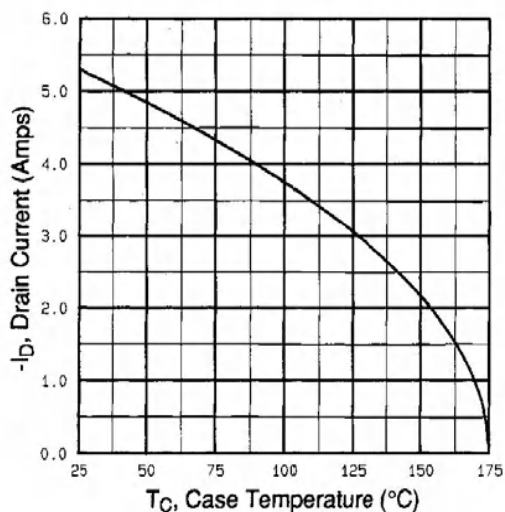


Fig. 9 - Maximum Drain Current vs. Case Temperature

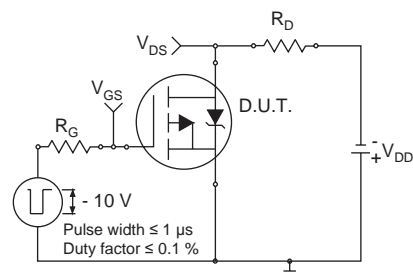


Fig. 10a - Switching Time Test Circuit

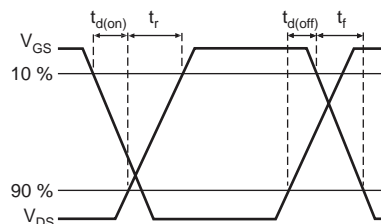


Fig. 10b - Switching Time Waveforms

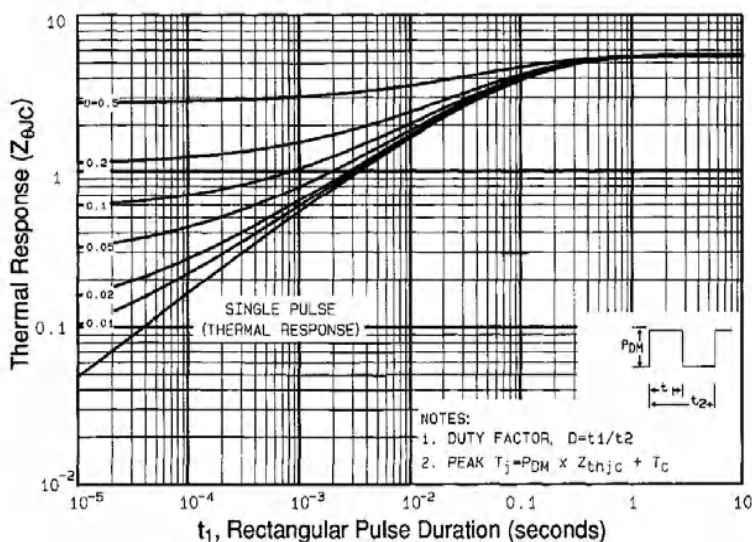


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

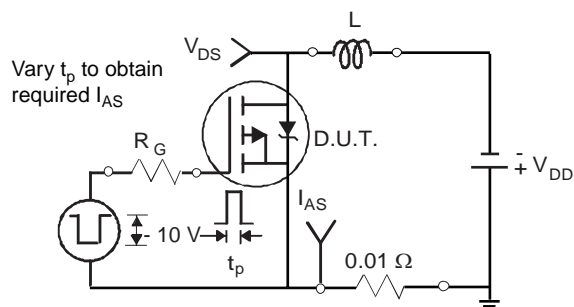


Fig. 12a - Unclamped Inductive Test Circuit

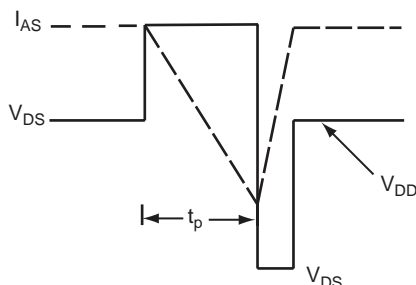


Fig. 12b - Unclamped Inductive Waveforms

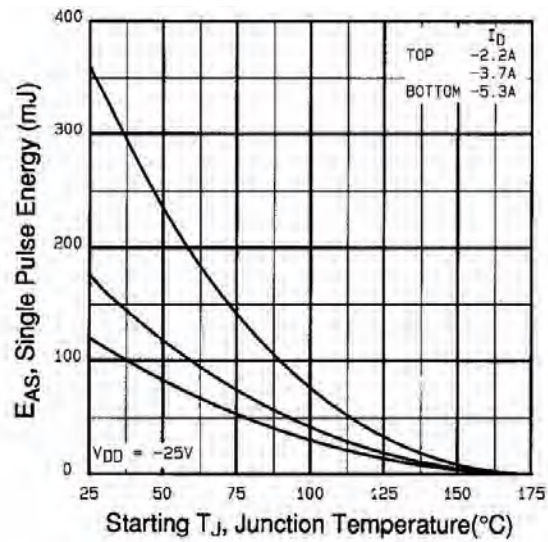


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

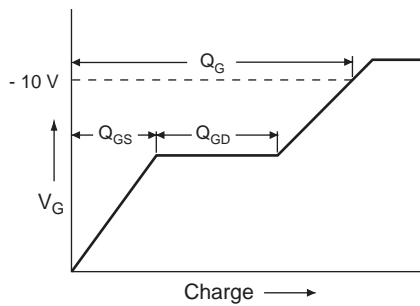


Fig. 13a - Basic Gate Charge Waveform

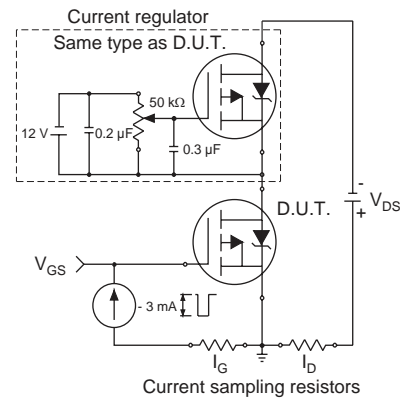
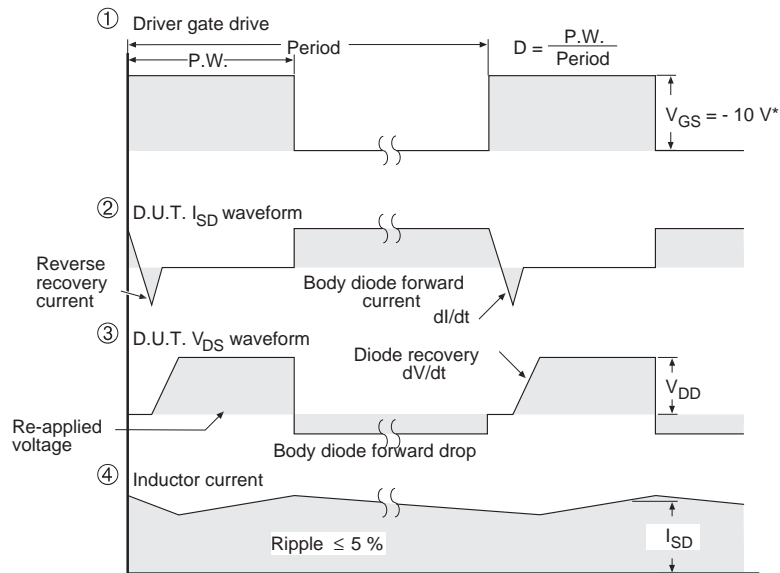
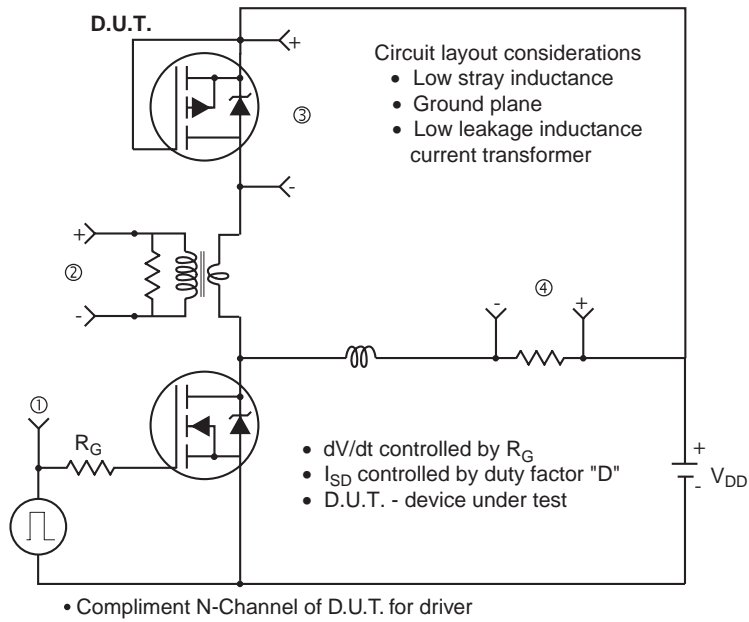


Fig. 13b - Gate Charge Test Circuit

### Peak Diode Recovery dV/dt Test Circuit

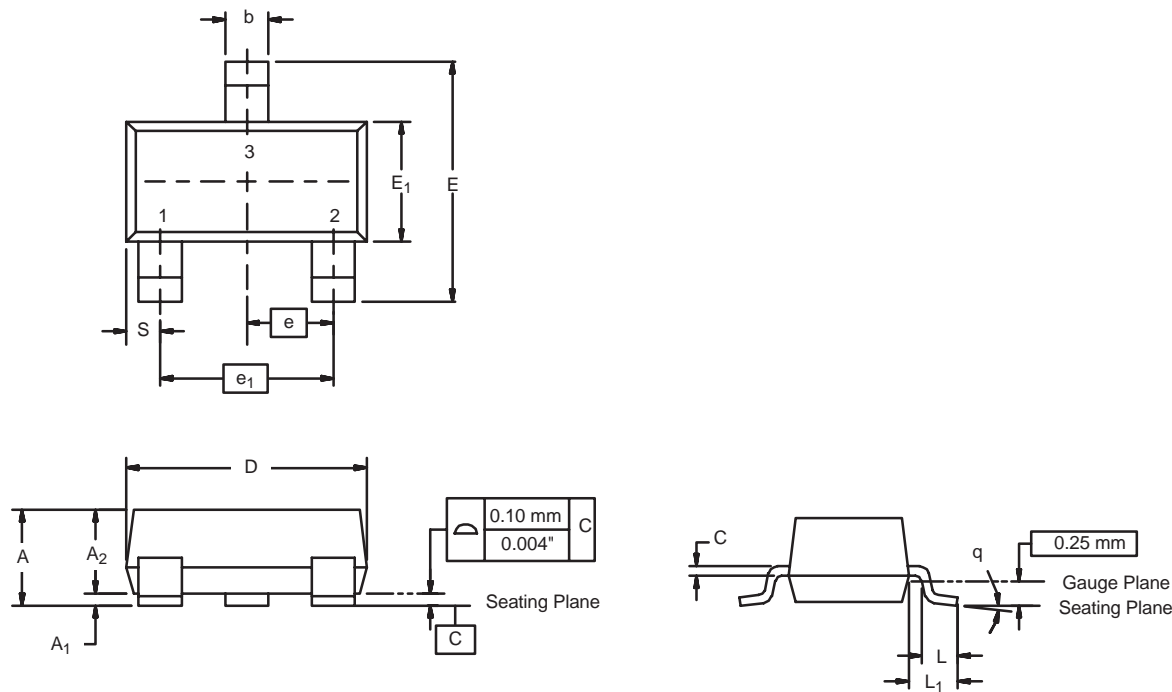


\*  $V_{GS} = -5 V$  for logic level and  $-3 V$  drive devices

**Fig. 14 - For P-Channel**



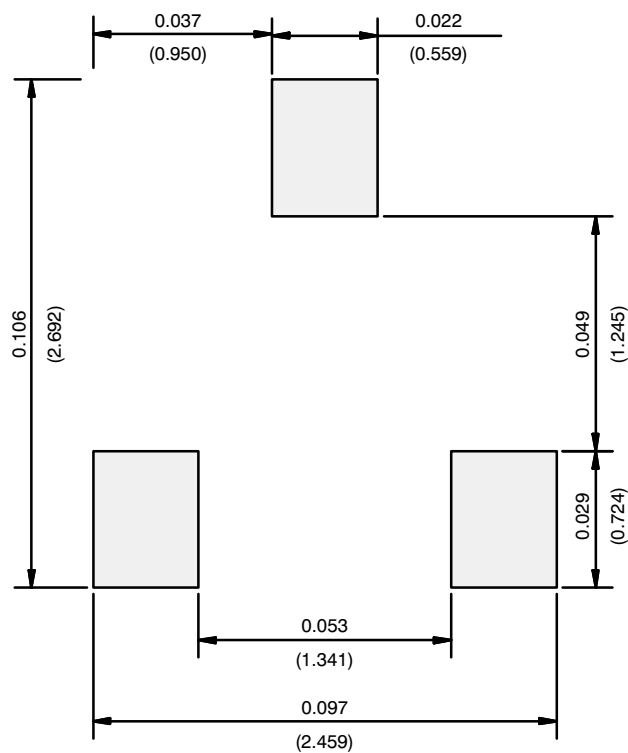
**SOT-23 (TO-236): 3-LEAD**



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	0.89	1.12	0.035	0.044
A <sub>1</sub>	0.01	0.10	0.0004	0.004
A <sub>2</sub>	0.88	1.02	0.0346	0.040
b	0.35	0.50	0.014	0.020
c	0.085	0.18	0.003	0.007
D	2.80	3.04	0.110	0.120
E	2.10	2.64	0.083	0.104
E <sub>1</sub>	1.20	1.40	0.047	0.055
e	0.95 BSC		0.0374 Ref	
e <sub>1</sub>	1.90 BSC		0.0748 Ref	
L	0.40	0.60	0.016	0.024
L <sub>1</sub>	0.64 Ref		0.025 Ref	
S	0.50 Ref		0.020 Ref	
q	3°	8°	3°	8°
ECN: S-03946-Rev. K, 09-Jul-01 DWG: 5479				



## RECOMMENDED MINIMUM PADS FOR SOT-23



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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