

## General Description

The WSD40L66DN56 uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

The WSD40L66DN56 meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

## Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent  $CdV/dt$  effect decline
- 100% EAS Guaranteed
- Green Device Available

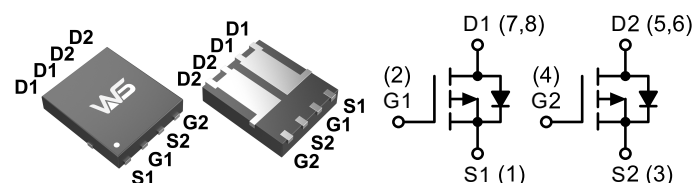
## Product Summary

$BV_{DSS}$	$R_{DS(ON)}$	$I_D$
-40V	9.8m $\Omega$	-66A

## Applications

- Battery protection
- Load switch
- Uninterruptible Power Supply(UPS)

## DFN5X6-8L-EP Pin Configuration



## Absolute Maximum Ratings ( $T_C=25^{\circ}\text{C}$ , Unless Otherwise Noted)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	-40	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_C=25^{\circ}\text{C}$	Continuous Drain Current, $V_{GS} @ -10\text{V}^1$	-66	A
$I_D@T_C=100^{\circ}\text{C}$	Continuous Drain Current, $V_{GS} @ -10\text{V}^1$	-42	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	-105	A
$E_{AS}$	Single Pulse Avalanche Energy <sup>3</sup>	146	mJ
$P_D@T_C=25^{\circ}\text{C}$	Power Dissipation <sup>4</sup>	1.5	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^{\circ}\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^{\circ}\text{C}$

## Thermal Data

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient <sup>1</sup>	---	25	$^{\circ}\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case <sup>1</sup>	---	2.4	$^{\circ}\text{C/W}$

**Electrical Characteristics** ( $T_J=25^{\circ}\text{C}$ , Unless Otherwise Noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V$ , $I_D=-250\mu A$	-40	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	$BV_{DSS}$ Temperature Coefficient	Reference to $25^{\circ}\text{C}$ , $I_D=-1\text{mA}$	---	-0023	---	$V/^{\circ}\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=-10V$ , $I_D=-30A$	---	9.8	13	m $\Omega$
		$V_{GS}=-4.5V$ , $I_D=-20A$	---	15	20	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$ , $I_D=-250\mu A$	-1.0	-1.6	-2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	4.74	---	mV/ $^{\circ}\text{C}$
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=-32V$ , $V_{GS}=0V$ , $T_J=25^{\circ}\text{C}$	---	---	1.0	$\mu A$
		$V_{DS}=-32V$ , $V_{GS}=0V$ , $T_J=55^{\circ}\text{C}$	---	---	5.0	
$I_{GSS}$	Gate-Source Leakage Current	$V_{DS}=0V$ , $V_{GS}=\pm 20V$	---	---	$\pm 100$	nA
$g_{fs}$	Forward Transconductance	$V_{DS}=-5V$ , $I_D=-18A$	---	24	---	S
$R_g$	Gate Resistance	$V_{DS}=0V$ , $V_{GS}=0V$ , $f = 1.0\text{MHz}$	---	7	14	$\Omega$
$Q_g$	Total Gate Charge (-4.5V)	$V_{DS}=-20V$ , $V_{GS}=-4.5V$ , $I_D=-12A$	---	27.9	---	nC
$Q_{gs}$	Gate-Source Charge		---	7.7	---	
$Q_{gd}$	Gate-Drain Charge		---	7.5	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=-15V$ , $V_{GS}=-10V$ , $R_G=3.3\Omega$ , $I_D=-1A$	---	40	---	ns
$T_r$	Rise Time		---	35.2	---	
$T_{d(off)}$	Turn-Off Delay Time		---	100	---	
$T_f$	Fall Time		---	9.6	---	
$C_{iss}$	Input Capacitance	$V_{DS}=-15V$ , $V_{GS}=0V$ , $f = 1.0\text{MHz}$	---	3500	---	pF
$C_{oss}$	Output Capacitance		---	323	---	
$C_{rss}$	Reverse Transfer Capacitance		---	222	---	

**Diode Characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$I_S$	Continuous Source Current <sup>1,5</sup>	$V_G=V_D=0V$ , Force Current	---	---	-52	A
$I_{SM}$	Pulsed Source Current <sup>2,5</sup>		---	---	-105	
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0V$ , $I_S=-1A$ , $T_J=25^{\circ}\text{C}$	---	---	-1.0	V

Note:

1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 20Z copper.
2. The data tested by pulsed, pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$
3. The power dissipation is limited by  $150^{\circ}\text{C}$  junction temperature
4. The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications, should be limited by total power dissipation.

### Typical Characteristics

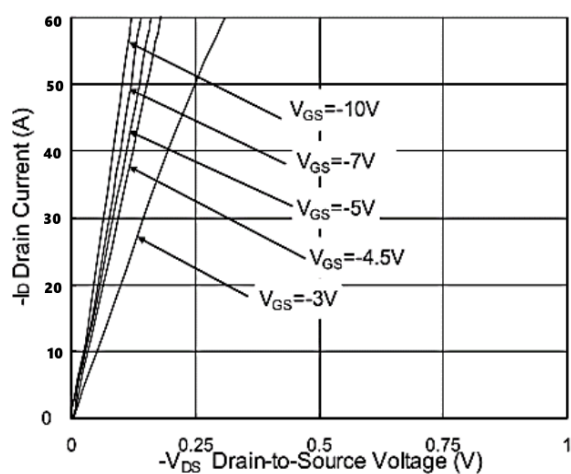


Fig.1 Typical Output Characteristics

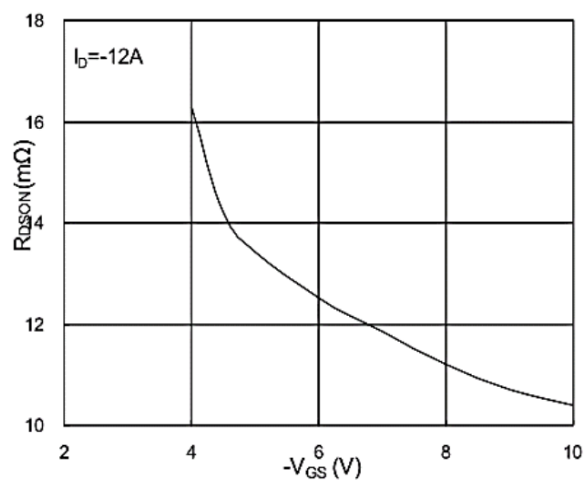


Fig.2 On-Resistance v.s Gate-Source

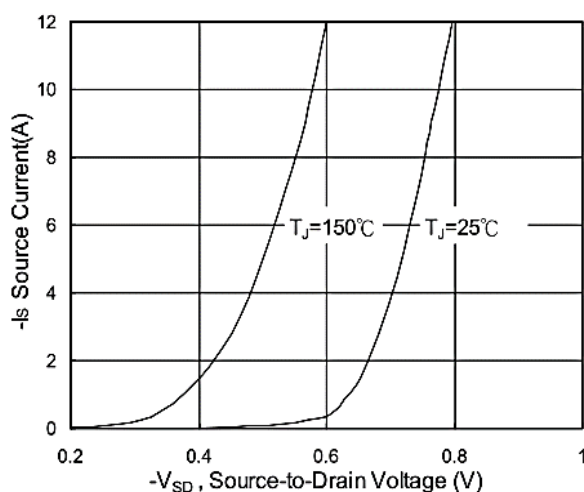


Fig.3 Forward Characteristics Of Reverse

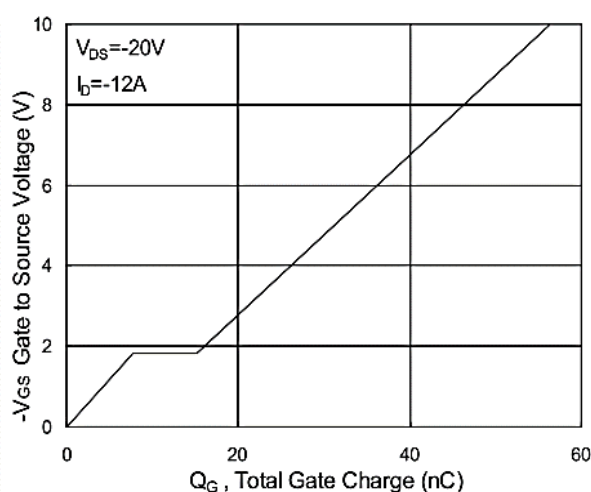


Fig.4 Gate-Charge Characteristics

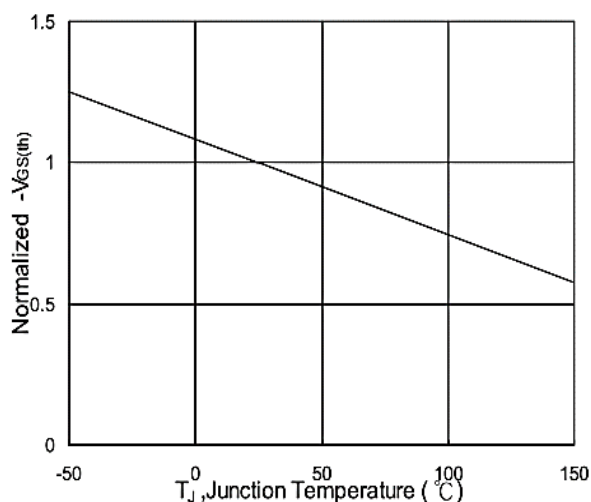


Fig.5 Normalized  $V_{GS(th)}$  v.s  $T_J$

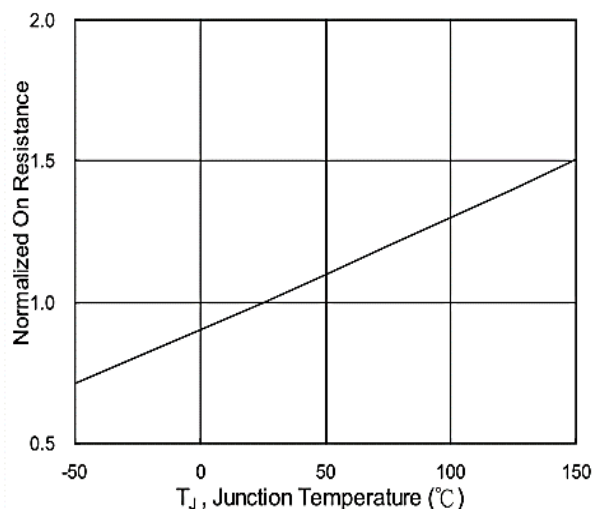


Fig.6 Normalized  $R_{DS(on)}$  v.s  $T_J$

Typical Characteristics (Cont.)

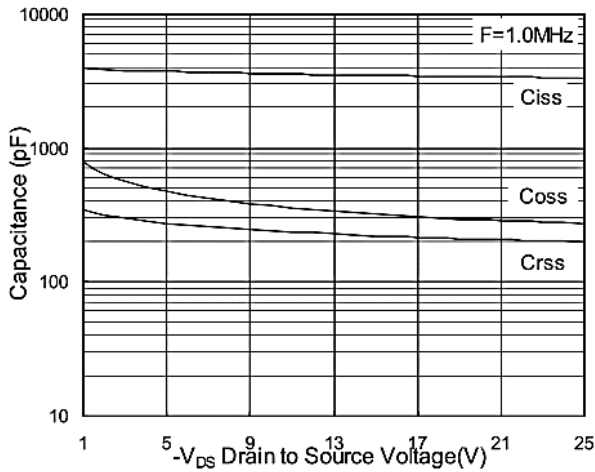


Fig.7 Capacitance

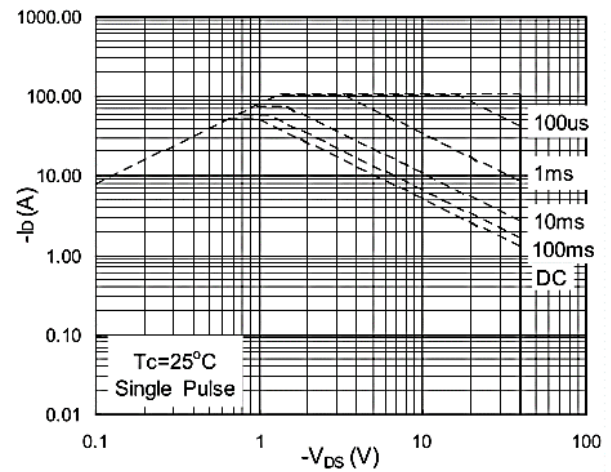


Fig.8 Safe Operating Area

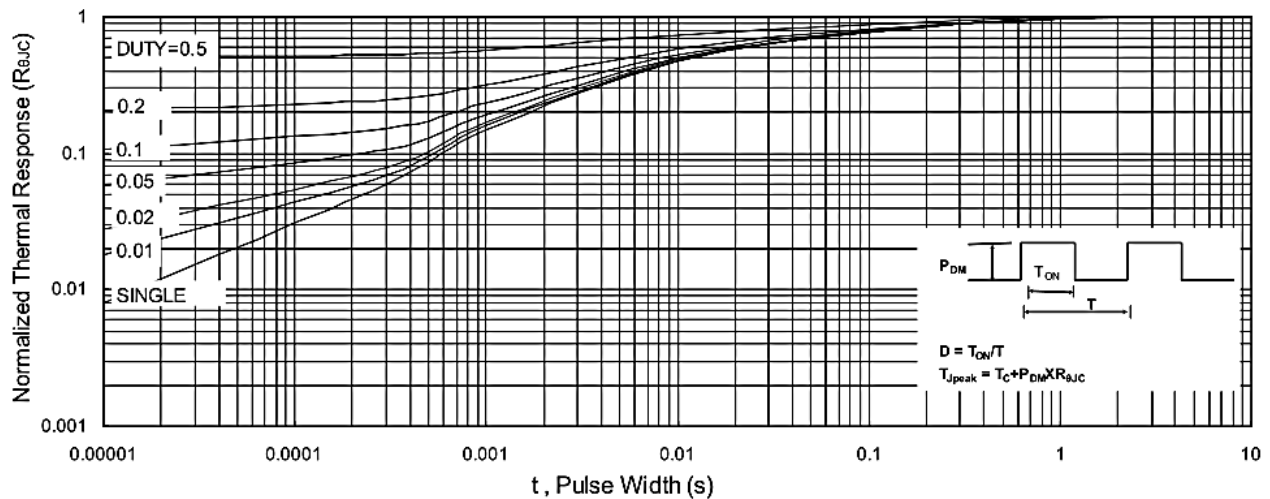


Fig.9 Normalized Maximum Transient Thermal Impedance

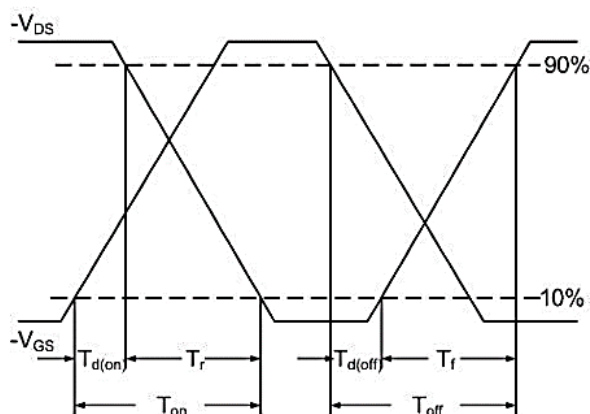


Fig.10 Switching Time Waveform

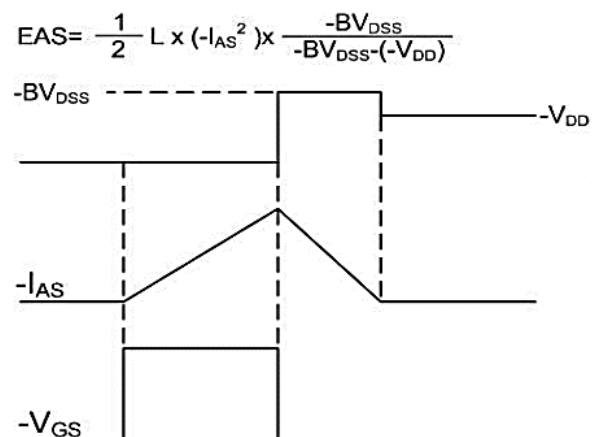
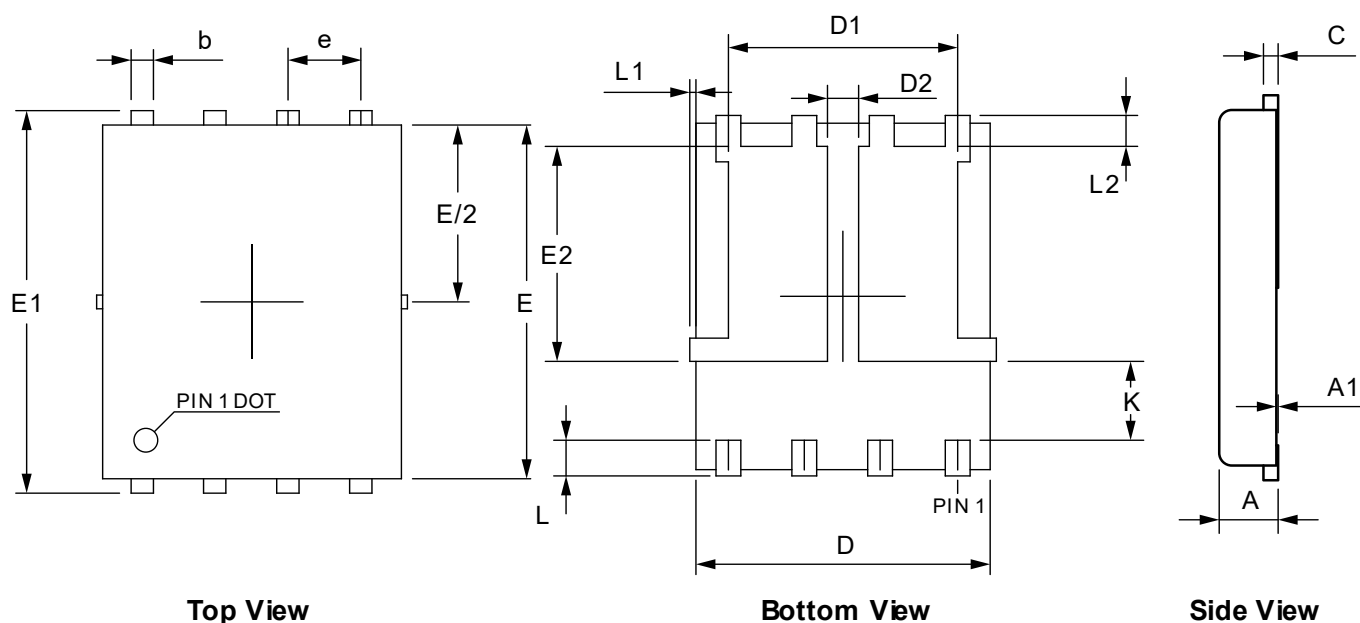


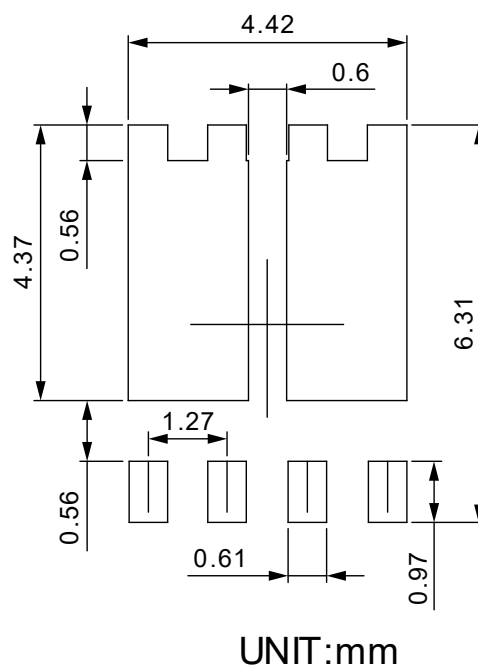
Fig.11 Unclamped Inductive Waveform

## Packaging information



SYMBOL	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.900	1.200	0.035	0.047
A1	0.000	0.050	0.000	0.002
b	0.300	0.500	0.012	0.020
c	0.150	0.300	0.006	0.012
D	4.800	5.000	0.189	0.197
D1	3.550	4.550	0.140	0.179
D2	0.500	0.910	0.020	0.036
E	5.650	5.850	0.222	0.230
E1	5.900	6.200	0.232	0.244
E2	3.200	3.780	0.126	0.149
e	1.27 BSC		0.050 BSC	
K	1.100	-	0.043	-
L	0.500	0.800	0.020	0.031
L1	0.000	0.150	0.000	0.006
L2	0.325	0.610	0.013	0.024

## RECOMMENDED LAND PATTERN



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