

3A Ultra-Low Dropout Voltage Regulator

The HT9059A is a high-performance positive voltage regulator designed for applications requiring very low input voltage and very low dropout voltage at up to 3A. It operates with a V_{IN} as low as 1V and a 3V V_{DD} , with a programmable output voltage as low as 0.8V. The HT9059A features ultra-low dropout, making it ideal for applications where V_{OUT} is very close to V_{IN} . Additionally, the HT9059A has an enable pin to further reduce power dissipation during shutdown. The HT9059A provides excellent regulation over variations in line, load, and temperature. The HT9059A also provides a power-good signal to indicate if the voltage level of V_O reaches 90% of its rated value. The recommended junction temperature range is -40°C to 125°C , and the ambient temperature range is -40°C to 85°C .

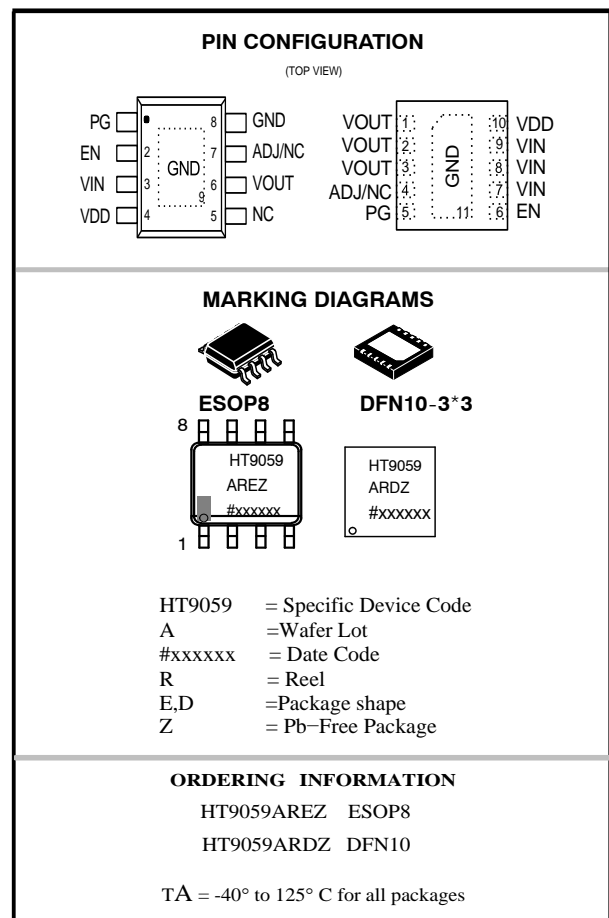
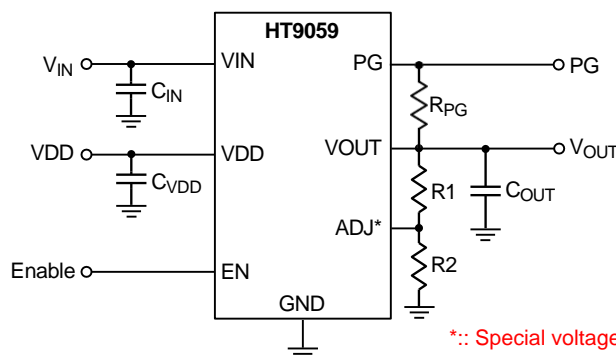
2 Features

- Output Current up to 3A
- High Accuracy ADJ Voltage (1.5%)
- Dropout Voltage: 350mV @ 3A (Typical)
- V_{OUT} Power-Good Signal
- V_{OUT} Pull Low Resistance when Disabled
- Current-Limit Protection
- Over-Temperature Protection

3 Applications

- Notebook PC Applications
- Motherboard Applications

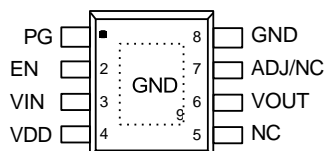
4 Simplified Application Circuit



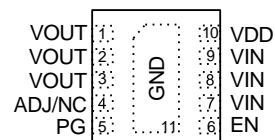
*:: Special voltage is accepted.

6 Pin Configuration

(TOP VIEW)



SOP-8 (Exposed Pad)



WDFN-10L 3x3

7 Functional Pin Description

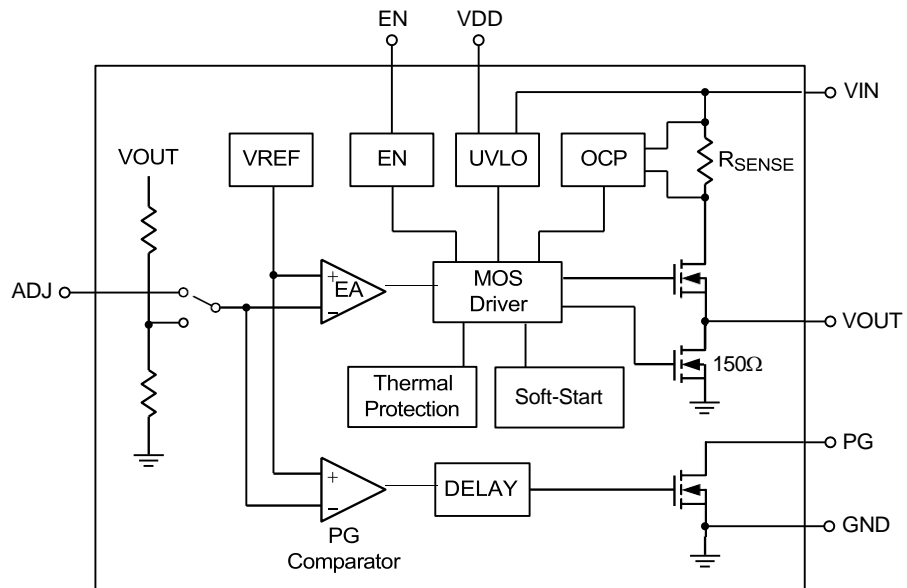
7.1 SOP-8 Package

Pin No.		Pin Name	Pin Function
Adjustable Output Voltage	Fixed Output Voltage		
1	1	PG	Power-good indicator. This open-drain output pin is pulled high when the VOUT or FB voltage is within the target range. It is pulled to ground under protection conditions, EN shutdown, or during the soft-start period.
2	2	EN	Enable control input. A logic-high enables the converter, while a logic-low forces the device into shutdown mode. Connect this pin to the VIN pin to conserve the system's power rail, or connect this pin to an external power rail for power sequence control. It is recommended to apply the enable voltage after the VIN pin voltage is ready for correct soft-start function. Do not leave this pin floating.
3	3	VIN	Supply voltage input. The input voltage range is from 1V to 5.5V. A suitable input capacitor should be placed close to this pin to minimize voltage spikes and noise, ensuring a stable input voltage.
4	4	VDD	Supply voltage of the control circuit. This pin provides the necessary power for the internal control logic and analog circuitry. It is important to ensure that the VDD voltage is stable and within the specified range to guarantee proper operation of the device.
5	5, 7	NC	No internal connection. Connect this pin to the GND plane of the top layer to extend the GND copper area to enhance the thermal performance.
6	6	VOUT	LDO output pin. Connect a ceramic capacitor with a capacitance of at least 10μF as close as possible from this pin to GND to minimize the output impedance.
7	--	ADJ	Feedback voltage input. This pin is used to set the output voltage via an external resistive voltage divider. The feedback reference voltage is 0.8V (typical). Place the resistive voltage divider as close to the FB pin as possible. Do not leave this pin floating.
8, 9 (Exposed Pad)	8, 9 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

7.2 WDFN-10L 3x3 Package

Pin No.		Pin Name	Pin Function
Adjustable Output Voltage	Fixed Output Voltage		
1, 2, 3	1, 2, 3	VOUT	LDO output pin. Connect a ceramic capacitor with a capacitance of at least 10 μ F as close as possible from this pin to GND to minimize the output impedance.
--	4	NC	No internal connection. Connect this pin to the GND plane of the top layer to extend the GND copper area to enhance the thermal performance.
4	--	ADJ	Feedback voltage input. This pin is used to set the output voltage via an external resistive voltage divider. The feedback reference voltage is 0.8V (typical). Place the resistive voltage divider as close to the FB pin as possible. Do not leave this pin floating.
5	5	PG	Power-good indicator. This open-drain output pin is pulled high when the VOUT or FB voltage is within the target range. It is pulled to ground under protection conditions, EN shutdown, or during soft-start period.
6	6	EN	Enable control input. A logic-high enables the converter, while a logic-low forces the device into shutdown mode. Connect this pin to the VIN pin to conserve the system's power rail and connect this pin to the external power rail for power sequence control. It is recommended to apply the enable voltage after the VIN pin voltage is ready for correct soft-start function. Do not leave this pin floating.
7, 8, 9	7, 8, 9	VIN	Supply voltage input. The input voltage range is from 1V to 5.5V. A suitable input capacitor should be placed close to this pin to minimize voltage spikes and noise, ensuring a stable input voltage.
10	10	VDD	Supply voltage of the control circuit. This pin provides the necessary power for the internal control logic and analog circuitry. It is important to ensure that the VDD voltage is stable and within the specified range to guarantee proper operation of the device.
11 (Exposed Pad)	11 (Exposed Pad)	GND	Ground: The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

8 Functional Block Diagram



9 Absolute Maximum Ratings

(Note 2)

- Supply Input Voltage, VIN to GND
 DC----- -0.3V to 6V
 < 10ms ----- -0.3V to 7V
- Control Voltage, VDD to GND
 DC----- -0.3V to 6V
 < 10ms ----- -0.3V to 7V
- VOUT, EN, ADJ, PG ----- -0.3V to 6V
- Supply Input Voltage, VIN to GND ----- -0.3V to 7V
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- Junction Temperature ----- 150°C
- Storage Temperature Range ----- -65°C to 150°C

Note 2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

10 ESD Ratings

(Note 3)

- ESD Susceptibility
- HBM (Human Body Model) -----2kV

Note 3. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 4)

- Supply Input Voltage, VIN ----- 1V to 5.5V
- Control Voltage VDD ($V_{DD} > V_{OUT} + 1.5V$) ----- V to 5.5V
- Junction Temperature Range ----- -40°C to 125°C
- Ambient Temperature Range ----- -40°C to 85°C

Note 4. The device is not guaranteed to function outside its operating conditions.

12 Thermal Information

([Note 5](#) and [Note 6](#))

Thermal Parameter		WDFN-10L 3x3	SOP-8 (Exposed Pad)	Unit
θ_{JA}	Junction-to-ambient thermal resistance (JEDEC standard)	55	47	°C/W
$\theta_{JC(Top)}$	Junction-to-case (top) thermal resistance	63.3	75.3	°C/W
$\theta_{JC(Bottom)}$	Junction-to-case (bottom) thermal resistance	6	6	°C/W
$\theta_{JA(EVB)}$	Junction-to-ambient thermal resistance (specific EVB)	37.4	35.2	°C/W
$\Psi_{JC(Top)}$	Junction-to-top characterization parameter	1.14	4.52	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	18.3	20.6	°C/W

Note 5. For more information about thermal parameter, see the Application and Definition of Thermal Resistances report, AN061.

Note 6. $\theta_{JA(EVB)}$, $\Psi_{JC(TOP)}$, and Ψ_{JB} are simulated on a high effective-thermal-conductivity four-layer test board, which is in size of 70mm x 50mm; furthermore, all layers with 1 oz. Cu. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

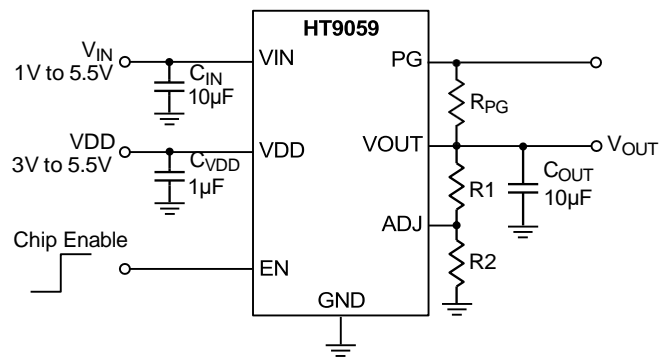
13 Electrical Characteristics

($V_{DD} = 5V$, $C_{IN} = C_{OUT} = 10\mu F$, $C_{VDD} = 1\mu F$, $T_A = 25^\circ C$, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Operation Range	VDD		3	--	5.5	V
VDD POR Threshold	VPOR_VDD	VDD Rising	2.4	2.7	3	V
VDD POR Falling Hysteresis	VPOR_HYS_P OR	VDD Falling	0.15	0.2	--	V
Input Voltage Range	VIN		1	--	5.5	V
VIN POR Threshold	VPOR_VIN	VIN Rising	0.7	0.8	0.9	V
VIN POR Falling Hysteresis	VPOR_HYS_V IN	VIN Falling	0.15	0.2	0.25	V
Quiescent Curren	IQ	IOUT = 0A	--	0.6	1.2	mA
Reference Voltage	VREF		0.788	0.8	0.812	V
Fixed Output Voltage Accuracy	VOUT_ACC	HT9059A	-1.5	--	1.5	%
		HT9059	-1	--	1	
VOUT Load Regulation	VLOAD_REG	IOUT = 1mA to 3A, VIN = VOUT + 1	--	0.5	1	%
OUT Line Regulation	VLINE_REG	VDD = 3.6V to 5.5V, VIN = VOUT + 1V to 5V, IOUT = 1mA	--	0.2	0.6	%
Dropout Voltage	VDROP	IOUT = 2A	--	250	350	mV
		IOUT = 3A	--	350	450	
Current Limit	ILIM	VIN = 3.6V	3.1	3.6	4.2	A
Short Circuit Current	ISC	VOUT < 0.2V	1	1.4	1.8	A
Discharge Resistor	RDISCHG	VEN = 0V	--	150	--	Ω
Over-Temperature Protection Temperature	TOTP		--	160	--	°C
Over-Temperature Protection Hysteresis	TOTP_HYS		--	70	--	°C

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
PG Rising Threshold	V _{PG}	Threshold, V _{PG} from low to high		--	90	--	%
PG Hysteresis	V _{PG_HYS}	Hysteresis, V _{PG} from high to low		--	10	--	%
PG Delay Time	t _{PG_DE}			0.2	1	1.5	ms
PG Sink Capability	V _{PG_L}	I _{PG_SNK} = 10mA		--	0.2	0.4	V
EN Input Voltage Rising Threshold	V _{EN_R}	Logic-high		1.2	--	--	V
EN Input Voltage Falling Threshold	V _{EN_F}	Logic-low		--	--	0.4	
EN Delay Time	t _{EN_DE}			0.3	0.85	1.4	ms
EN Input Current	I _{EN}	V _{EN} = 5V		--	12	--	μA
VDD Pin Shutdown Current	I _{SHDN_VDD}	V _{EN} = 0V	HT9059A	--	--	1	μA
			HT9059	--	15	30	
VIN Pin Shutdown Current	I _{SHDN_VIN}	V _{EN} = 0V, V _{VIN} = 5V		--	--	1	μA
Inrush Current	I _{INRUSH}	V _{OUT} = 1.8V, C _{OUT} = 10μF, I _{OUT} = 1A		--	0.5	--	A
Soft-Start Time	t _{SS}			1.9	2.8	3.75	ms

14 Typical Application Circuit



$$V_{OUT} = 0.8 \times (R1 + R2) / R2$$

Figure 1. Adjustable Voltage Regulator

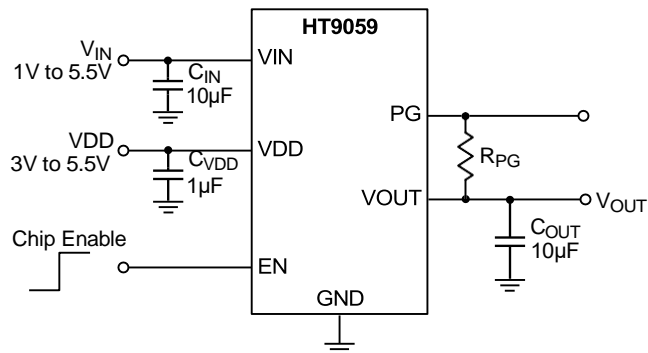
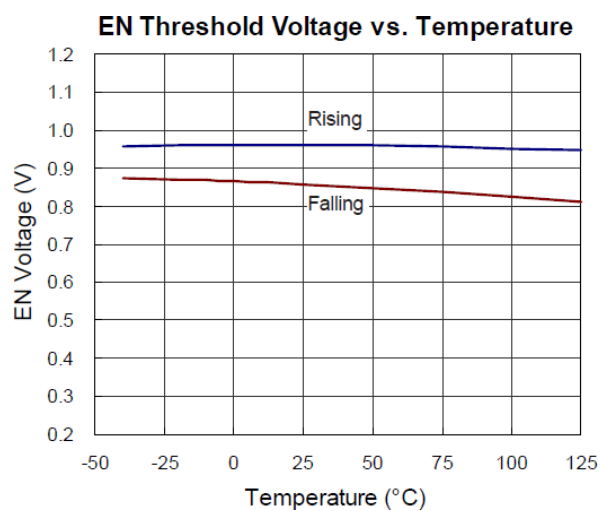
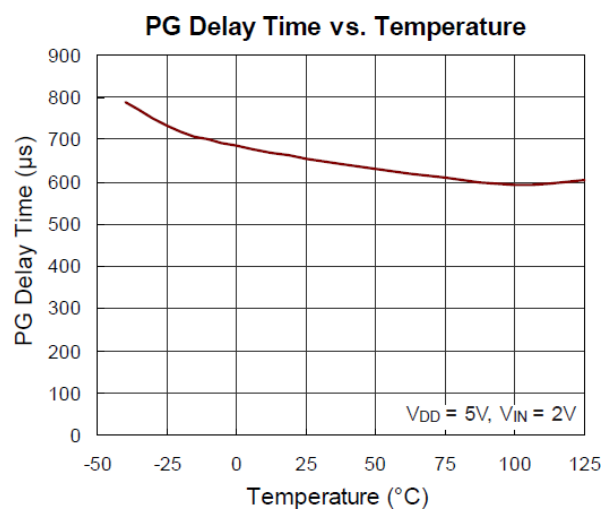
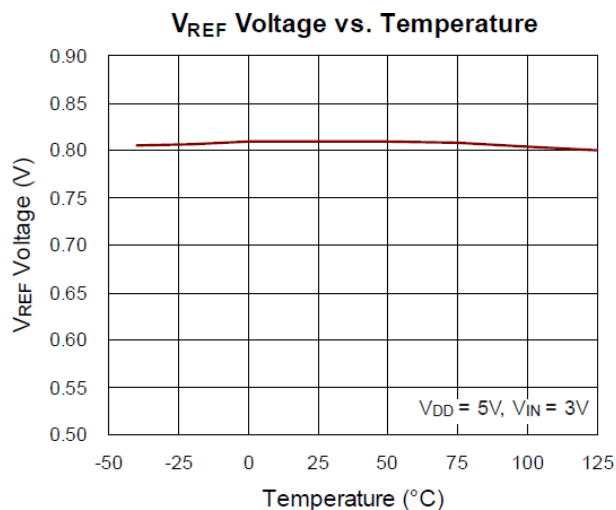
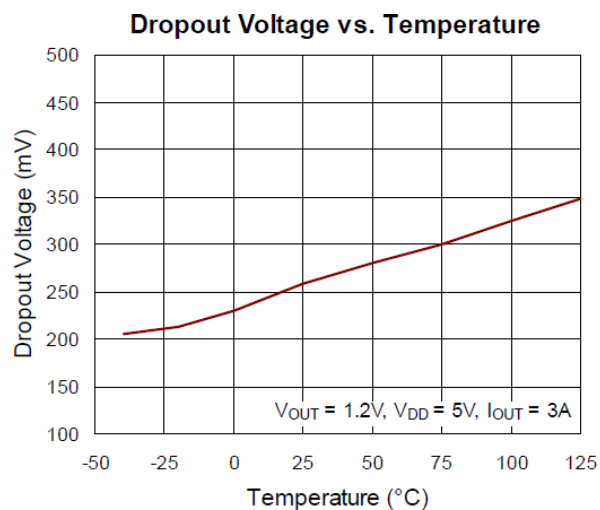
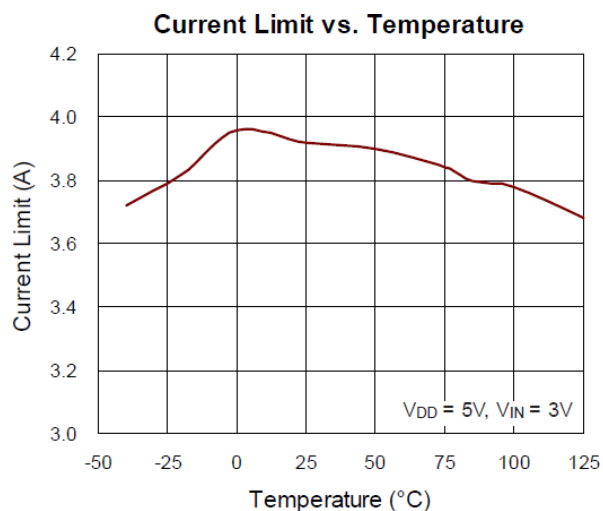
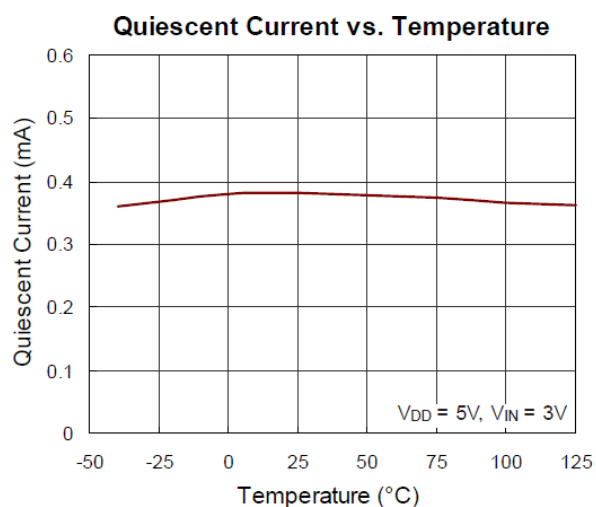
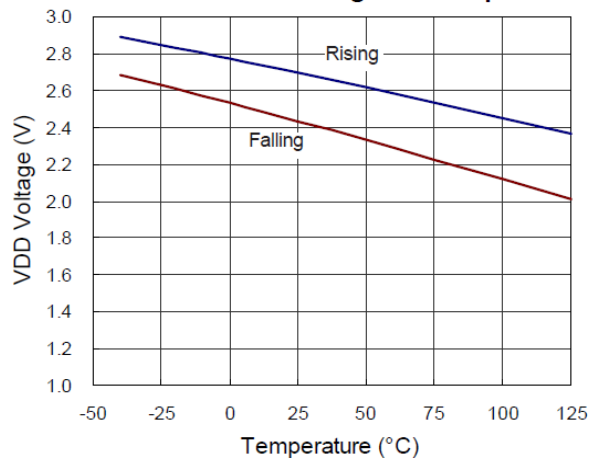


Figure 2. Fixed Voltage Regulator

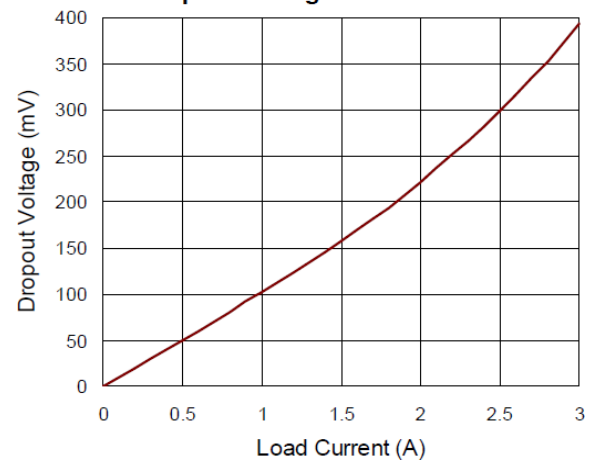
15 Typical Operating Characteristics



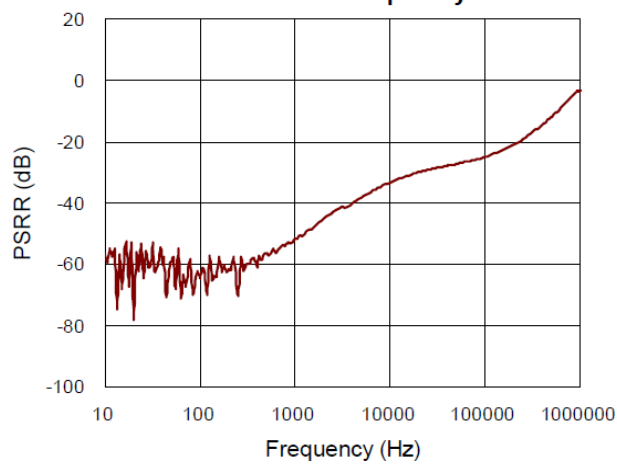
VDD POR Threshold Voltage vs. Temperature



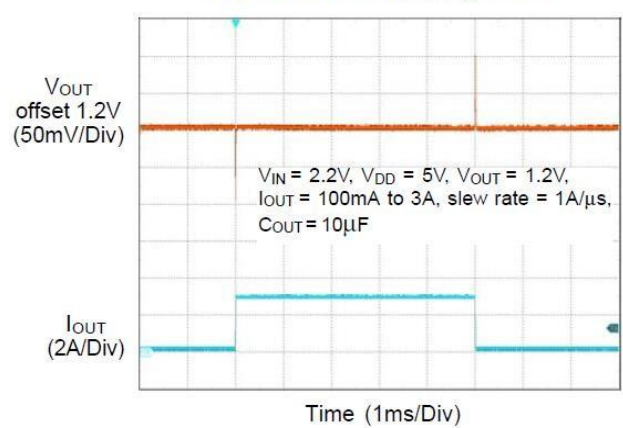
Dropout Voltage vs. Load Current



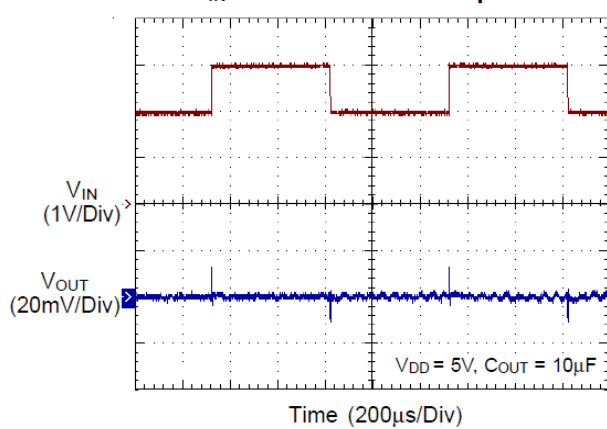
PSRR vs. Frequency



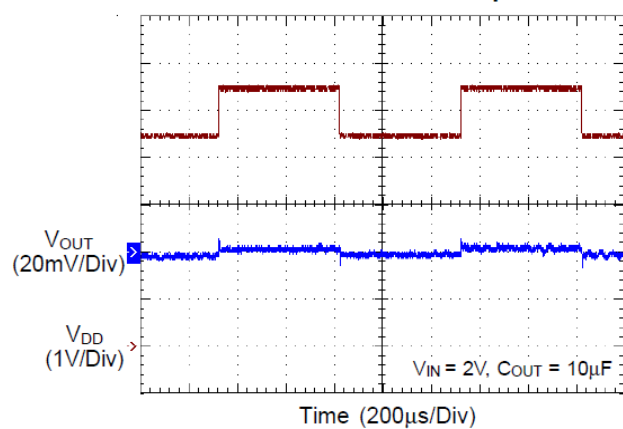
Load Transient Response



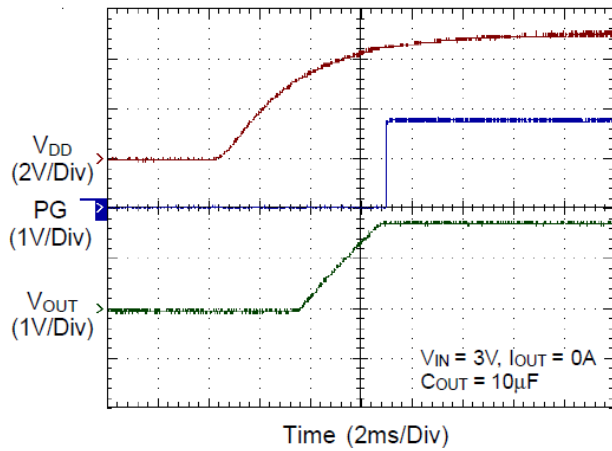
V_{IN} Line Transient Response



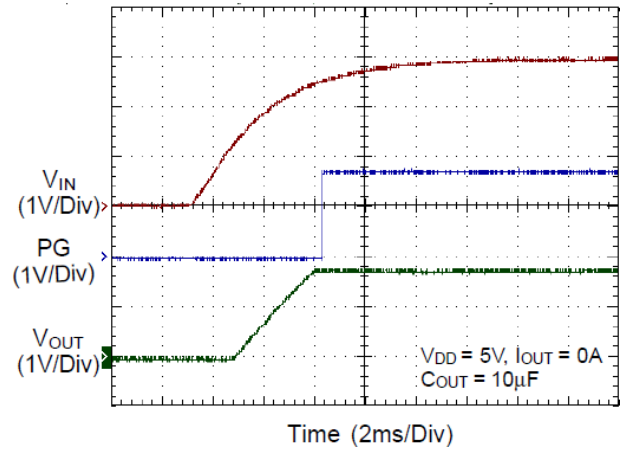
V_{DD} Line Transient Response



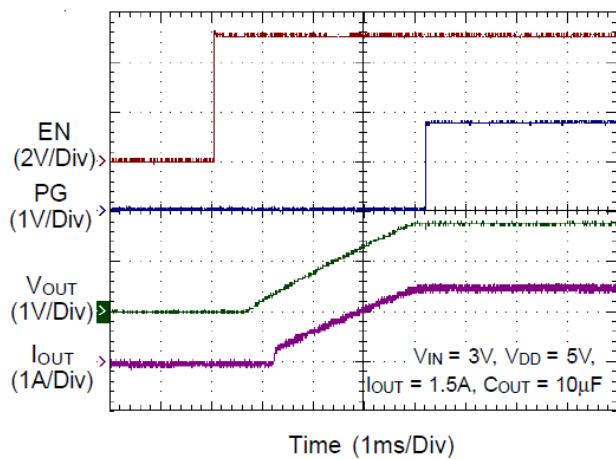
Start Up from V_{DD}



Start Up from V_{IN}



Start Up from Enable and PG Delay



16 Application Information

(Note 7)

16.1 Adjustable Mode Operation

The output voltage of the HT9059A is adjustable from 0.8V to VIN using external voltage divider resistors, as shown in the Typical Application Circuit (Figure 1). The values of resistors R1 and R2 should be more than 10kΩ to reduce power loss. The output voltage can be calculated using the following equation:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2} \right)$$

where VREF is the reference voltage (typically 0.8V).

16.2 Enable

The HT9059A enters shutdown mode when the EN pin is in a logic low condition. In this state, the pass transistor, error amplifier, and bandgap are turned off, reducing the supply current to a typical 1μA. The HT9059A enters operation mode when the EN pin is in a logic high condition. If the EN pin is floating, note the HT9059A's internal initial logic level. For the HT9059A, the EN pin function pulls to a low level internally, so the regulator will be turned off when the EN pin is floating.

16.3 Input Capacitor

Good bypassing is recommended from input to ground to improve AC performance. A 10μF or greater input capacitor, located as close as possible to the IC, is recommended.

16.4 Output Capacitor

The output capacitor must meet both the minimum capacitance and ESR requirements in all LDO applications. The HT9059A is designed specifically to work with low ESR ceramic output capacitors for space-saving and performance considerations. Using a ceramic capacitor with a value of at least 10μF on the HT9059A output ensures stability. The HT9059A also works well with output capacitors of other types due to the wide stable ESR range. Output capacitors with larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located no more than 0.5 inches from the VOUT pin of the HT9059A and returned to a clean analog ground.

16.5 Current Limit

The HT9059A includes an independent current limit and short circuit current protection to prevent unexpected applications. The current limit monitors and controls the pass transistor's gate voltage, minimally limiting the output current to 3.1A (typical). When the output voltage drops below 0.2V, the short circuit current protection activates the current foldback function and maintains the load current at a maximum of 1.8A. The output can be shorted to ground indefinitely without damaging the device.

16.6 Power-Good Function

The power good function is an open-drain output. Connect a 100kΩ pull-up resistor to VOUT to obtain an output voltage. The PG pin will output high immediately after the output voltage reaches 90% of the normal output voltage.

16.7 Over-Temperature Protection

Over-Temperature Protection limits power dissipation to prevent the HT9059A overheating. When the operating junction temperature exceeds 160°C, the circuit activates the over-temperature protection function and turns the pass transistor off. The pass transistor turns on again after the junction temperature cools by 70°C.

16.8 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, $\theta_{JA(EVB)}$, is highly package dependent. For a WDFN-10L 3x3 package, the thermal resistance, $\theta_{JA(EVB)}$, is 37.4°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. For a SOP-8 (Exposed Pad) package, the thermal resistance, $\theta_{JA(EVB)}$, is 35.2°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at $T_A = 25^\circ\text{C}$ can be calculated as follows:

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (37.4^\circ\text{C/W}) = 2.67\text{W for a WDFN-10L 3x3 package.}$$

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (35.2^\circ\text{C/W}) = 2.84\text{W for a SOP-8 (Exposed Pad) package.}$$

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, $\theta_{JA(EVB)}$. The derating curves in [Figure 3](#) allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

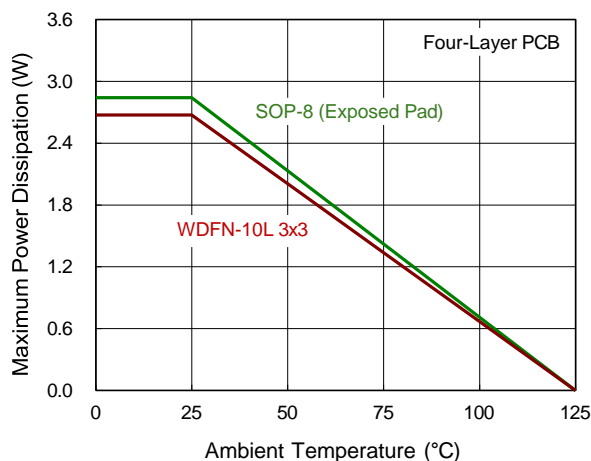
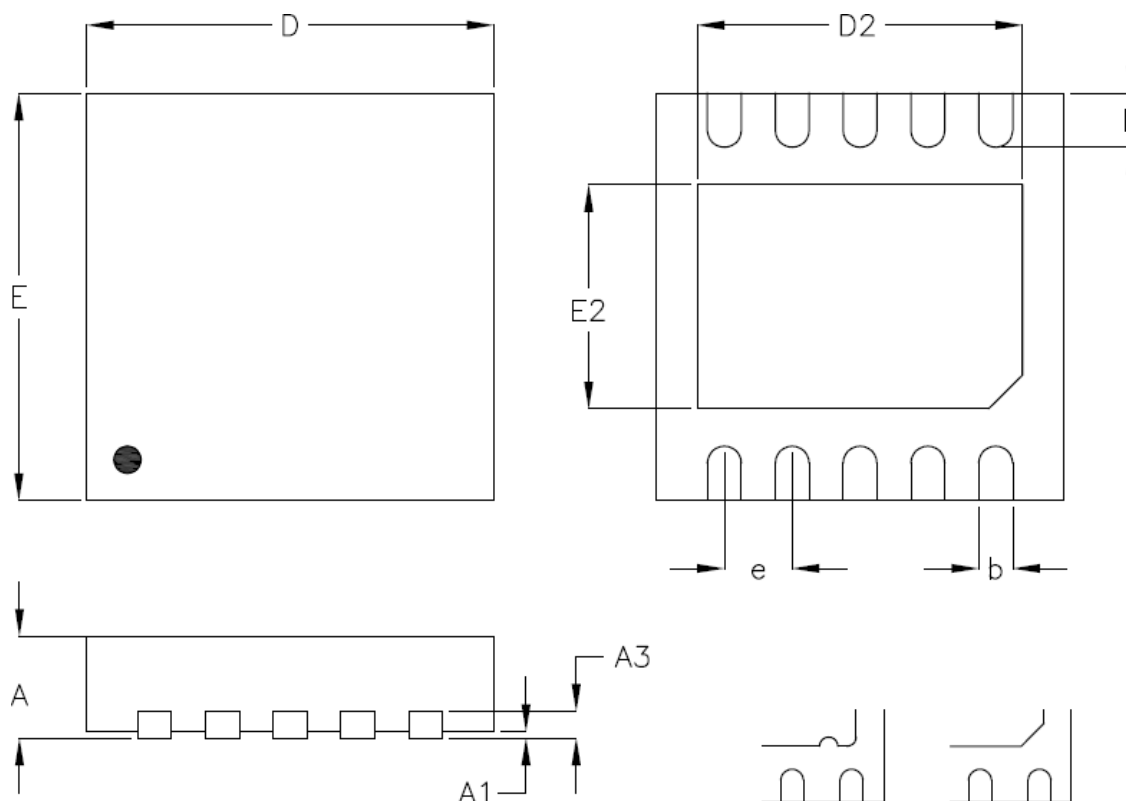


Figure 3. Derating Curve of Maximum Power Dissipation

Note 7. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

17 Outline Dimension

17.1 WDFN-10L 3x3 Package



DETAILA

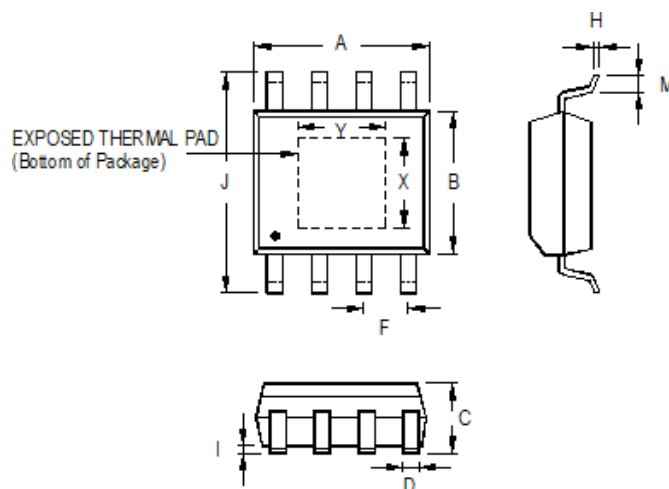
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 10L DFN 3x3 Package

17.2 ESOP-8 (Exposed Pad) Package



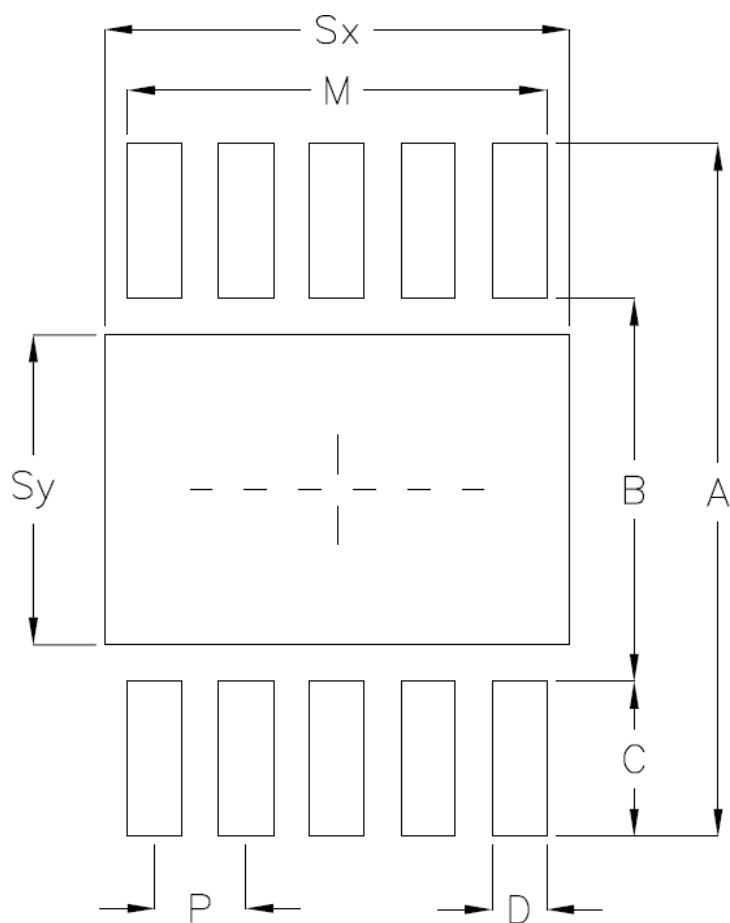
Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package

Note 8. The package of the HT9059A uses Option 2.

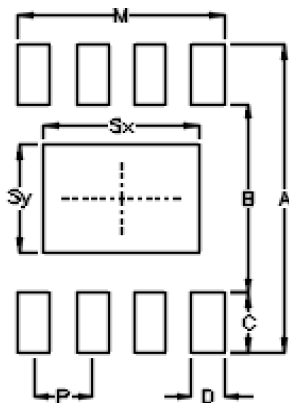
18 Footprint Information

18.1 WDFN-10L 3x3 Package



Package	Number of Pin	Footprint Dimension (mm)								Tolerance
		P	A	B	C	D	Sx	Sy	M	
V/W/U/X/ZDFN3*3-10	10	0.50	3.80	2.10	0.85	0.30	2.55	1.70	2.30	±0.05

18.2 ESOP-8 (Exposed Pad) Package



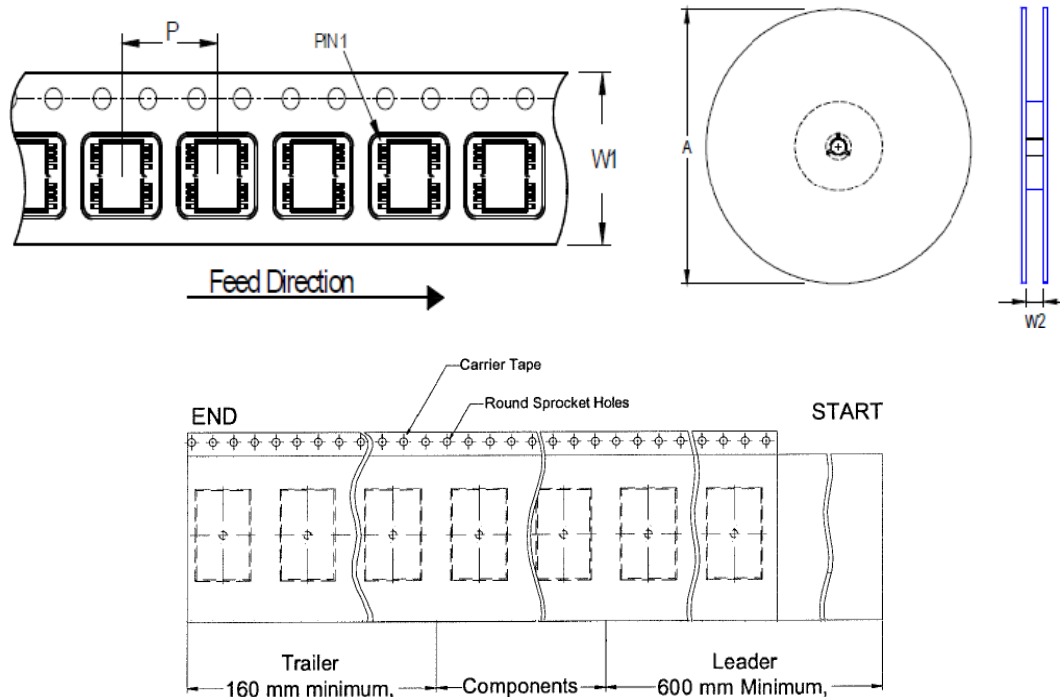
Package		Number of Pin	Footprint Dimension (mm)								Tolerance
			P	A	B	C	D	Sx	Sy	M	
ESOP-8	Option1	8	1.27	6.80	4.20	1.30	0.70	2.30	2.30	4.51	±0.10
	Option2							3.40	2.40		

Note 9. The package of the HT9059A uses Option 2.

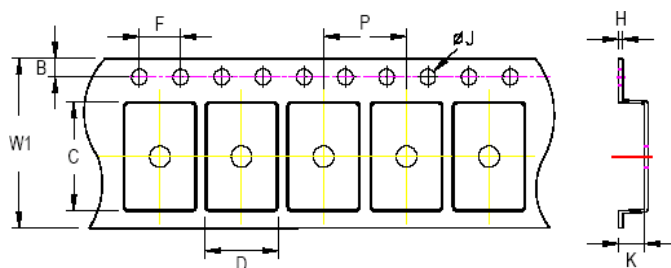
19 Packing Information

19.1 Tape and Reel Data

19.1.1 ESOP-8 (Exposed Pad)

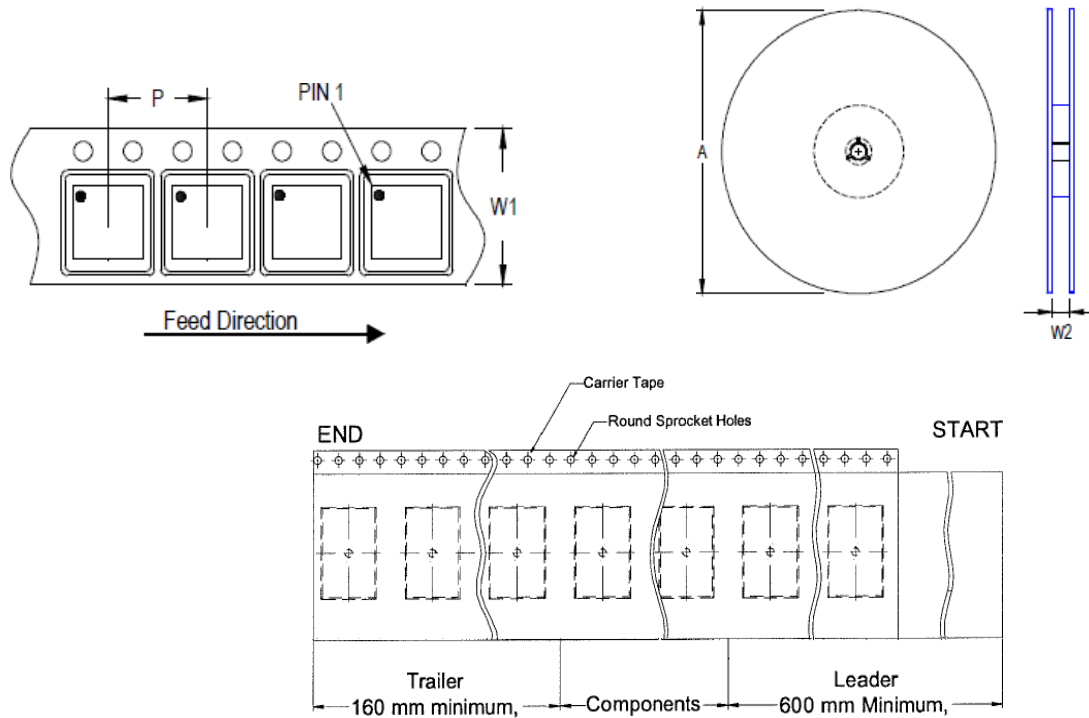


Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
ESOP-8	12	8	330	13	2,500	160	600	12.4/14.4

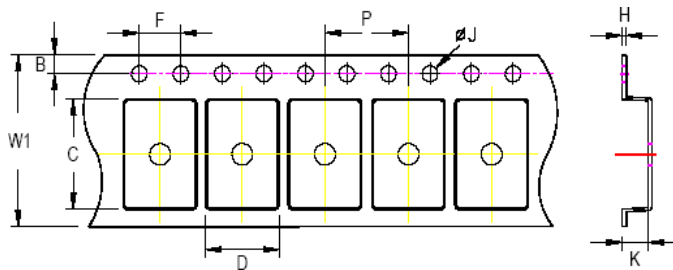


C, D, and K are determined by component size.
 The clearance between the components and the cavity is as follows:
 - For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.9mm	2.3mm	0.6mm

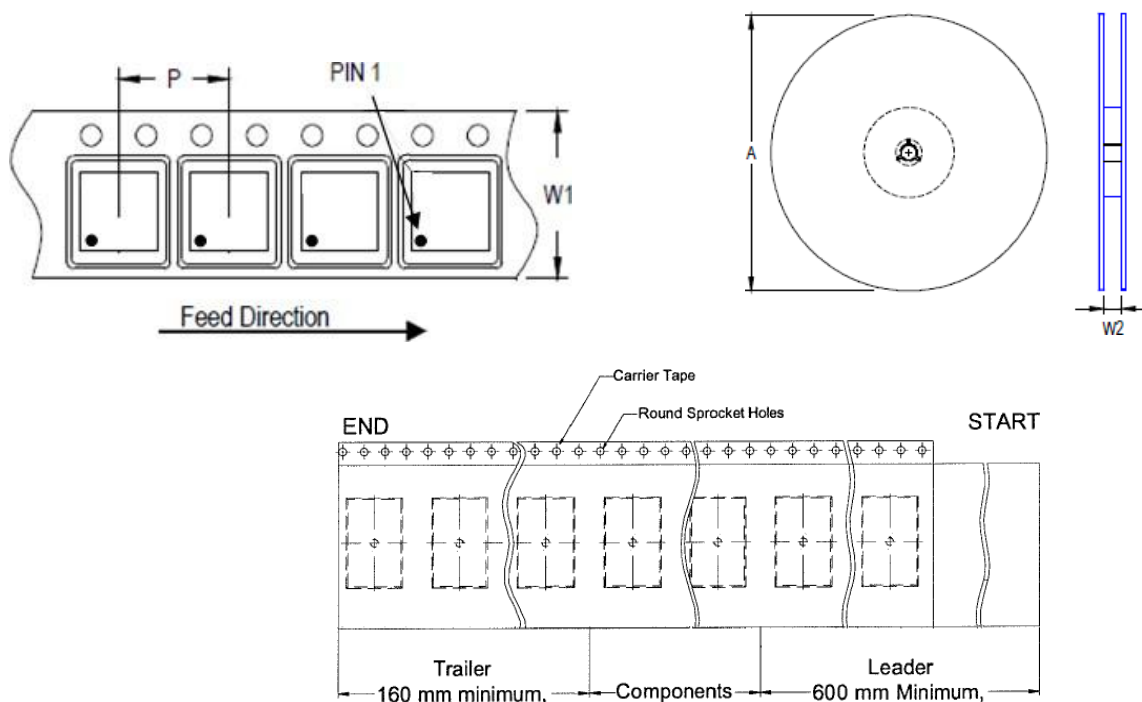
19.1.2 WDFN-10L 3x3
19.1.2.1 Units per Reel: 1500


Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
(V, W) QFN/DFN 3x3	12	8	180	7	1,500	160	600	12.4/14.4

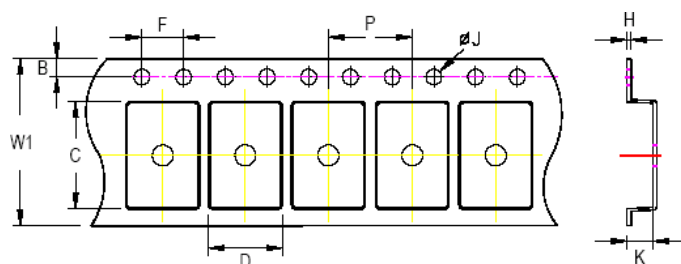


C, D, and K are determined by component size.
The clearance between the components and the cavity is as follows:
 - For 12mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
12mm	12.3mm	7.9mm	8.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

19.1.2.2 Units per Reel: 3000


Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 3x3	8	4	180	7	3,000	160	600	8.4/9.9



C, D, and K are determined by component size.
The clearance between the components and the cavity is as follows:
- For 8mm carrier tape: 0.5mm max.

Tape Size	W1	P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm