RoHS HAL Green

Low Quiescent Current, Programmable-Delay Supervisory Circuit

The HT3808xxx family of microprocessor supervisory circuits monitor system voltages from 0.4V to 5.0V, asserting an open drain RESET signal when the SENSE voltage drops below a preset threshold or when the manual reset (MR) pin drops to a logic low. The RESET output remains low for the user adjustabledelay time after the SENSE voltage and manual reset (MR) return above their thresholds.The HT3808 uses a precision reference to achieve 0.5% threshold accuracy for VIT ≤ 3.3V. The reset delay time can be set to 20ms by disconnecting the CT pin, 300ms by connecting the CT pin to VDD using a resistor, or can be user-adjusted between 1.25ms and 10s by connecting the CT pin to an external capacitor. The HT3808 has a very low typical quiescent current of 2.4μA so it is well-suited to battery-powered applications. It is available in a small SOT23 and an ultra-small 2mm × 2mm QFN PowerPAD™ package and is fullyspecified over a temperature range of –40°C to +125°C (TJ).

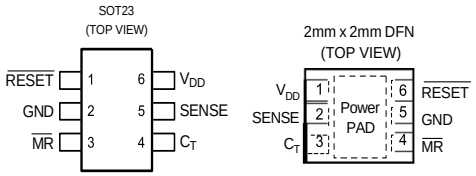
FEATURES

- **Power-On Reset Generator with Adjustable Delay Time: 1.25ms to 10s**
- **Very Low Quiescent Current: 2.4μA typ**
- **High Threshold Accuracy: 0.5% typ**
- **Fixed Threshold Voltages for Standard Voltage Rails from 0.9V to 5V and Adjustable Voltage Down to 0.4V Are Available**
- **Manual Reset (MR) Input**
- **Open-Drain RESET Output**

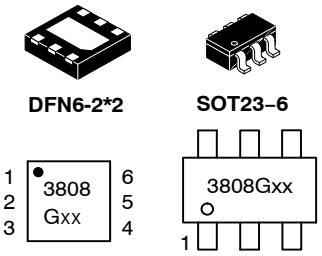
APPLICATIONS

- **DSP or Microcontroller Applications**
- **Notebook/Desktop Computers**
- **PDAs/Hand-Held Products**
- **Portable/Battery-Powered Products**
- **FPGA/ASIC Applications**

PIN CONFIGURATION



MARKING DIAGRAMS



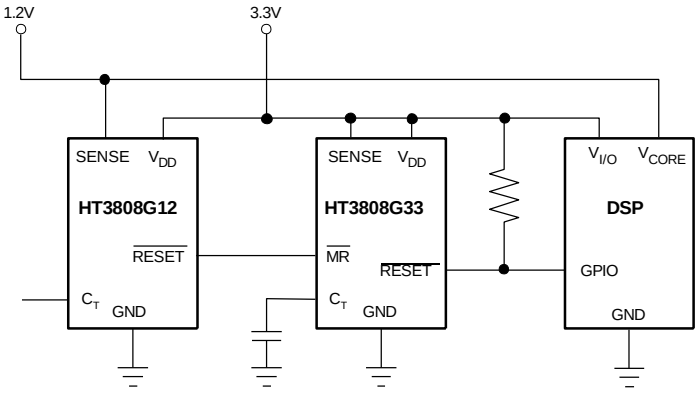
xx = Supply voltage
Y = Date Code
G = Version number
R = Reel
Z = Pb–Free Package

ORDERINGINFORMATION

HT3808GxxRDZ DFN6(2*2)
HT3808GxxRTZ SOT23-6

T_A = -40° to 125° C for all packages

Typical Application Circuit



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	NOMINAL SUPPLY VOLTAGE(2)	THRESHOLD VOLTAGE (V_{IT})
HT3808G01	Adjustable	0.405V
HT3808G09	0.9V	0.84V
HT3808G12	1.2V	1.12V
HT3808G15	1.5V	1.40V
HT3808G18	1.8V	1.67V
HT3808G25	2.5V	2.33V
HT3808G30	3.0V	2.79V
HT3808G33	3.3V	3.07V
HT3808G50	5.0V	4.65V

ABSOLUTE MAXIMUM RATINGS

over operating junction temperature range (unless otherwise noted)(1)

	HT3808	UNIT
Input voltage range, V_{DD}	–0.3 to 7.0	V
C_T voltage range, V_{CT}	–0.3 to V_{DD} + 0.3	V
Other voltage ranges: V_{RESET}, V_{MR}, V_{SENSE}	–0.3 to 7	V
$\overline{RESET}$ pin current	5	mA
Operating junction temperature range, T_J(2)	–40 to +150	°C
Storage temperature range, T_{STG}	–65 to +150	°C
ESD rating, HBM	2	kV
ESD rating, CDM	500	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the Electrical Characteristics is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

(2) Due to the low dissipated power in this device, it is assumed that $T_J = T_A$.

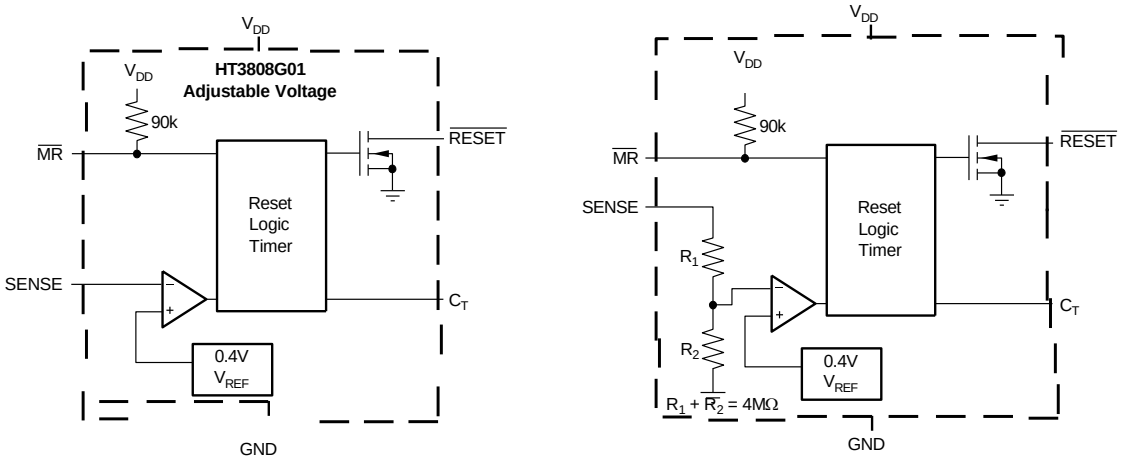
ELECTRICAL CHARACTERISTICS

1.8V ≤ V_{DD} ≤ 6.5V, R_{LRESET} = 100kΩ, C_{LRESET} = 50pF, over operating temperature range (T_J = –40°C to +125°C), unless otherwise noted. Typical values are at T_J = +25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Input supply range			1.8		6.5	V
I_{DD}	Supply current (current into V_{DD} pin)		V_{DD} = 3.3V, $\overline{RESET}$ not asserted $\overline{MR}$, RESET, C_T open		2.4	5.0	µA
			V_{DD} = 6.5V, $\overline{RESET}$ not asserted $\overline{MR}$, RESET, C_T open		2.7	6.0	µA
V_{OL}	Low-level output voltage		1.3V ≤ V_{DD} < 1.8V, I_{OL} = 0.4mA			0.3	V
			1.8V ≤ V_{DD} ≤ 6.5V, I_{OL} = 1.0mA			0.4	V
	Power-up reset voltage(1)		V_{OL} (max) = 0.2V, $I_{\overline{RESET}}$ = 15µA			0.8	V
V_{IT}	Negative-going input threshold accuracy	HT3808G01		–2.0	±1.0	+2.0	%
		V_{IT} ≤ 3.3V		–1.5	±0.5	+1.5	
		3.3V < V_{IT} ≤ 5.0V		–2.0	±1.0	+2.0	
		V_{IT} ≤ 3.3V	–40°C < T_J < +85°C	–1.25	±0.5	+1.25	
		3.3V < V_{IT} ≤ 5.0V	–40°C < T_J < +85°C	–1.5	±0.5	+1.5	
V_{HYS}	Hysteresis on V_{IT} pin	HT3808G01			1.5	3.0	%V_{IT}
		Fixed versions			1.0	2.5	
$R_{\overline{MR}}$	$\overline{MR}$ Internal pull-up resistance			70	90		kΩ
I_{SENSE}	Input current at SENSE pin	HT3808G01	V_{SENSE} = V_{IT}	–25		25	nA
		Fixed versions	V_{SENSE} = 6.5V		1.7		µA
I_{OH}	$\overline{RESET}$ leakage current		$V_{\overline{RESET}}$ = 6.5V, $\overline{RESET}$ not asserted			300	nA
C_{IN}	Input capacitance, any pin	C_T pin	V_{IN} = 0V to V_{DD}		5		pF
		Other pins	V_{IN} = 0V to 6.5V		5		
V_{IL}	$\overline{MR}$ logic low input			0.3 V_{DD}			V
V_{IH}	$\overline{MR}$ logic high input					0.7 V_{DD}	
t_w	Maximum transient duration	SENSE	V_{IH} = 1.05V_{IT}, V_{IL} = 0.95V_{IT}		20		µs
		$\overline{MR}$	V_{IH} = 0.7V_{DD}, V_{IL} = 0.3V_{DD}		0.001		
t_d	$\overline{RESET}$ delay time	C_T = Open	See timing diagram	12	20	28	ms
		C_T = V_{DD}		180	300	420	ms
		C_T = 100pF		0.75	1.25	1.75	ms
		C_T = 180nF		0.7	1.2	1.7	s
t_{pHL}	Propagation delay	$\overline{MR}$ to $\overline{RESET}$	V_{IH} = 0.7V_{DD}, V_{IL} = 0.3V_{DD}		150		ns
	High to low level $\overline{RESET}$ delay	SENSE to $\overline{RESET}$	V_{IH} = 1.05V_{IT}, V_{IL} = 0.95V_{IT}		20		µs
θ_{JA}	Thermal resistance, junction-to-ambient				290		°C/W

(1) The lowest supply voltage (V_{DD}) at which $\overline{RESET}$ becomes active. $T_{rise(VDD)}$ ≥ 15µs/V.

FUNCTIONAL BLOCK DIAGRAMS



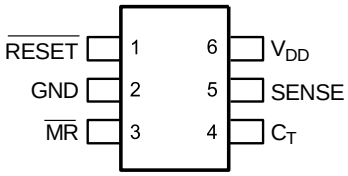
Adjustable Voltage Version

Fixed Voltage Version

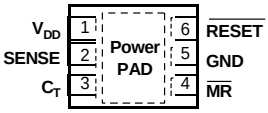
Figure 1. Adjustable and Fixed Voltage Versions

PIN ASSIGNMENTS

DBV PACKAGE
SOT23
(TOP VIEW)



DRV PACKAGE
2mm x 2mm QFN
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	SOT23 (DBV) PIN NO.	
$\overline{\text{RESET}}$	1	$\overline{\text{RESET}}$ is an open drain output that is driven to a low impedance state when $\overline{\text{RESET}}$ is asserted (either the SENSE input is lower than the threshold voltage (V_{IT}) or the $\overline{\text{MR}}$ pin is set to a logic low). $\overline{\text{RESET}}$ will remain low (asserted) for the reset period after both SENSE is above V_{IT} and $\overline{\text{MR}}$ is set to a logic high. A pull-up resistor from 10kΩ to 1MΩ should be used on this pin, and allows the reset pin to attain voltages higher than V_{DD}.
GND	2	Ground
$\overline{\text{MR}}$	3	Driving the manual reset pin ($\overline{\text{MR}}$) low asserts $\overline{\text{RESET}}$. $\overline{\text{MR}}$ is internally tied to V_{DD} by a 90kΩ pull-up resistor.
C_T	4	Reset period programming pin. Connecting this pin to V_{DD} through a 40kΩ to 200kΩ resistor or leaving it open results in fixed delay times (see *Electrical Characteristics*). Connecting this pin to a ground referenced capacitor ≥ 100pF gives a user-programmable delay time. See *Selecting The Reset Delay Time* in the *Device Operation* section for more information.
SENSE	5	This pin is connected to the voltage to be monitored. If the voltage at this terminal drops below the threshold voltage V_{IT}, then $\overline{\text{RESET}}$ is asserted.
V_{DD}	6	Supply voltage. It is good analog design practice to place a 0.1μF ceramic capacitor close to this pin.
PowerPAD		PowerPAD. Connect to ground plane to enhance thermal performance of package.

TIMING DIAGRAM

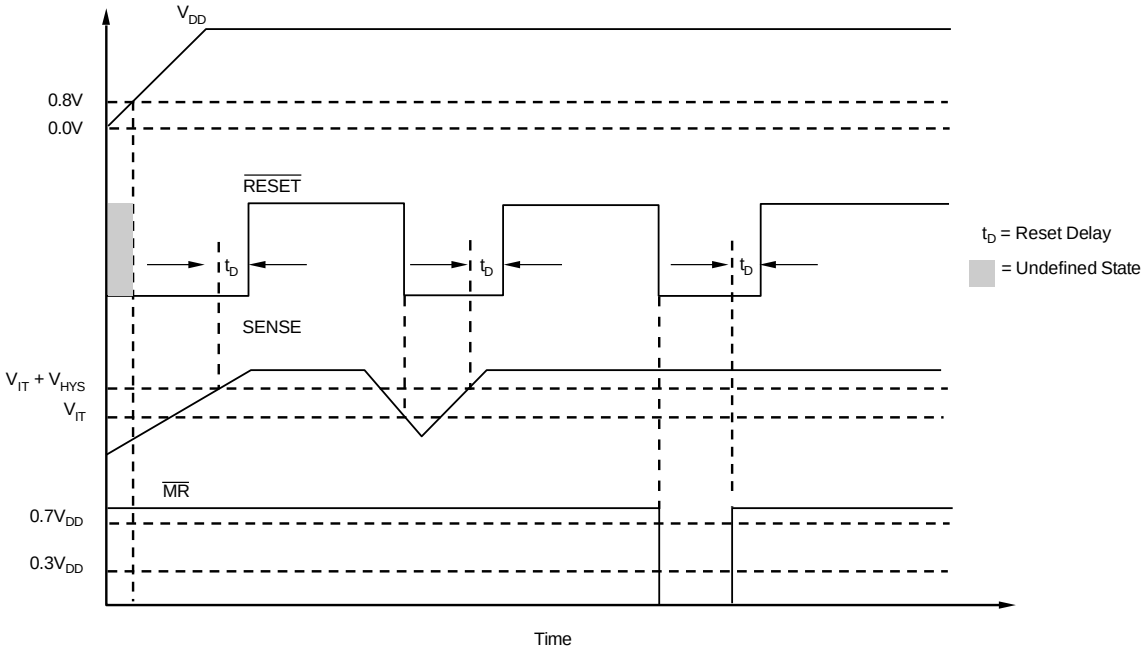


Figure 2. HT3808 Timing Diagram Showing $\overline{MR}$ and SENSE Reset Timing

TRUTH TABLE

$\overline{MR}$	SENSE > V_{IT}	$\overline{RESET}$
L	0	L
L	1	L
H	0	L
H	1	H

TYPICAL CHARACTERISTICS

At T_J = +25°C, V_{DD} = 3.3V, R_{LRESET} = 100kΩ, and C_{LRESET} = 50pF, unless otherwise noted.

SUPPLY CURRENT vs SUPPLY VOLTAGE

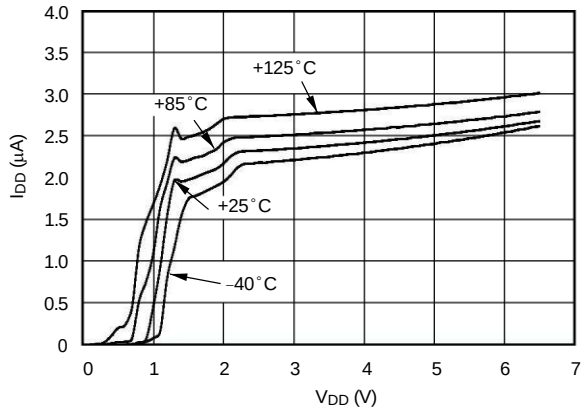


Figure 3.

RESET TIMEOUT PERIOD vs C_T

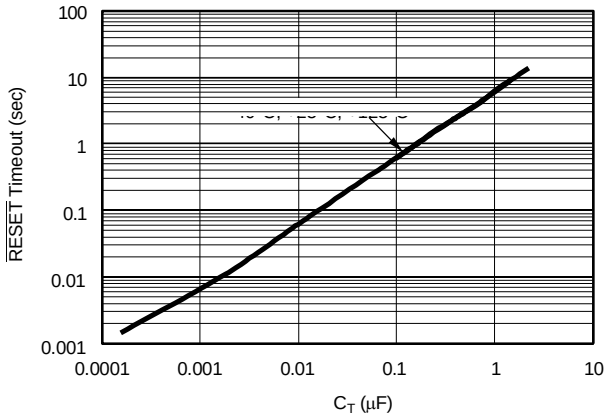


Figure 4.

NORMALIZED RESET TIMEOUT PERIOD vs TEMPERATURE (C_T = OPEN, C_T = V_{DD}, C_T = Any)

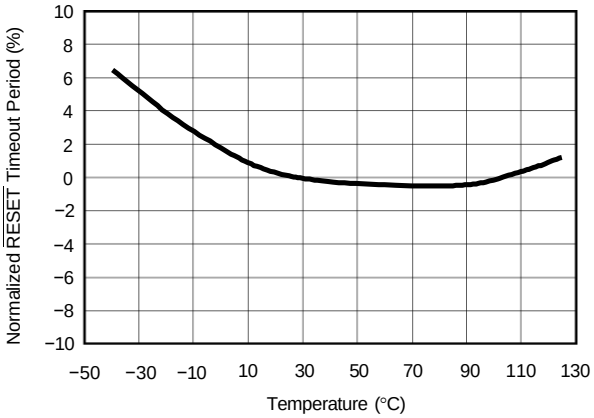


Figure 5.

MAXIMUM TRANSIENT DURATION AT SENSE vs SENSE THRESHOLD OVERDRIVE VOLTAGE

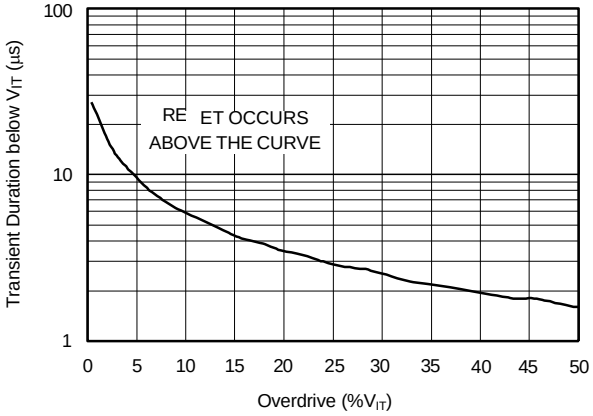


Figure 6.

At T_J = +25°C, V_{DD} = 3.3V, R_{LRESET} = 100kΩ, and C_{LRESET} = 50pF, unless otherwise noted.

NORMALIZED SENSE THRESHOLD VOLTAGE (V_{IT}) vs TEMPERATURE

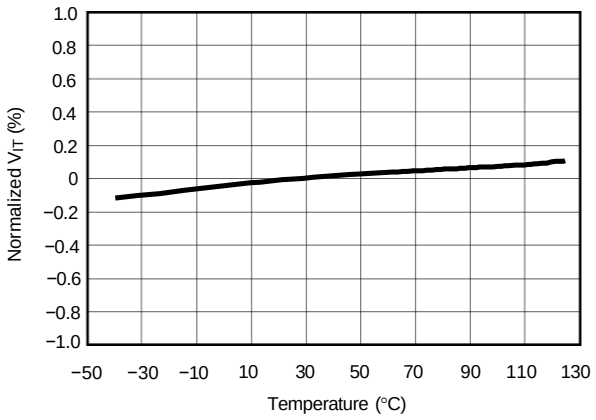


Figure 7.

LOW-LEVEL $\overline{\text{RESET}}$ VOLTAGE vs $\overline{\text{RESET}}$ CURRENT

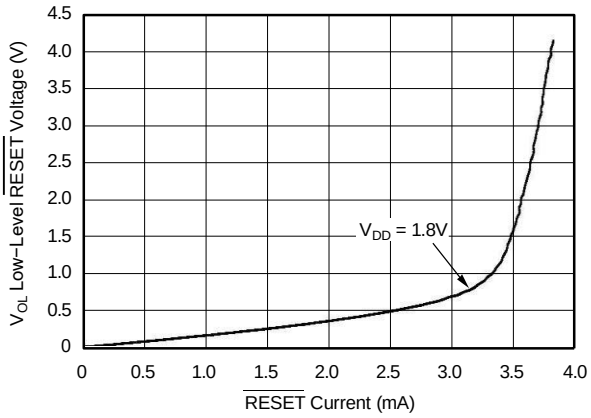


Figure 8.

LOW-LEVEL $\overline{\text{RESET}}$ VOLTAGE vs $\overline{\text{RESET}}$ CURRENT

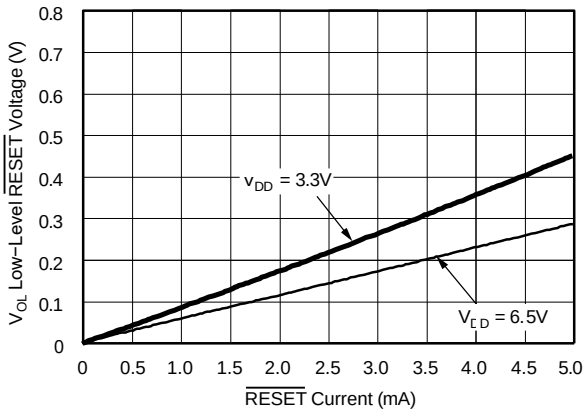


Figure 9.

DEVICE OPERATION

The HT3808 microprocessor supervisory product family is designed to assert a RESET signal when either the SENSE pin voltage drops below V_{IT} or the manual reset (MR) is driven low. The RESET output remains asserted for a user-adjustable time after both the manual reset (MR) and SENSE voltages return above their thresholds. A broad range of voltage threshold and reset delay time adjustments are available, allowing these devices to be used in a wide array of applications. Reset threshold voltages can be factory-set from 0.82V to 3.3V or from 4.4V to 5.0V, while the HT3808G01 can be set to any voltage above 0.405V using an external resistor divider. Two preset delay times are also user-selectable: connecting the C_T pin to V_{DD} results in a 300ms reset delay, while leaving the C_T pin open yields a 20ms reset delay. In addition, connecting a capacitor between C_T and GND allows the designer to select any reset delay period from 1.25ms to 10s.

RESET OUTPUT

A typical application of the HT3808G25 used with the OMAP1510 processor is shown in Figure 10. The open drain RESET output is typically connected to the RESET input of a microprocessor. A pull-up resistor must be used to hold this line high when RESET is not asserted. The RESET output is undefined for voltage below 0.8V, but this is normally not a problem since most microprocessors do not function below this voltage. RESET remains high (unasserted) as long as SENSE is above its threshold (V_{IT}) and the manual reset (MR) is logic high. If either SENSE falls below V_{IT} or MR is driven low, RESET is asserted, driving the RESET pin to a low impedance.

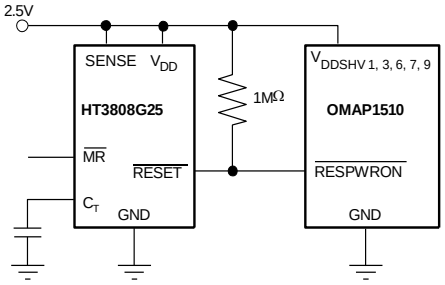


Figure 10. Typical Application of the HT3808 with an OMAP Processor

Once MR is again logic high and SENSE is above V_{IT} + V_{HYS} (the threshold hysteresis), a delay circuit is enabled which holds RESET low for a specified reset delay period. Once the reset delay has expired, the RESET pin goes to a high impedance state. The pull-up resistor from the open drain RESET to the supply line can be used to allow the reset signal for the microprocessor to have a voltage higher than V_{DD} (up to 6.5V). The pull-up resistor should be no smaller than 10kΩ as a result of the finite impedance of the RESET line.

SENSE INPUT

The SENSE input provides a terminal at which any system voltage can be monitored. If the voltage on this pin drops below V_{IT}, then RESET is asserted. The comparator has a built-in hysteresis to ensure smooth RESET assertions and de-assertions. It is good analog design practice to put a 1nF to 10nF bypass capacitor on the SENSE input to reduce sensitivity to transients and layout parasitics.

The HT3808G01 can be used to monitor any voltage rail down to 0.405V using the circuit shown in Figure 11.

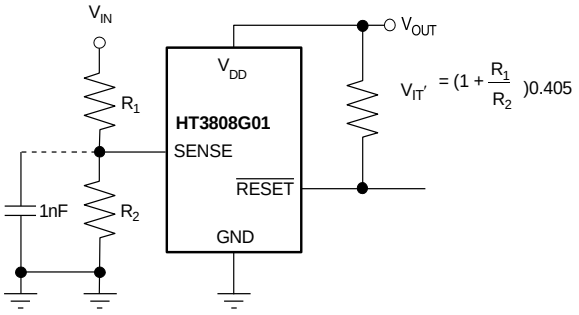


Figure 11. Using the HT3808G01 to Monitor a User-Defined Threshold Voltage

MANUAL RESET (MR) INPUT

The manual reset (MR) input allows a processor or other logic circuits to initiate a reset. A logic low ($0.3V_{DD}$) on MR causes RESET to assert. After MR returns to a logic high and SENSE is above its reset threshold, RESET is de-asserted after the user defined reset delay expires. Note that MR is internally tied to V_{DD} using a 90kΩ resistor so this pin can be left unconnected if MR will not be used.

See Figure 12 for how MR can be used to monitor multiple system voltages. Note that if the logic signal driving MR does not go fully to V_{DD}, there will be some additional current draw into V_{DD} as a result of the internal pull-up resistor on MR. To minimize current draw, a logic-level FET can be used as illustrated in Figure 13.

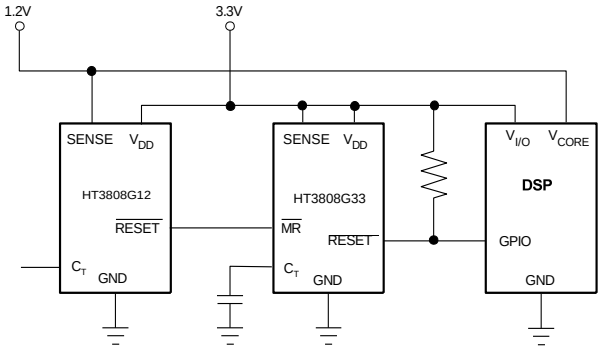


Figure 12. Using $\overline{MR}$ to Monitor Multiple System Voltages

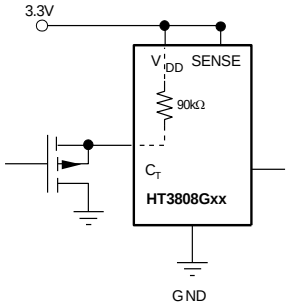


Figure 13. Using an External MOSFET to Minimize I_{DD} When MR Signal Does Not Go to V_{DD}

SELECTING THE RESET DELAY TIME

The HT3808 has three options for setting the RESET delay time as shown in Figure 14. Figure 14a shows the configuration for a fixed 300ms typical delay time by tying C_T to V_{DD}; a resistor from 40kΩ to 200kΩ must be used. Supply current is not affected by the choice of resistor. Figure 14b shows a fixed 20ms delay time by leaving the C_T pin open. Figure 14c shows a ground referenced capacitor connected to C_T for a user-defined program time between 1.25ms and 10s.

The capacitor C_T should be ≥ 100pF nominal value in order for the HT3808xxx to recognize that the capacitor is present. The capacitor value for a given delay time can be calculated using the following equation:

$$C_T\ (nF) = [t_D\ (s) — 0.5 \times 10^{-3}\ (s)] \times 175 \quad (1)$$

The reset delay time is determined by the time it takes an on-chip precision 220nA current source to charge the external capacitor to 1.23V. When a RESET is asserted the capacitor is discharged. When the RESET conditions are cleared, the internal current source is enabled and begins to charge the external capacitor. When the voltage on this capacitor reaches 1.23V, RESET is de-asserted. Note that a low leakage type capacitor such as a ceramic should be used, and that stray capacitance around this pin may cause errors in the reset delay time.

IMMUNITY TO SENSE PIN VOLTAGE TRANSIENTS

The HT3808 is relatively immune to short negative transients on the SENSE pin. Sensitivity to transients is dependent on threshold overdrive, as shown in the *Maximum Transient Duration at Sense vs Sense Threshold Overdrive Voltage* graph (Figure 6) in the Typical Characteristics section.

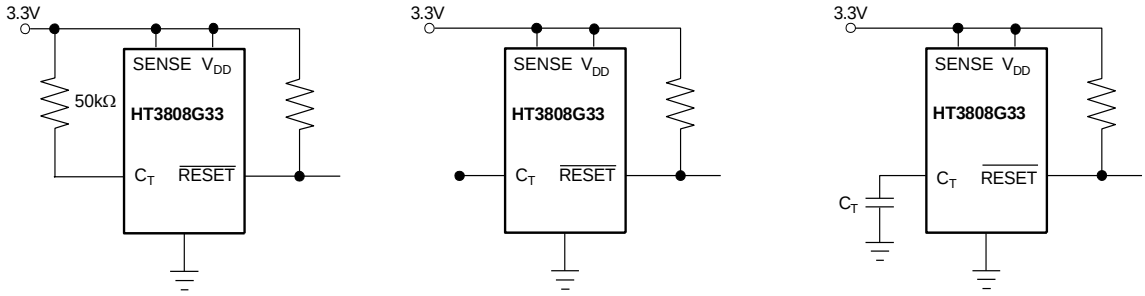
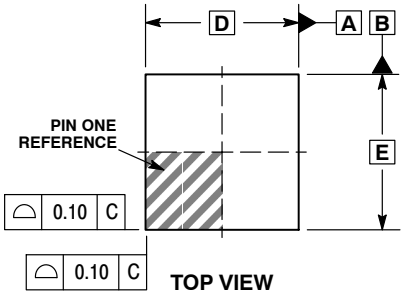
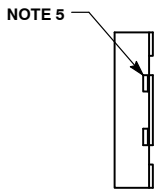


Figure 14. Configuration Used to Set the $\overline{RESET}$ Delay Time

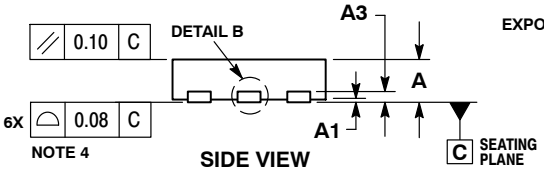
DFN6(2*2)

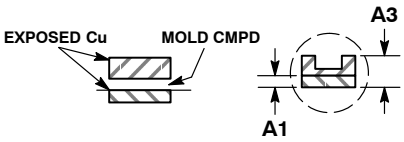


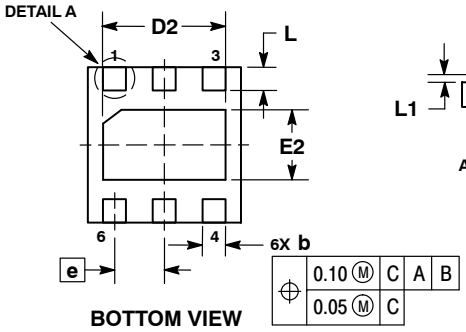


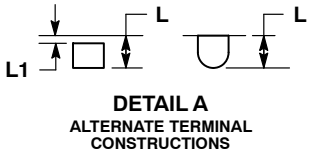
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TIE BARS MAY BE VISIBLE IN THIS VIEW AND ARE CONNECTED TO THE THERMAL PAD.

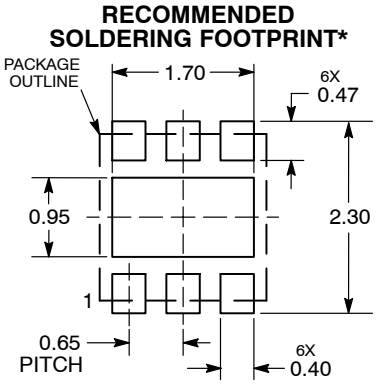
DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.25	0.35
D	2.00 BSC	
D2	1.50	1.70
E	2.00 BSC	
E2	0.80	1.00
e	0.65 BSC	
L	0.25	0.35
L1	---	0.15



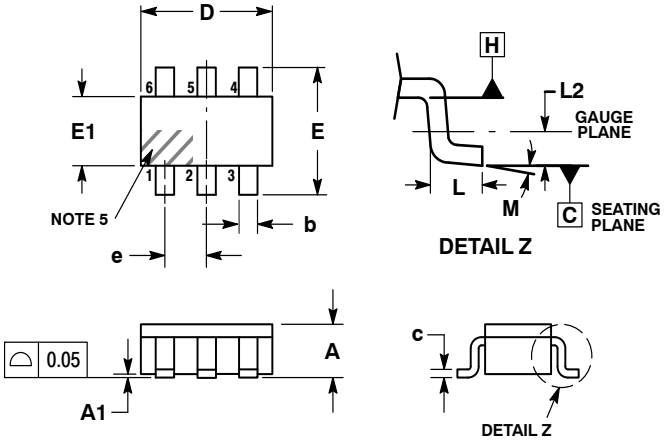








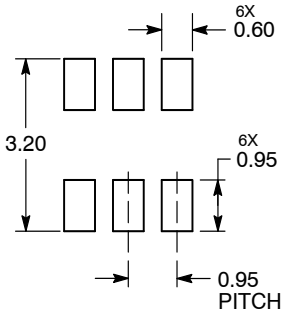
SOT23-6



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	–	10°

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS