RoHS HAL

PB Green

Silicon Carbide Power MOSFET
N-Channel Enhancement Mode

Features

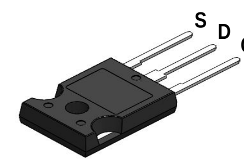
- High Blocking Voltage with Low On-Resistance
- High Speed Switching with Low Capacitances
- Easy to Parallel and Simple to Drive
- Avalanche Ruggedness
- Halogen Free, RoHS Compliant

Typical Applications

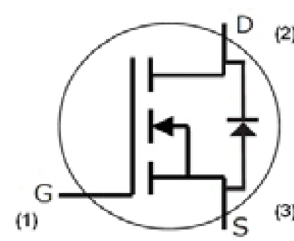
- Solar inverters
- Switch Mode Power Supplies
- High voltage DC/DC converters
- Battery Chargers
- Motor Drives
- Pulsed Power applications

Benefits

- Higher System Efficiency
- Reduced Cooling Requirements
- Increased Power Density
- Increase system switching frequency



TO-247-3



ORDERING INFORMATION

HT36N1200ADZ

T_A = -55° to 150° C for all packages

Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain - Source Voltage	V_{DS}			1200	V	$T_C = 25°C$	
Maximum Gate - Source Voltage	$V_{GS(max)}$	-10		+25		Transient	
Operational Gate-Source Voltage	$V_{GS\ op}$		-5/20			Static	Note 1
DC Continuous Drain Current	I_D			36	A	$V_{GS} = 20$ V, $T_C = 25$ °C, $T_J \le 150$ °C	Fig. 19 Note 2
				24		$V_{GS} = 20$ V, $T_C = 100$ °C, $T_J \le 150$ °C	
Pulsed Drain Current	I_{DM}			80		t_{Pmax} limited by T_{jmax} $V_{GS} = 20V$, $T_C = 25$ °C	Fig. 22
Power Dissipation	P_D			192	W	$T_C = 25$ °C, $T_J = 150$ °C	Fig. 20
Operating Junction and Storage Temperature	T_J, T_{stg}			-55 to +150	°C		
Solder Temperature	T_L			260		According to JEDEC J-STD-020	
Mounting Torque	M_D			1 8.8	Nm lbf-in	M3 or 6-32 screw	

Note (1): Recommended turn-on gate voltage is 20V with ±5% regulation tolerance, see Application Note PRD-04814 for additional details
Note (2): Verified by design

Electrical Characteristics (T_C = 25°C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	1200	—	—	V	V_{GS} = 0 V, I_D = 100 µA	
Gate Threshold Voltage	$V_{GS(th)}$	2.0	2.9	4	V	V_{DS} = $V_{GS,}$ I_D = 5 mA	Fig. 11
		—	2.4	—		V_{DS} = $V_{GS,}$ I_D = 5 mA, T_J = 150°C	
Zero Gate Voltage Drain Current	I_{DSS}	—	1	100	µA	V_{DS} = 1200 V, V_{GS} = 0 V	
Gate-Source Leakage Current	I_{GSS}	—	—	250	nA	V_{GS} = 20 V, V_{DS} = 0 V	
Drain-Source On-State Resistance	$R_{DS(on)}$	—	80	98	mΩ	V_{GS} = 20 V, I_D = 20 A	Fig. 4, 5, 6
		—	144	—		V_{GS} = 20 V, I_D = 20 A, T_J = 150°C	
Transconductance	g_{fs}	—	10	—	S	V_{DS}= 20 V, I_{DS}= 20 A	Fig. 7
			9			V_{DS}= 20 V, I_{DS}= 20 A, T_J = 150°C	
Input Capacitance	C_{iss}	—	1130	—	pF	V_{GS} = 0 V V_{DS} = 1000 V f = 1 Mhz V_{AC} = 25 mV	Fig. 17, 18
Output Capacitance	C_{oss}	—	92	—			
Reverse Transfer Capacitance	C_{rss}	—	7.5	—			
C_{oss} Stored Energy	E_{oss}	—	50	—	µJ		Fig. 16
Avalanche Energy, Single Pluse	E_{AS}	—	1		J	I_D = 20 A, V_{DD} = 50V	Fig. 29
Turn-On Switching Energy	E_{on}	—	523	—	µJ	V_{DS} = 800 V, V_{GS} = -5 V/20 V, I_D = 20 A, $R_{G(ext)}$ = 2.5 Ω, L= 156 µH	Fig. 25
Turn-Off Switching Energy	E_{off}	—	72	—			
Turn-On Delay Time	$t_{d(on)}$	—	15	—	ns	V_{DD} = 800 V, V_{GS} = -5 V/20 V I_D = 20 A, $R_{G(ext)}$ = 2.5 Ω, R_L = 40 Ω, Timing relative to V_{DS} Per IEC60747-8-4 pg 83	Fig. 27
Rise Time	t_r	—	22	—			
Turn-Off Delay Time	$t_{d(off)}$	—	24	—			
Fall Time	t_f	—	14	—			
Internal Gate Resistance	$R_{G(int)}$	—	3.9	—	Ω	f = 1 MHz, V_{AC} = 25 mV	
Gate to Source Charge	Q_{gs}	—	17	—	nC	V_{DS} = 800 V, V_{GS} = -5/20 V I_D = 20 A Per IEC60747-8-4 pg 21	Fig. 12
Gate to Drain Charge	Q_{gd}	—	29	—			
Total Gate Charge	Q_g	—	71	—			

Reverse Diode Characteristics

Parameter	Symbol	Typ.	Max.	Unit	Test Conditions	Notes
Diode Forward Voltage	V_{SD}	4.3	—	V	V_{GS} = -5 V, I_{SD} = 10 A	Fig. 8, 9, 10
Diode Forward Voltage		3.8	—		V_{GS} = -5 V, I_{SD} = 10 A, T_J = 150°C	
Continuous Diode Forward Current[1]	I_S	—	36	A	T_C = 25°C	Note 1
Reverse Recovery Time[1]	t_{rr}	24	—	ns	V_{GS} = -5 V, I_{SD} = 20 A, V_R = 800 V di_F/dt = 1950 A/µs	Note 1
Reverse Recovery Charge[1]	Q_{rr}	152	—	nC		
Peak Reverse Recovery Current[1]	I_{RRM}	10	—	A		

Note:
[1] When using SiC Body Diode the maximum recommended V_{GS} = -5V

Thermal Characteristics

Parameter	Symbol	Typ	Max.	Unit	Note
Thermal Resistance from Junction to Case	$R_{\theta JC}$	0.60	0.65	°C/W	Fig. 21
Thermal Resistance From Junction to Ambient	$R_{\theta JA}$	—	40		

Typical Performance

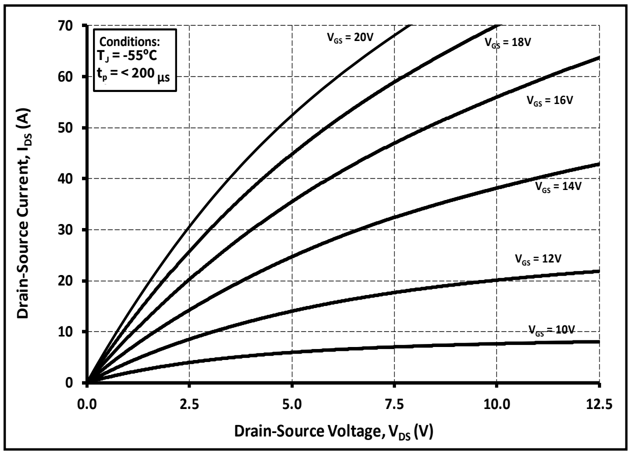


Figure 1. Output Characteristics T_J = -55°C

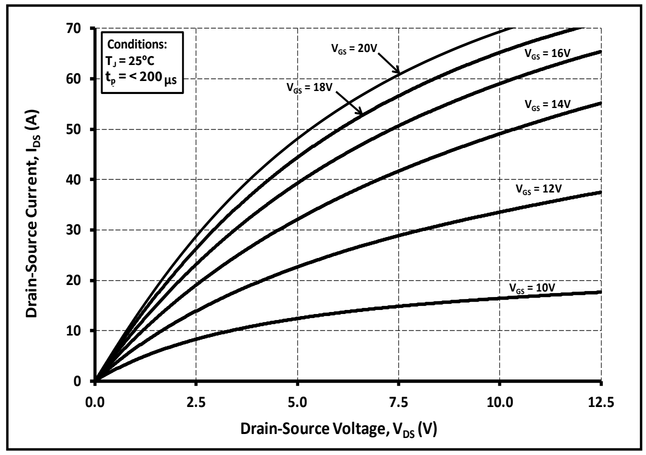


Figure 2. Output Characteristics T_J = 25°C

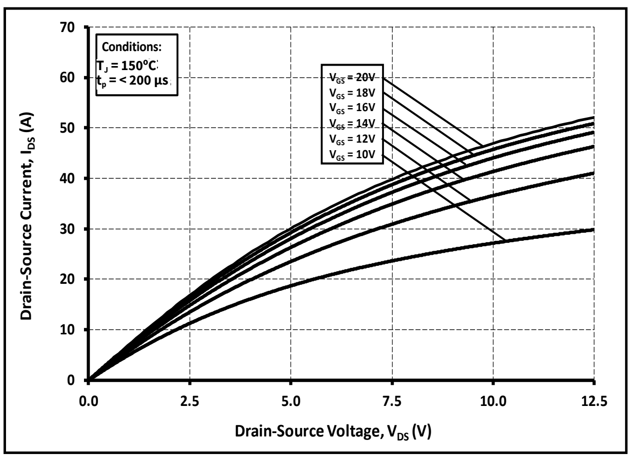


Figure 3. Output Characteristics T_J = 150°C

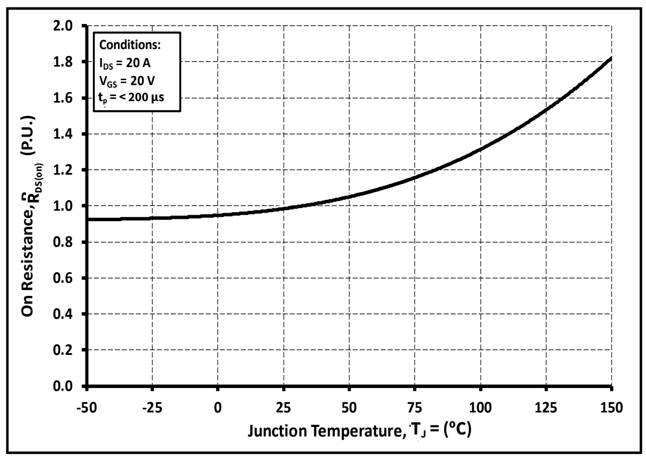


Figure 4. Normalized On-Resistance vs. Temperature

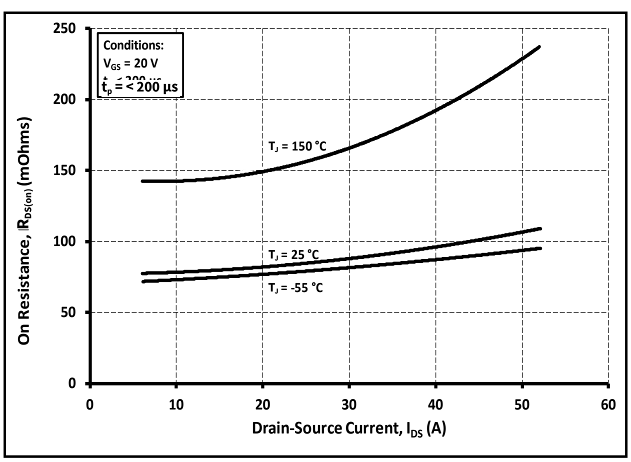


Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

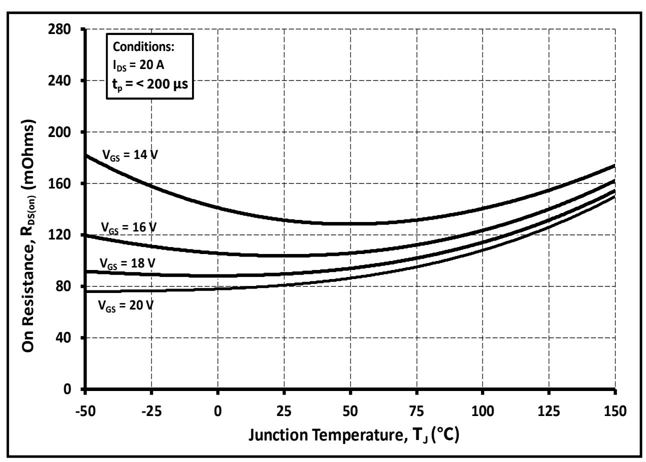


Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

Typical Performance

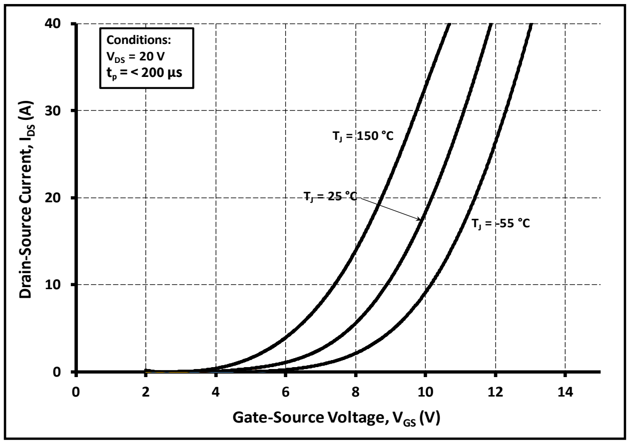


Figure 7. Transfer Characteristic For Various Junction Temperatures

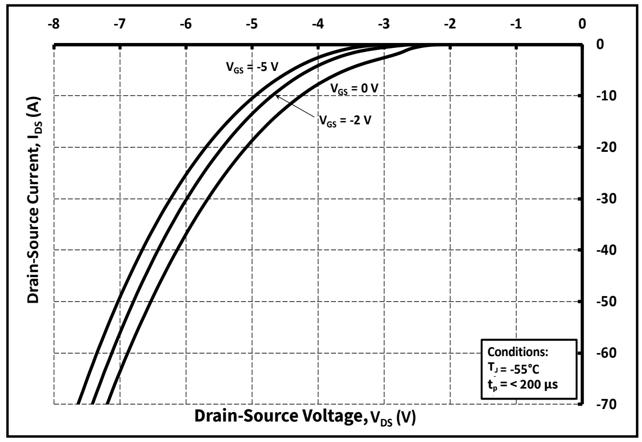


Figure 8. Body Diode Characteristic at -55℃

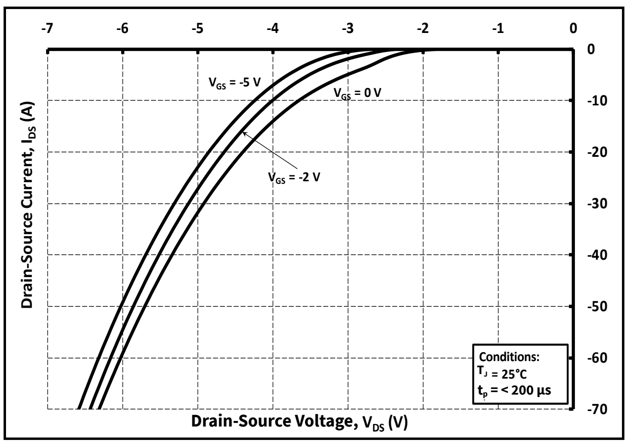


Figure 9. Body Diode Characteristic at 25℃

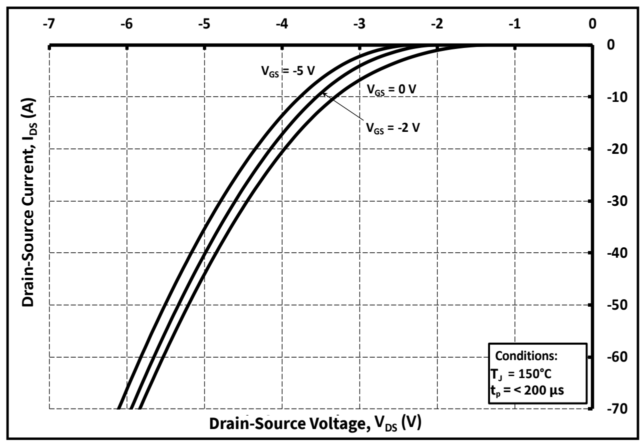


Figure 10. Body Diode Characteristic at 150℃

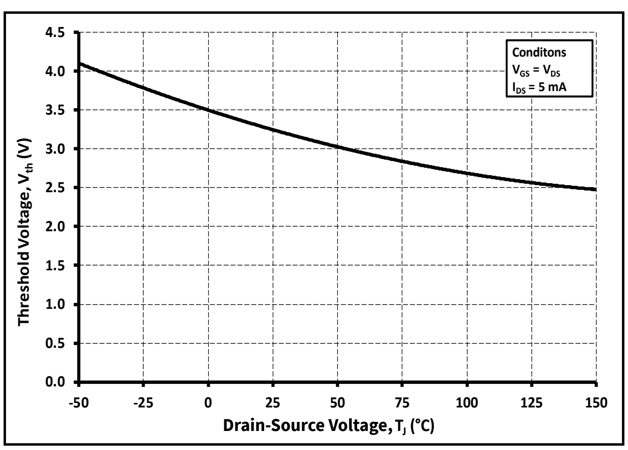


Figure 11. Threshold Voltage vs. Temperature

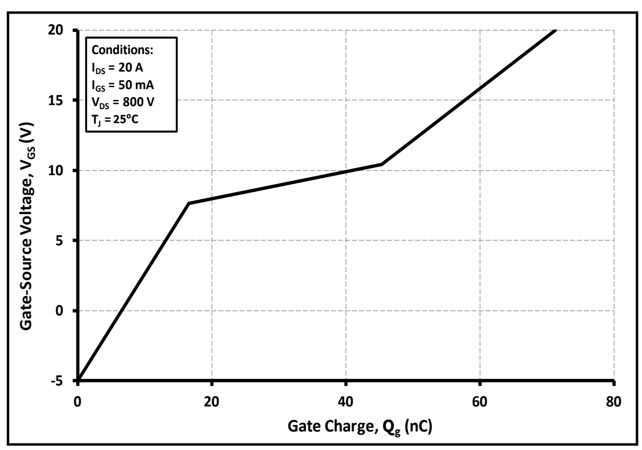


Figure 12. Gate Charge Characteristics

Typical Performance

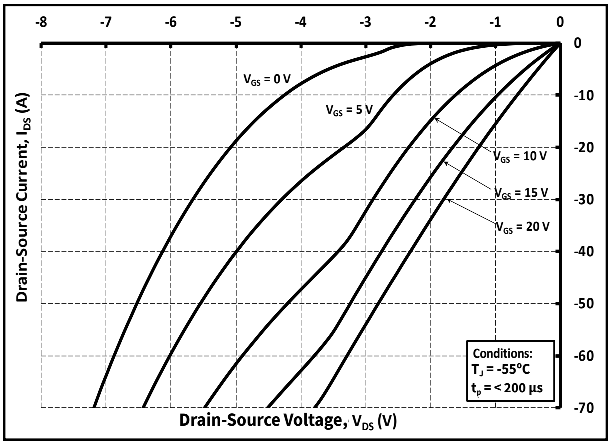


Figure 13. 3rd Quadrant Characteristic at -55℃

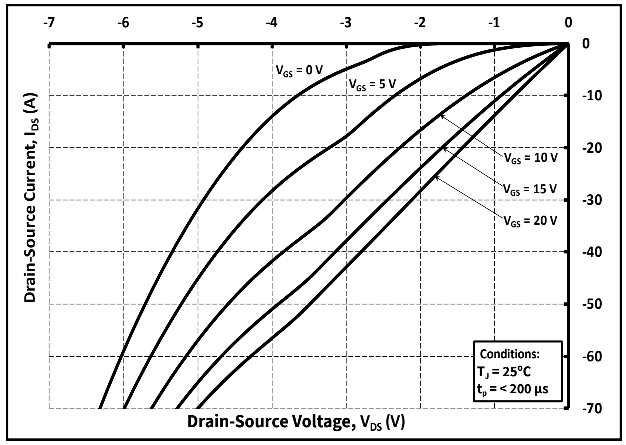


Figure 14. 3rd Quadrant Characteristic at 25℃

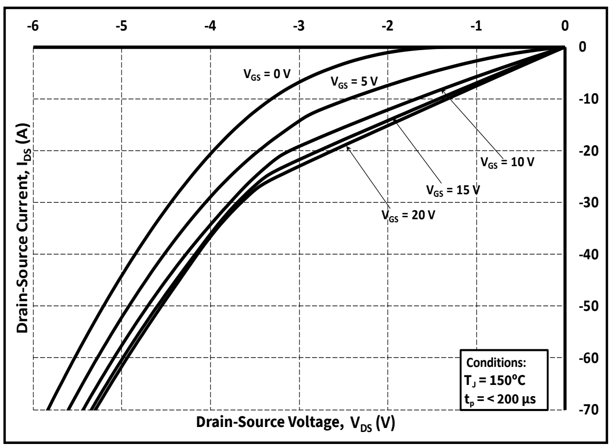


Figure 15. 3rd Quadrant Characteristic at 150℃

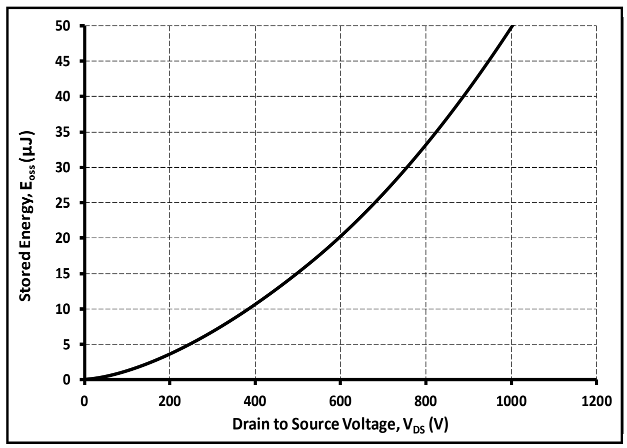


Figure 16. Output Capacitor Stored Energy

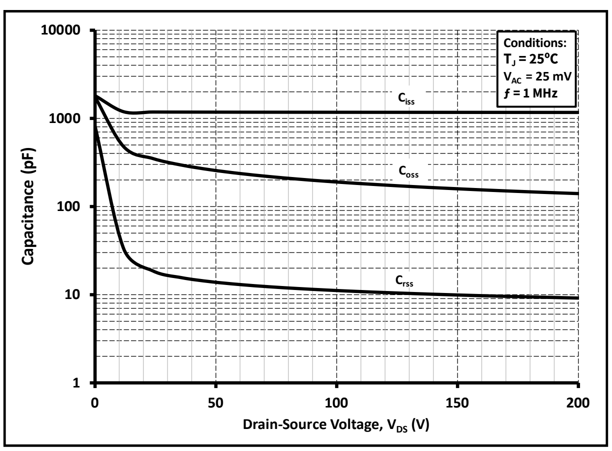


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200 V)

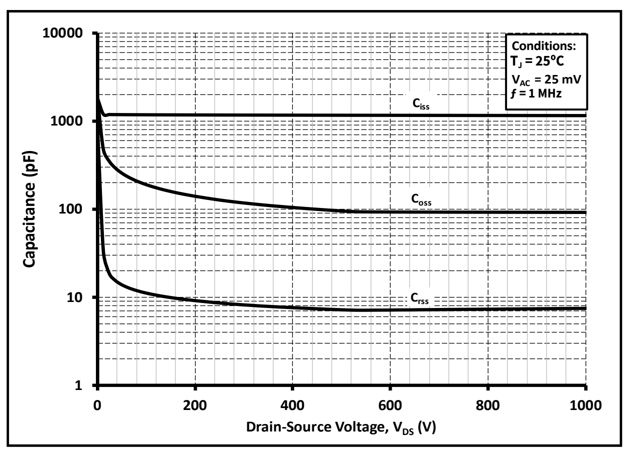


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 1000 V)

Typical Performance

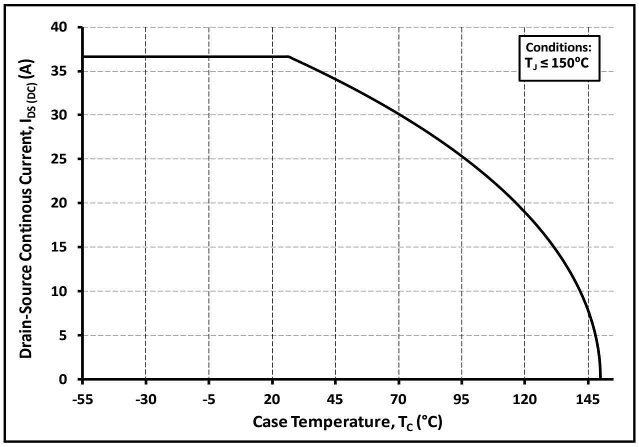


Figure 19. Continuous Drain Current Derating vs. Case Temperature

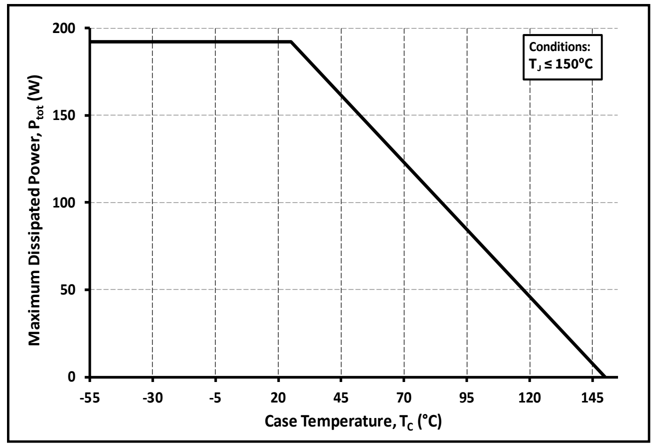


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

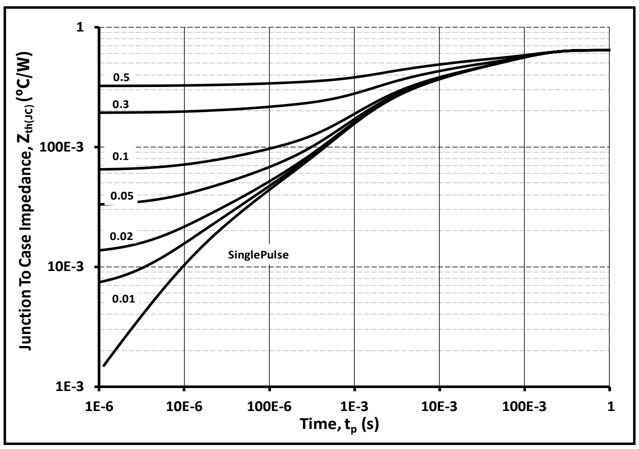


Figure 21. Transient Thermal Impedance (Junction - Case)

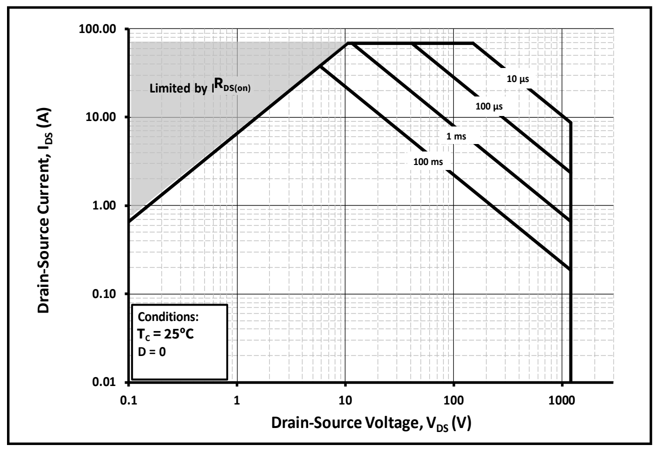


Figure 22. Safe Operating Area

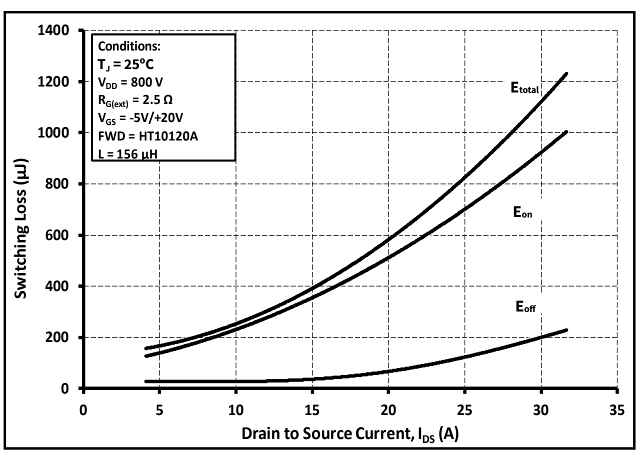


Figure 23. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 600 V)

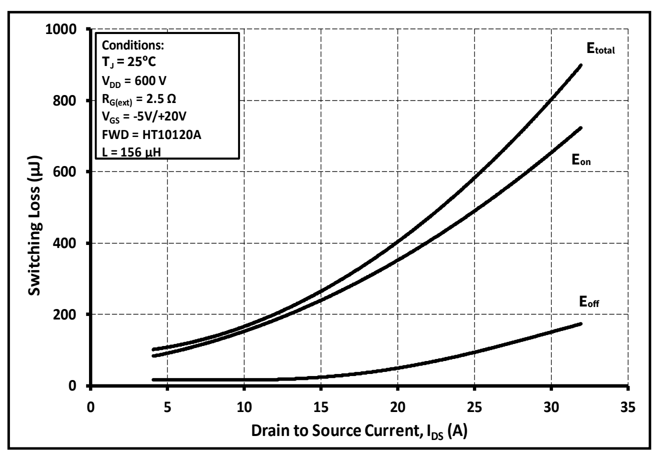


Figure 24. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 800 V)

Typical Performance

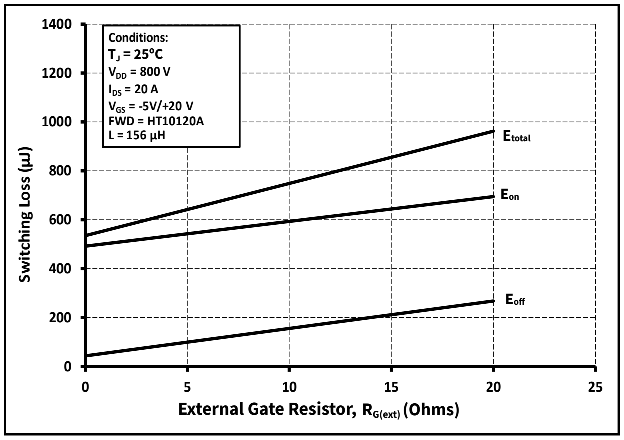


Figure 25. Clamped Inductive Switching Energy vs $R_{G(ext)}$

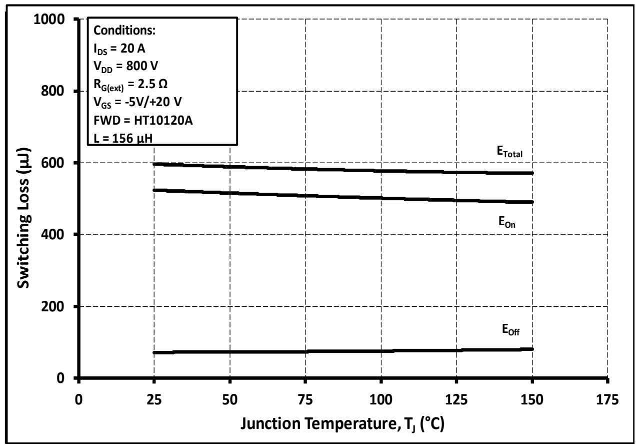


Figure 26. Clamped Inductive Switching Energy vs. Temperature

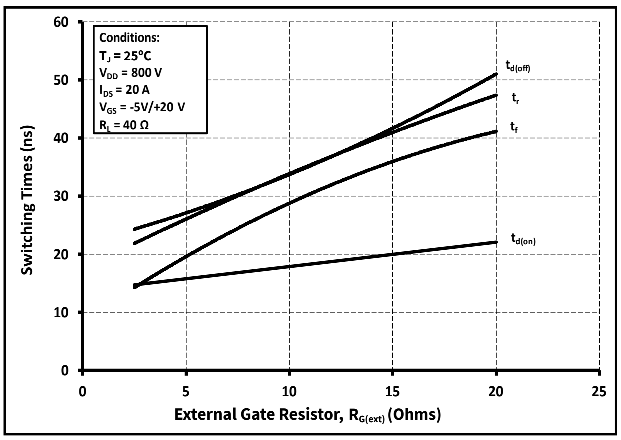


Figure 27. Switching Times vs. $R_{G(ext)}$

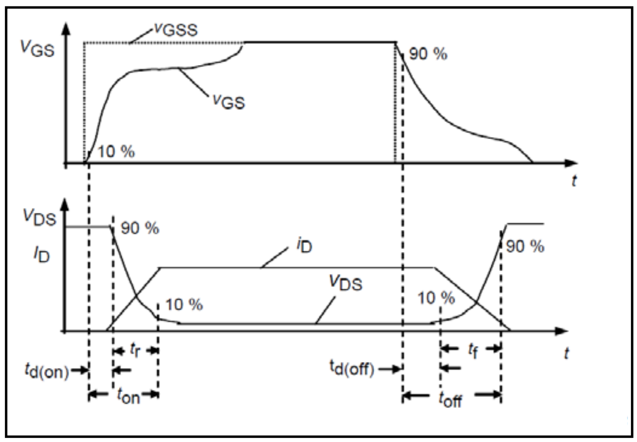


Figure 28. Switching Times Definition

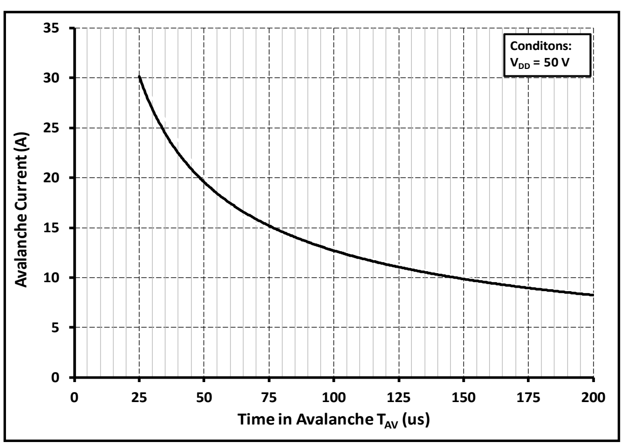


Figure 29. Single Avalanche SOA curve

Test Circuit Schematic

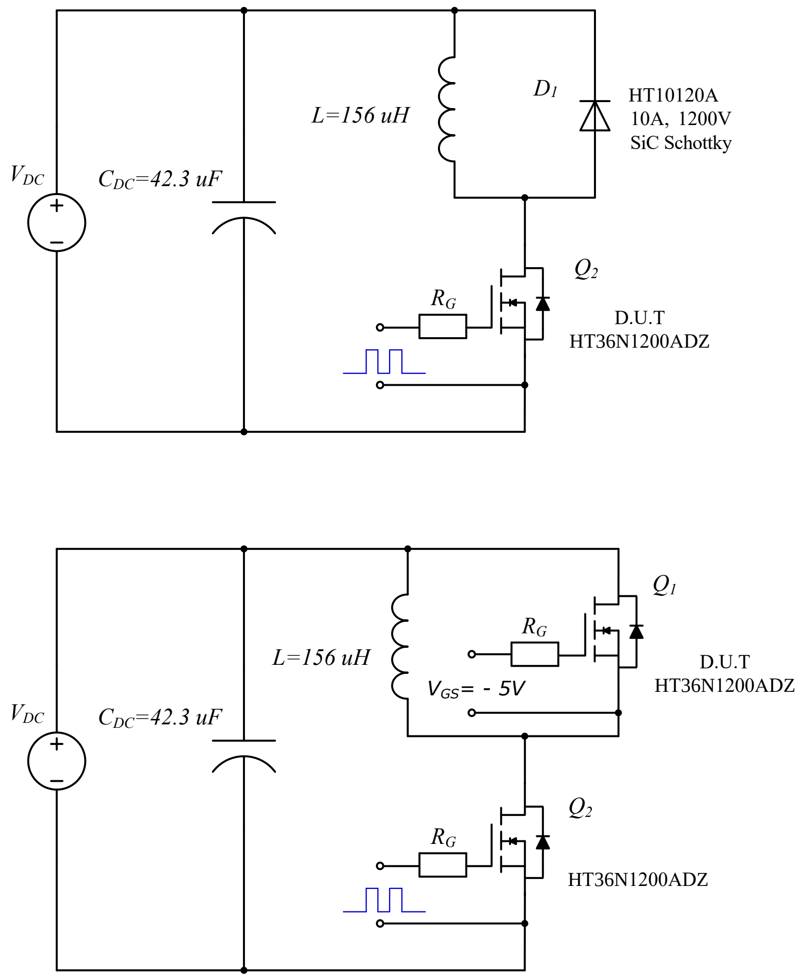
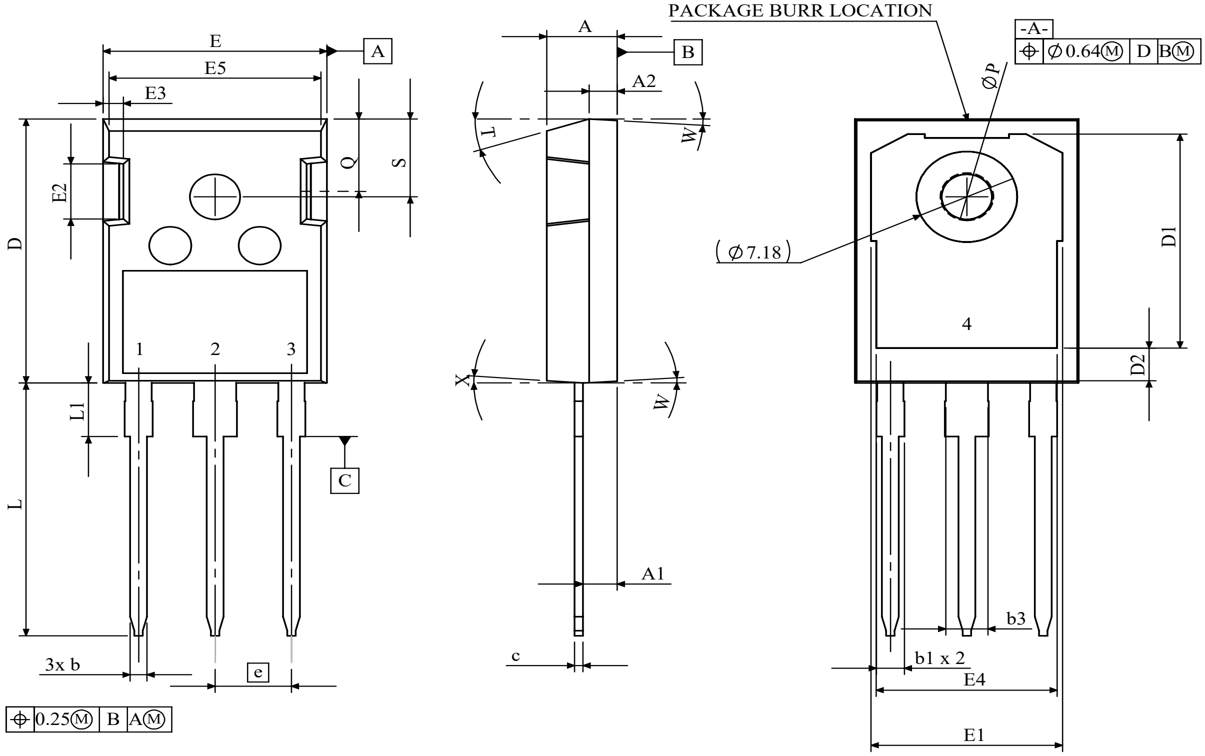


Figure 31. Body Diode Recovery Test Circuit

Package Dimensions – TO-247-3L



SYMBOL	MIN (mm)	MAX (mm)
A	4.83	5.21
A1	2.27	2.52
A2	1.91	2.16
b	1.07	1.33
b1	1.91	2.41
b3	2.87	3.38
c	0.55	0.74
D	20.75	21.05
D1	16	17.4
D2	2.86	3.26
E	15.75	16.13
E1	13.5	14.55
E2	3.68	5.1
E3	1	1.9
E4	12.38	13.43
E5	14.65	15.05
e	5.44 BSC	
L	19.73	20.48
L1	3.97	4.69
∅P	3.18	4.06
Q	5.42	5.96
S	5.85	6.49
T	17.5° REF.	
W	3.5° REF.	
X	4° REF.	

1	GATE
2	DRAIN
3	SOURCE
4	DRAIN

NOTES:
1. ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT.
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
3. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. BURR OR MOLD FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS

Recommended Solder Pad Layout